Practical Concerns and Solutions in Integrated High-Resolution ADCs

揭路
清华大学
High Resolution ADC Needs

- General specifications
  - High SNDR: $>90\text{dB}$
  - High efficiency: $>175\text{dB FoMs}$
  - Med-low speed: kHz $\sim$ MHz BW

IoT Devices
Sensor Readout
Biomedical
Acoustic
Varieties of Solutions Exist

• General specifications
  • High SNDR: >90dB
  • High efficiency: >175dB FoMs
  • Med-low speed: kHz ~ MHz BW

[Graph showing performance metrics for different ADC types]

[B. Murmann, “ADC Survey” Jun 2021]
Problem Solved?

• High **SNDR** and **FoM** – Achieved

• Higher **BW** – on the way

• But we concern **MORE** in practice!
  • Especially for integrated ADC IP

E.g. Wearable devices, IoT, smart sensing…
Process and Area Concerns

- Many **advanced** high-resolution ADCs are made in **old process**
  - And they are large too
- But SoC prefers **advanced process**

![Published high-resolution ADCs](image)

[B. Murmann, “ADC Survey” Jun 2021]
Driving Effort

- Driving high-resolution Nyquist ADC is a big challenge
  - $C_s$ is large for low $KT/C$

- Oversampling does not fully relax driving effort
  - Need to charge $C_s$ faster
Nyquist And Single-End Capability

- Many applications need a “Nyquist” ADC
  - Support single-shot conversion
  - Support multiplexing

- Single-ended capability is also desired
  - Compatible with various input formats
  - i.e., a high full-scale CMRR
And More …

• **Decoupling**
  • Many high-resolution ADCs heavily rely on *large decaps*
  • Typically for stabilizing / denoise references
  • E.g. SAR ADC

• **Calibration and trimming**
  • Foreground calibration / trimming increases *testing cost*
  • Background calibration / DEM increases *P/A cost*

• **PVT robustness**
  • Sometimes ignored by academic designs

…
The Complete Wish List

- High SNDR and FoM → ✔ Lots of solutions

Practical Features:
- Advanced process compatible → ✗ OTA, high swing -> more digital?
- Low area
- Easy driving
- Nyquist capable
- Single-ended capable
- Easy decoupling
- Calibration / trimming free
- PVT Robust

…

- SAR / pipe -> oversampling? KT/C cancel?
- DSM -> Incremental?
- CT-DSM ?
- Open loop based ?
The Complete Wish List

✓ High SNDR and FoM

Practical Features:
✓ Advanced process compatible
✓ Low area
✓ Easy driving
✓ Nyquist capable
✓ Single-ended capable
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✓ PVT Robust

…
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The “Zoom” Framework

- **Slow coarse stage + single-bit DSM**
  - ✓ Effectively multi-bit
  - ✓ Inherent linear DSM
  - ✓ Low DAC toggle rate
  - ✓ Small input to LF
  - ✗ DAC mismatch unsolved
  - ✗ Only works for DC
  - ✗ Massive SC input sampling

![Diagram of the “Zoom” Framework](image)

\[F_{CLK} = \text{OSR} \times F_S\]
Mismatch Error in DAC

- Mismatch error in DAC brings nonlinearity

### Thermometer DAC (2bits)

<table>
<thead>
<tr>
<th>Activation Map</th>
<th>Time</th>
<th>Mean Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>E4</td>
<td>4</td>
<td>E1</td>
</tr>
<tr>
<td>E3</td>
<td>1</td>
<td>E1</td>
</tr>
<tr>
<td>E2</td>
<td>3</td>
<td>E1+E2+E3</td>
</tr>
<tr>
<td>E1</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

Mismatch Error (E1)

Mean Error

\[ E \propto D_{IN} \rightarrow \text{Distortion} \]
The "Real Time" (RT) DEM

• Circulate the elements step-by-step for a complete round

<table>
<thead>
<tr>
<th>Activation Map</th>
<th>Thermometer DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td>D_{IN}</td>
</tr>
<tr>
<td>E4</td>
<td>E3</td>
</tr>
<tr>
<td>E3</td>
<td>E3</td>
</tr>
<tr>
<td>E2</td>
<td>E2</td>
</tr>
<tr>
<td>E1</td>
<td>E1</td>
</tr>
</tbody>
</table>

| RT-DEM DAC |
| D_{IN} | E4 | E4 | E4 | E4 | E4 |
| E4 | E3 | E3 | E3 | E3 | E3 |
| E3 | E3 | E2 | E2 | E2 | E2 |
| E2 | E2 | E2 | E2 | E2 | E2 |
| E1 | E1 | E1 | E1 | E1 | E1 |

Error ∝ D_{IN} ⟷ Distortion

Mean Error

\[ \text{Mean Error} = \frac{(E_1 + E_2 + E_3 + E_4)}{4} \]

Linear gain error

\[ \text{Error} \propto D_{IN} \]
The “Real Time” (RT) DEM

- Remove mismatch completely
- Simple implementation

![Diagram of RT-DEM DAC]

<table>
<thead>
<tr>
<th>E4</th>
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<tr>
<td>E2</td>
<td>E2</td>
<td>E2</td>
<td>E2</td>
<td>E2</td>
</tr>
<tr>
<td>E1</td>
<td>E1</td>
<td>E1</td>
<td>E1</td>
<td>E1</td>
</tr>
</tbody>
</table>

\[ \text{Error } \propto D_{\text{IN}} \rightarrow \text{Linear gain error} \]
The “Real Time” (RT) DEM

✓ Remove mismatch completely
✓ Simple implementation

• Limitations
  - High OSR
  - 1\textsuperscript{st}-order IDSM

OK for advanced process

Evenly weighted
Decoupled Stages with RT-DEM

- Simple hardware
- Completely remove mismatch
- Low toggle rate
- Code independent ripple

? Cannot track AC
Introduce Tracking Mechanism

- Simple hardware
- Completely remove mismatch
- Low toggle rate
- Code independent ripple
- Tracks input
- Gain calibration free
✓ Simple hardware
✓ Completely remove mismatch
✓ Low toggle rate
✓ Code independent ripple
✓ Tracks input
✓ Gain calibration free

? Needs complicated B2T

- What is the simplest ADC providing “thermometer” output?
Simplest – Counting ADC

- Ramp DAC’s output till $V_{IN}$
- Count the steps of ramping

✓ Reusing the DEM and DAC
  ✓ No B2T!
  ✓ Low power
  ✓ Compact
Even Simpler – Comparator Reuse

- Ramp DAC’s output till $V_{IN}$
- Count the steps of ramping

✓ Reusing all hardware
  ✓ No B2T!
  ✓ Low power
  ✓ Even more compact!

![Diagram of comparator reuse](image-url)
Switch to Continuous-Time

- **Gm-C loop filter (integrator)**
  - Fast, settling free
  - High efficiency
  - Linearity relaxed by small input
  - Low swing - scaling friendly

- **Cap-coupled input**
  - Easy driven
  - kT/C noise free
“Zoom of Incremental + Counting” (ZIC)

✓ High SNDR
✓ Good scalability
✓ Small and simple
✓ Easy driving
✓ Stable Vref ripple
✓ Nyquist capable
✓ Calibration free
✓ PVT Robust
Input Network Concern

- Cap coupling – easy driving
- Cannot accept DC input

\[ C_U = 12.5fF \]
\[ C_{IN} = 132C_U \]
Input Network Concern

- Cap coupling – easy driving
- Reset during idle
  ✓ Reset to $V_{IN,CM}$ gives great CMRR
  × Induce $kT/C$ noise

Half 0, half 1 @ $\Phi_{IDLE}$
(effectively $V_{CM}$)

Cap coupling – easy driving
Reset during idle
- Reset to $V_{IN,CM}$ gives great CMRR
- Induce $kT/C$ noise

Half 0, half 1 @ $\Phi_{IDLE}$ (effectively $V_{CM}$)
Input Network Concern

- Cap coupling – easy driving
- Reset during idle
- Apply chopping – $kT/C$ is DC error
  ✓ Also suppress flicker noise and leakages
Input Network Concern

- Cap coupling – easy driving
- Reset during idle
- Apply chopping
  - $V_{IN,CM} = (V_{IN}^+ + V_{IN}^-)/2$
  - Sample both $V_{IN}$ on split $C_{IN}$
  - Chopping is embedded

[H. Wang, ISSCC’17]
Full Schematic

Gm reused as a pre-amplifier
✓ Suppress comparator offset

Comparator don’t care integrator gain
✓ Inherently PVT robust

4-tap FIR DAC
✓ Small swing
✓ Jitter insensitive

- V_IN+
- V_IN-
V_REF+
V_IN+
V_REF−
V_IN−

Chopper (XOR)
Circular Shifter
FIR

GND

Φ
DSM

Φ
CNT

V_DD

FIR

CNT
(14b)

DSM

D
INT
(14b)

D
OUT

Count

Shifter

Control

Intergrator

7

x32

V_INT

DCS

V裒

7

V_TOP
Dynamic Power Concern

-market concerns and solutions in integrated high-resolution ADCs

-Only two DFFs are flipping at each DEM step

-Weak Latch

-Minimum size

-DAC[1]

-DAC[128]

-Loop

-7x DFF

-FIR

-Circular Shift Register

-Connectors

-Minimum size comparator

-Small gate count $\rightarrow \sim 100uW @ 500M F_{CLK}$

-Can be further reduced in advanced process

-Divider chain

-DAC[1]

-DAC[128]

-CNT_{DSM}

-CNT_{Track}
Clock Generation Concern

- The 500MHz clock sounds costly to generate? - Not really
  - ✓ Loose jitter requirement: 3ps rms for 105dB
  - ✓ Loose frequency precision: even ±20% $F_{CLK}$ is tolerable

- A “crappy” free-running relaxation oscillator* is enough
  - ~200uW @ 500M (post sim)
  - 10x40um
  - No trimming needed

*Not used in actual measurement
Prototype ADC

- 28nm CMOS
- Core Area: 90x160 um²

28nm CMOS
Core Area: 90x160 um²
Single-Tone Test @20kS/s

$2^{16}$-FFT, 16x Averaged

SNDR = 102.9dB (16.8bit)  
SFDR = 113.6dB

-0.7dB @ 2.3kHz

SNDR = 99.1dB (16.2bit)  
SFDR = 113.9dB

(Tracking slope limited) -7.0dB @ 9.9kHz
**CMRR and Single-Ended Input**

- **CMRR**
  - >105dB full-scale CMRR @100Hz
  - 80dB CMRR up to 10kHz

- **SNDR**
  - 95.1dB (15.5bit)

- **SFDR**
  - 101.0dB

- **PSD**
  - -7.3dB @ 2.3kHz (SE input)

- **AC line**
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PVT Measurements

SNDR\text{ \textsubscript{raw}} = 101.7 \text{ dB}

SNDR\text{ \textsubscript{cal}} = 102.0 \text{ dB}

No need to cal. in practice!
**SOTA Design Comparison**

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Process (nm)</th>
<th>Area (mm²)</th>
<th>Supply (V)</th>
<th>OSR</th>
<th>F_s,nyq (kS/s)</th>
<th>Power (mW)</th>
<th>SNDR (dB)</th>
<th>FOM_s (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>This work</strong></td>
<td>28</td>
<td>0.014</td>
<td>0.9 / 1.2</td>
<td>2¹⁴</td>
<td>2¹³</td>
<td>0.47</td>
<td>102.9</td>
<td>176.2</td>
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<tr>
<td><strong>ISSCC’22</strong></td>
<td>160</td>
<td>0.27</td>
<td>1.8</td>
<td>87.5</td>
<td>40</td>
<td>0.59</td>
<td>100.1</td>
<td>176.4</td>
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<tr>
<td><strong>VLSI’20</strong></td>
<td>65</td>
<td>0.134</td>
<td>1.2</td>
<td>256</td>
<td>40</td>
<td>0.44</td>
<td>106.5</td>
<td>183.1</td>
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<tr>
<td><strong>VLSI’18</strong></td>
<td>65</td>
<td>0.39</td>
<td>1.2</td>
<td>150</td>
<td>48</td>
<td>0.55</td>
<td>100.8</td>
<td>176.4</td>
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<tr>
<td><strong>ISSCC’21</strong></td>
<td>180</td>
<td>0.78</td>
<td>1.8 / 5</td>
<td>1</td>
<td>2000</td>
<td>0.14</td>
<td>100.9</td>
<td>183.3</td>
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<tr>
<td><strong>ISSCC’22</strong></td>
<td>40</td>
<td>0.061</td>
<td>1.1</td>
<td>25</td>
<td>80</td>
<td>8.5</td>
<td>105.3</td>
<td>186.0</td>
</tr>
<tr>
<td><strong>ISSCC’20</strong></td>
<td>40</td>
<td>0.061</td>
<td>1.1</td>
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<td>80</td>
<td>8.5</td>
<td>105.3</td>
<td>186.0</td>
</tr>
</tbody>
</table>

- Includes decimation filter.
- FOM_s (dB) includes decimation filter.
## Practical Features

<table>
<thead>
<tr>
<th>Architecture</th>
<th>ISSCC’22 This work</th>
<th>VLSI’20 E. Elan</th>
<th>VLSI’18 B. Wang</th>
<th>ISSCC’21 S. Mondal</th>
<th>ISSCC’22 J. Steensgaard</th>
<th>ISSCC’20 J. Liu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zoom (Cnt’ + CT-IDSM)</td>
<td>Zoom (SAR + DT-DSM)</td>
<td>DT-IDSM</td>
<td>CT-DSM</td>
<td>Multi-step SAR</td>
<td>NS-SAR</td>
<td></td>
</tr>
<tr>
<td>Full-Scale CMRR @ DC</td>
<td>&gt;100dB</td>
<td>&gt;100dB</td>
<td>Not Support</td>
<td>Not Support</td>
<td>140dB</td>
<td>Not Support</td>
</tr>
<tr>
<td>Multiplexing / Single-Shot</td>
<td>Incremental</td>
<td>Not Support</td>
<td>Incremental</td>
<td>Not Support</td>
<td>Nyquist Sampling</td>
<td>Not Support</td>
</tr>
<tr>
<td>PVT</td>
<td>Stable</td>
<td>Stable</td>
<td>Stable</td>
<td>Not Report</td>
<td>Stable</td>
<td>Stable</td>
</tr>
<tr>
<td>Mismatch Solution</td>
<td>RT-DEM</td>
<td>DWA</td>
<td>DWA</td>
<td>1bit-DAC</td>
<td>Cal. + DEM</td>
<td>MES</td>
</tr>
<tr>
<td>Input Network</td>
<td>Cap Coupling</td>
<td>Switched Cap</td>
<td>Switched Cap</td>
<td>Resistive</td>
<td>Switched Cap</td>
<td>Switched Cap</td>
</tr>
</tbody>
</table>
Area & Process Highlight

[B. Murmann, “ADC Survey” Jun 2021]
Conclusion

• **Prototype Highlights:**
  
  • Smallest for 90+dB SNDR
  
  • Highest SNDR for 28nm
  
  • Nyquist and single-end capability

• **Suggestions for designing integrated high-resolution ADC**
  
  • Always consider the deployment in practice
  
  • Take advantage of fast digital (e.g. high OSR)
  
  • Simple analog circuitry is preferred
  
  • Architecture hybridization is promising
Thanks!

Q&A