A Battery-Input Sub-1V Output 92.9% Peak Efficiency 0.3A/mm² Current Density Hybrid SC-Parallel-Inductor Buck Converter with Reduced Inductor Current in 65nm CMOS

Guigang Cai¹, Yan Lu¹, Rui P. Martins¹,²
¹University of Macau, Macao, China
²On leave from University of Lisboa, Lisbon, Portugal
Outline

- Background and Motivation
- Proposed CPL-Buck Converter with Reduced Inductor Current
  - Topology and Working Principle
  - Conduction Loss Reduction
  - $V_{\text{OUT}}$ Drop Due to DCR and Switch On-Resistances
- Circuit Implementation
- Measurement Results
- Conclusions
Outline

- Background and Motivation
- Proposed CPL-Buck Converter with Reduced Inductor Current
  - Topology and Working Principle
  - Conduction Loss Reduction
  - $V_{OUT}$ Drop Due to DCR and Switch On-Resistances
- Circuit Implementation
- Measurement Results
- Conclusions
Compact Electronic Devices

- Small volume: high current density.
- High efficiency: prolong the usage time.
- Large voltage conversion ratio (VCR): 3-4.2V to sub-1V.
Pros: Wide VCR range, easy to implement.
Cons: Large $\Delta I_L$, high DCR loss, narrow duty ratio at high VCR.
Flying Capacitor Multilevel Converter

- Wide VCR range.
- Small $\Delta I_L$.
- Extended duty ratio.
- High DCR loss.
- Flying cap. balancing issue.
Hybrid Converter with Reduced $I_L$

N. Tang et. al., ISSCC 2019

$V_{IN}$

$L$

$S_1$

$V_X$

$C_F$

$S_2$

$V_{OUT}$

$S_3$

$C_{OUT}$

$I_{OUT}$

$V_{OUT}$

$I_L$

$V_X$

$2V_{OUT}$

$V_{OUT}$

$DT$

$t$

$I_{OUT}$

$I_{OUT}/(2-D)$

$t$

$V_{CF} = V_{OUT}$

$I_L = \frac{I_{OUT}}{2 - D}$

$V_{OUT} = \frac{V_{IN}}{2 - D}$

ICAC 2022
Hybrid Converter with Reduced $I_L$

C. Hardy et al., ISSCC 2019

$V_{CF1} = 2V_{OUT}$

$V_{CF2} = V_{OUT}$

$V_{o1} = \frac{V_{IN}}{3-D}$

$I_L = \frac{I_{o1}}{3-D}$
Hybrid Converter with Reduced $I_L$

- Reduced $I_L$, low DCR loss.
- $V_{IN}/2 < V_{OUT} < V_{IN}$
- $C_F$ automatic balance.
- $V_{IN}/3 < V_{O1} < V_{IN}/2$
- Limited VCR range.
Hybrid Converter with Reduced $I_L$

Always-Dual-Path (ADP) hybrid converter.

- Reduced $I_L$, low DCR loss.
- $C_F$ automatic balance.
- High VCR
- Large $\Delta I_L$.
Outline

- Background and Motivation
- Proposed CPL-Buck Converter with Reduced Inductor Current
  - Topology and Working Principle
  - Conduction Loss Reduction
  - $V_{\text{OUT}}$ Drop Due to DCR and Switch On-Resistances
- Circuit Implementation
- Measurement Results
- Conclusions
Proposed CPL-Buck Converter

- $L$ at the output side for large VCR regulation.
- $C_{F1}$ in-series with $L$ reduces inductor switching node ($V_{F2}$) voltage.
- SC in-parallel with $L$ (CPL) reduces $I_L$.
Working Principle: Sub-1/3X Mode
Working Principle: Sub-1/3X Mode

\[ V_{IN} \]
\[ S_1 \quad V_{F1} \quad S_2 \quad V_{F2} \quad S_3 \quad V_{F3} \quad S_4 \quad V_{F4} \quad S_5 \quad V_{CF2} \quad S_6 \quad V_{CF1} \quad S_7 \quad \Phi_1 \]

0–DT

\[ I_L \]

\[ V_{F1} \]

\[ V_{CF1} \]

\[ \Phi_2 \]

DT–T

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ V_{IN} \]

\[ V_{IN} \]

\[ I_1 \]

\[ I_2 \]

\[ V_{IN} - 2V_{OUT} \]

\[ V_{F2} \]

\[ I_{OUT} \]

\[ I_{OUT} \]

\[ I_{OUT} \]

\[ V_{OUT} \]

\[ I_{OUT} \]

\[ I_{OUT} \]

ICAC 2022
Working Principle: Sub-1/3X Mode

\[ I_L = \frac{I_{OUT}}{1+2D} \]

\[ V_{OUT} = \frac{D}{1+2D} V_{IN} \]

\[ P_{COND,L} = \left( \frac{1}{1+2D} \right)^2 I_{OUT}^2 R_{DCR} \]
Working Principle: Sub-1/2X Mode

\[ V_{IN} - V_{OUT} = \frac{I_{OUT}}{1+D} \]

\[ I_3 \]

\[ I_L \]

\[ V_{F2} \]

\[ V_{IN} - V_{OUT} \]

\[ 0 - DT \]

\[ \phi_1 \]

\[ CF_1 \]

\[ CF_2 \]

\[ VF_1 \]

\[ VF_2 \]

\[ VF_3 \]

\[ VF_4 \]

\[ VF_3 \]

\[ VF_4 \]

\[ VF_2 \]

\[ VF_1 \]

\[ CF_2 \]

\[ CF_1 \]

\[ V_{F1} \]

\[ S_1 \]

\[ S_2 \]

\[ S_3 \]

\[ S_4 \]

\[ S_5 \]

\[ S_6 \]

\[ L \]

\[ C_{OUT} \]

\[ I_{OUT} \]

\[ V_{OUT} \]

\[ I_{OUT} \]
Working Principle: Sub-1/2X Mode

ICAC 2022
Working Principle: Sub-1/2X Mode

$$V_{IN} - V_{OUT}$$

$$I_{OUT} = \frac{I_{OUT}}{1+D}$$

$$V_{OUT} = \frac{D}{1+D} V_{IN}$$

$$P_{COND_L} = \left(\frac{1}{1+D}\right)^2 I_{OUT}^2 R_{DCR}$$
Power Stage Transfer Function

Sub-1/3X Mode

\[ T(s) \approx \frac{V_{IN}}{V_m(1+2D)^2} \cdot \frac{2DL}{R_o(1+2D)^2} \]

Sub-1/2X Mode

\[ T(s) \approx \frac{V_{IN}}{V_m(1+D)^2} \cdot \frac{DL}{R_o(1+D)^2} \]

Left-half-plane (LHP) zero.

The flying capacitors, as well as the duty cycle \( D \), have effect on the complex pole frequency.
Inductor Conduction Loss Reduction

**I_L** and **P\textsubscript{COND\_L}** Expression

<table>
<thead>
<tr>
<th>Work Mode</th>
<th>Sub-1/3X Mode</th>
<th>Sub-1/2X Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>M</strong></td>
<td>(\frac{D}{1+2D})</td>
<td>(\frac{D}{1+D})</td>
</tr>
<tr>
<td><strong>I_L</strong></td>
<td>(\frac{I\text{_OUT}}{1+2D})</td>
<td>(\frac{I\text{_OUT}}{1+D})</td>
</tr>
<tr>
<td><strong>P\textsubscript{COND_L}</strong></td>
<td>((1-2M)^2I^2\text{_OUT}R_L)</td>
<td>((1-M)^2I^2\text{_OUT}R_L)</td>
</tr>
</tbody>
</table>

For VCR=0.3, \(I_L\) is reduced to 0.4\(I\text{\_OUT}\), normalized \(P\text{\_COND\_L}\) is reduced to 0.16.
Total Conduction Loss Reduction

Normalized total conduction loss

- Assume the on-resistance of $S_1$, $S_{2-3}$ and $S_{4-6}$ are $R_1$, $R_2$ and $R_3$, respectively, and assume $R_1=R_2=R_{ON}$, $R_3=0.5R_{ON}$, $R_L=NR_{ON}$.

- $P_{COND\_CPL}$ can be maximumly reduced to 59%, 48%, 35% and 27% with $N=1$, 2, 5 and 10, respectively.
**Inductor Current Ripple**

- Much better than the ADP converter.
- Comparable with 3-level buck converter.

**Inductor Current Ripple Expression**

<table>
<thead>
<tr>
<th></th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-level buck converter</td>
<td>$\Delta I_L = \frac{V_{IN}}{fL} \cdot M(1-2M)$</td>
</tr>
<tr>
<td>ADP hybrid converter</td>
<td></td>
</tr>
<tr>
<td>2-phase mode</td>
<td>$\Delta I_L = \frac{V_{IN}}{fL} \cdot 2M(1-2M)$</td>
</tr>
<tr>
<td>3-phase mode</td>
<td>$\Delta I_L = \frac{V_{IN}}{fL} \cdot M \frac{1.5-3M}{1-M}$</td>
</tr>
<tr>
<td>This work</td>
<td></td>
</tr>
<tr>
<td>sub-1/3X mode</td>
<td>$\Delta I_L = \frac{V_{IN}}{fL} \cdot \frac{(1-3M)}{1-2M}$</td>
</tr>
<tr>
<td>sub-1/2X mode</td>
<td>$\Delta I_L = \frac{V_{IN}}{fL} \cdot \frac{(1-2M)}{1-M}$</td>
</tr>
</tbody>
</table>
$V_{OUT}$ Drop Due to Resistance

In sub-1/3X mode, ideally, $V_{OUT} = \frac{DV_{IN}}{1+2D}$

$V_{CF2} = V_{OUT} + \frac{2R_3I_{OUT}}{1+2D} > V_{OUT}$

$V_{CF1} = 2V_{OUT} + \frac{(R_2 + 2R_3 + D(R_2 - R_3))I_{OUT}}{(1+2D)(1-D)} > 2V_{OUT}$

$V_{OUT} \approx \frac{DV_{IN}}{1+2D} - \frac{(R_2 + R_L + D(R_1 + 2R_3 - R_L) + D^2(-R_1 + R_2 - R_3))I_{OUT}}{(1+2D)^2(1-D)}$

$V_{CF1}$ and $V_{CF2}$ are larger than $2V_{OUT}$ and $V_{OUT}$, respectively. $V_{OUT}$ is smaller than $DV_{IN}/(1+2D)$. 
**$V_{OUT}$ Drop Due to Resistance**

- In light load, $V_{OUT}$ increases with $D$;
- In heavy load, $D$ increases, $V_{OUT}$ will increase first. Then after reaching a peak value, it will drop rapidly.

Simulated $V_{OUT}$ drop with $R_1 = R_L = 80 \text{ mΩ}$, $R_2 = 40 \text{ mΩ}$ and $R_3 = 20 \text{ mΩ}$. 
$V_{\text{OUT}}$ Drop Due to Resistance

- In light load, $V_{\text{OUT}}$ increases with $D$;
- In heavy load, $D$ increases, $V_{\text{OUT}}$ will increase first. Then after reaching a peak value, it will drop rapidly.
- Mode switches based on $D$.

Simulated $V_{\text{OUT}}$ drop with $R_1 = R_L = 80$ mΩ, $R_2 = 40$ mΩ and $R_3 = 20$ mΩ.
Outline

- Background and Motivation
- Proposed CPL-Buck Converter with Reduced Inductor Current
  - Topology and Working Principle
  - Conduction Loss Reduction
  - $V_{\text{OUT}}$ Drop Due to DCR and Switch On-Resistances
- Circuit Implementation
- Measurement Results
- Conclusions
Schematic of the CPL-Buck Converter

- $S_1$: Stacking two 2.5V PMOS transistors.
- $S_2$ and $S_3$: Stacking one 2.5V and one 1V NMOS transistors.
- $S_4$-$6$: 1V NMOS.
- clk_40 and clk_80 with duty ratios of 40% and 80% for mode selection.
Internal Power Rails

- **PLDO**: $V_{IN}$ to 2.4 V, for analog blocks.
- **1/2X SC**: $V_{IN}$ to $V_{SC} = 1/2V_{IN}$, for $S_1$ driving, no need for bootstrap capacitor.
- **NLDO**: $V_{SC}$ to 1V, for digital block and $S_2$ and $S_4$ driving.
Ramp Generator with Specific Duty Ratio

- $V_{H2X} = 0.2V_{DD}$ and $V_{L2X} = 0.4V_{DD}$, so $D$ of clk_20 and clk_40 is 20% and 40%.
Ramp Generator with Specific Duty Ratio

- \( V_{H2X} = 0.2V_{DD} \) and \( V_{L2X} = 0.4V_{DD} \), so \( D \) of \( \text{clk}_20 \) and \( \text{clk}_40 \) is 20% and 40%.
Outline

- Background and Motivation
- Proposed CPL-Buck Converter with Reduced Inductor Current
  - Topology and Working Principle
  - Conduction Loss Reduction
  - $V_{\text{OUT}}$ Drop Due to DCR and Switch On-Resistances
- Circuit Implementation
- Measurement Results
- Conclusions
Chip Micrograph and PCB

- 65 nm CMOS process.
- Die area: 2.72 mm$^2$.
- $C_{F1}$ and $C_{F2}$: 4.7 μF, soldered on-die, 1.0×0.5×0.5 mm$^3$.
- L: 470 nH, 1.6×0.8×0.8 mm$^3$.
- $C_{OUT}$: 10 μF, 1.6×0.8×0.8 mm$^3$.
- Working frequency: 2 MHz.
Measured Steady State Waveforms

\[ V_{IN}=4.2\text{V}, \quad V_{OUT}=1\text{V}, \quad I_{OUT}=1.2\text{A}, \quad \text{Sub-1/3X Mode} \]

- \[ V_{F1}: 2\text{V/div} \]
- \[ V_{F3}: 1\text{V/div} \]
- \[ V_{F4}: 1\text{V/div} \]
- \[ I_{L}: 500\text{mA/div} \]
- \[ I_{L\_AVG}=570\text{mA} \]

- 52.5% \( I_{L} \) reduction

\[ V_{IN}=3\text{V}, \quad V_{OUT}=1\text{V}, \quad I_{OUT}=1.2\text{A}, \quad \text{Sub-1/2X Mode} \]

- \[ V_{F1}: 2\text{V/div} \]
- \[ V_{F3}: 1\text{V/div} \]
- \[ V_{F4}: 1\text{V/div} \]
- \[ I_{L}: 500\text{mA/div} \]
- \[ I_{L\_AVG}=730\text{mA} \]

- 39.2% \( I_{L} \) reduction

\[ V_{IN}=3\text{V}, \quad V_{OUT}=1\text{V}, \quad I_{OUT}=1.2\text{A}, \quad \text{Sub-1/2X Mode} \]
Load Transient and Reference Tracking

Vin = 4.2V, Vout = 1V

Vout = 50mV

Vout = 40mV

Iout = 0.2A

1.2A

25 µs

Edge time: 1 µs

Vin = 4.2V, Iout = 0.6A

Vout = 1V

0.8V

Vref = 50 µs

Vref = 50 µs

ICAC 2022
92.9% peak efficiency at $V_{IN}=3V$, $V_{OUT}=0.8V$ and $I_{OUT}=0.4A$.

Sub-1/3X mode shows higher efficiency than sub-1/2X mode.
Efficiency and Current Density

High Efficiency & High Current Density

ISSCC 2017, Hybrid Dickson SC
CICC 2020, 5L FCML
ISSCC 2021, Hybrid Cascade SC
VLSI 2021, ADP
JSSC 2020, SMML
This work

[1] VCR=0.193
[2] VCR=0.218
[3] VCR=0.262
[4] VCR=0.240
[7] VCR=0.244
This work VCR=0.238
## Performance Summary and Comparison

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65 nm</td>
<td>180nm</td>
<td>180nm</td>
<td>180nm</td>
<td>180nm</td>
<td>65nm</td>
</tr>
<tr>
<td>Topology</td>
<td>Hybrid Dickson SC</td>
<td>5-level FCML</td>
<td>SMML</td>
<td>Hybrid Cascaded SC</td>
<td>ADP</td>
<td>CPL-Buck</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>3-4.5V</td>
<td>5.5V</td>
<td>3-5V</td>
<td>4-6V</td>
<td>3.4-4.5V</td>
<td>3-4.2V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>0.3-1V</td>
<td>0.4-1.2V</td>
<td>0.3-1.2V</td>
<td>0.4-1.2V</td>
<td>0.3-1.7V</td>
<td>0.6-1V</td>
</tr>
<tr>
<td>Output Current</td>
<td>1.53A</td>
<td>1.4A</td>
<td>2.5A</td>
<td>1A</td>
<td>1.6A</td>
<td>1.2A</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>0.2-5MHz</td>
<td>N.A.</td>
<td>5MHz</td>
<td>N.A.</td>
<td>1MHz</td>
<td>2MHz</td>
</tr>
<tr>
<td>Inductor</td>
<td>180nH</td>
<td>240nH</td>
<td>220nH</td>
<td>240nH</td>
<td>4.7μH</td>
<td>470nH</td>
</tr>
<tr>
<td>Inductor Size</td>
<td>4mm²</td>
<td>2×1.6mm²</td>
<td>5mm²</td>
<td>2×1.6mm²</td>
<td>4mm³</td>
<td>1.6×0.8×0.8mm³</td>
</tr>
<tr>
<td>Flying Cap.</td>
<td>3×22μF</td>
<td>3×4.7μF</td>
<td>4×1μF</td>
<td>2×4.7μF</td>
<td>2×10μF</td>
<td>2×4.7μF</td>
</tr>
<tr>
<td>Output Cap.</td>
<td>22μF</td>
<td>10μF</td>
<td>1μF</td>
<td>14.1μF</td>
<td>10μF</td>
<td>10μF</td>
</tr>
<tr>
<td>Peak Eff. @Vout, @VCR</td>
<td>90 @0.81V, @0.193</td>
<td>90 @1.0V, @0.182</td>
<td>89 @1.0V, @0.222</td>
<td>95.1 @1.1V, @0.220</td>
<td>86.5 @1.1V, @0.244</td>
<td>92.9 @ 0.8V, @0.267</td>
</tr>
<tr>
<td>Total Area</td>
<td>9.56mm²</td>
<td>12.8mm²</td>
<td>10.5mm²</td>
<td>11.0mm²</td>
<td>9.08mm²</td>
<td>4.0mm²</td>
</tr>
<tr>
<td>Current Density</td>
<td>0.16 A/mm²</td>
<td>0.11 A/mm²</td>
<td>0.24 A/mm²</td>
<td>0.09 A/mm²</td>
<td>0.18 A/mm²</td>
<td>0.30 A/mm²</td>
</tr>
<tr>
<td>Inductor Current Reduction</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td>YES</td>
</tr>
</tbody>
</table>

**Inductor Current Reduction**

- NO
- YES

**Performance Summary and Comparison**

- Technology: 65 nm
- Topology: Hybrid Dickson SC
- Input Voltage: 3-4.5V
- Output Voltage: 0.3-1V
- Output Current: 1.53A
- Switching Frequency: 0.2-5MHz
- Inductor: 180nH
- Inductor Size: 4mm²
- Flying Cap.: 3×22μF
- Output Cap.: 22μF
- Peak Eff. @Vout, @VCR: 90 @0.81V, @0.193
- Total Area: 9.56mm²
- Current Density: 0.16 A/mm²
- Inductor Current Reduction: NO

*ICAC 2022*
Outline

- Background and Motivation
- Proposed CPL-Buck Converter with Reduced Inductor Current
  - Topology and Working Principle
  - Conduction Loss Reduction
  - $V_{OUT}$ Drop Due to DCR and Switch On- Resistances
- Circuit Implementation
- Measurement Results
- Conclusions
Conclusions

- Reduces $V_X$ swing by an in-series $C_{F_1}$, reduces $I_L$ by an in-parallel SC.
- A larger VCR range compared with the inductor-input topologies.
- Good performances in $I_L$ reduction and small $\Delta I_L$.
- Analyzed the $V_{OUT}$ drop due to the DCR and switch on-resistances.
- Obtained 92.9% peak efficiency, 0.3 A/mm$^2$ current density, using a $1.6 \times 0.8 \times 0.8$ mm$^3$ inductor.
Thank You for Your Attention!

Guigang CAI

June. 23rd, 2022