Fully Passive Noise-Shaping SAR ADC with 4× Passive Gain and 2nd-Order Mismatch Error Shaping

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Outline

- Introduction
- NS SAR with 4× Passive Gain
- 2nd-Order MES with Digital Prediction
- ADC Architecture and Measurement Results
- Conclusion

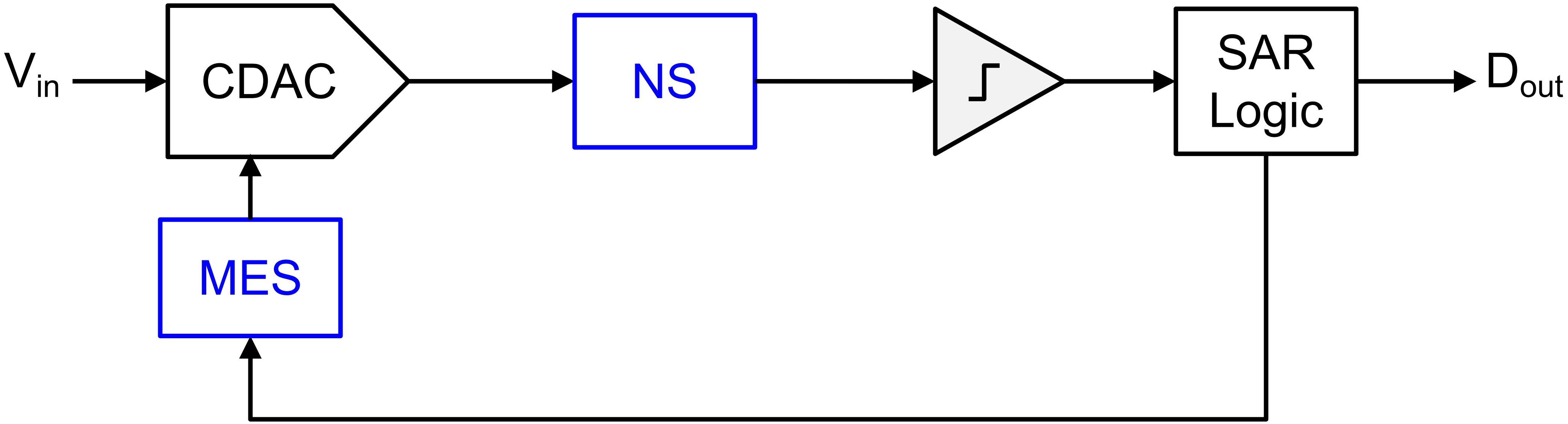
High-Resolution ADC Challenges

- To achive high resolution (e.g. >90dB SNDR)

- SAR ADC
  - Scaling friendly ☺
  - Excellent power efficiency with medium resolution ☺
  - Comparator noise: 4× power increase for 6dB noise reduction ☹
  - CDAC mismatch: need costly calibration ☹
- ΔΣ ADC
  - Suppress comparator noise by noise shaping ☺
  - Address CDAC mismatch by DWA ☺
  - Need power hungry OTAs ☹
  - Unfriendly to advanced process ☹

Proposed Solution

- Enable high resolution (>90dB SNDR)
- Maintian scaling friendliness, high power efficiency and PVT robustness
  - –Comparator noise → Fully passive noise shaping (NS) SAR ★
  - –CDAC mismatch → 2nd-order mismatch error shaping (MES) ★



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- Introduction
- NS SAR with 4× Passive Gain
  - Review
  - Proposed NS SAR
  - Comparison
- 2nd-Order MES with Digital Prediction
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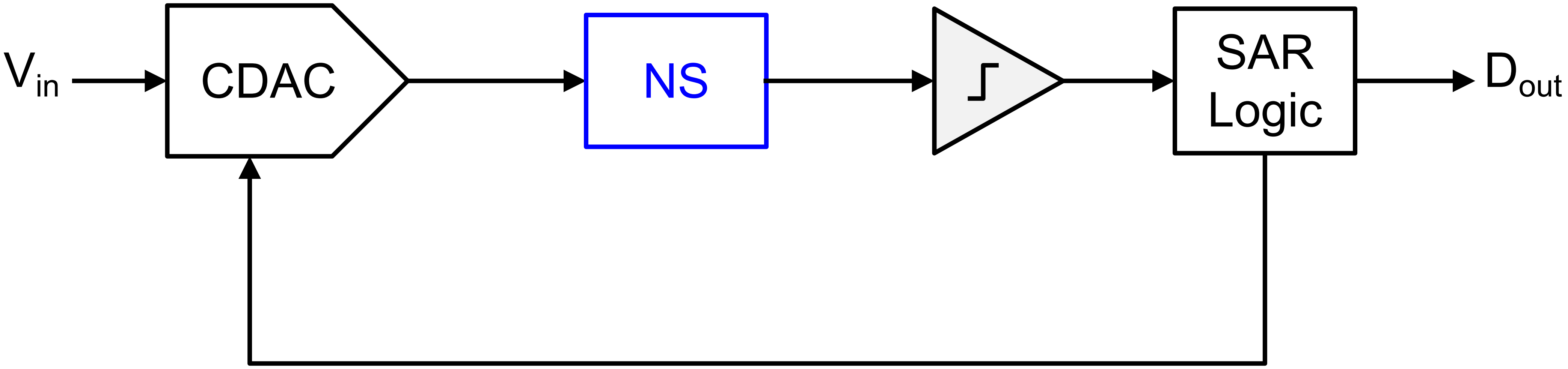
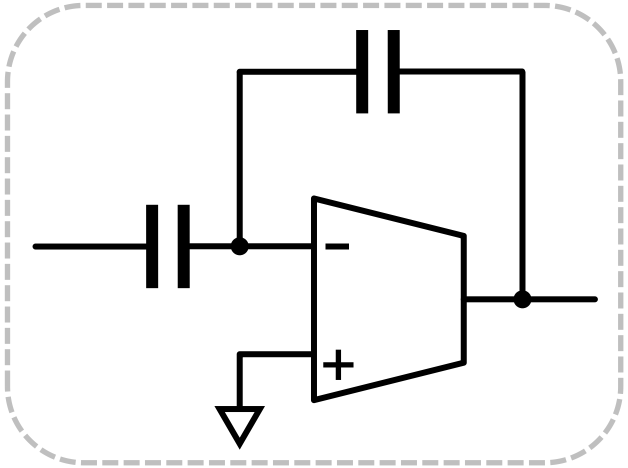
NS SAR ADC

- SAR + ΔΣ → low cost + high resolution
- Key is NS filter ★
  - Aggressive NS
  - Low power, low area, and robust



NS Filter Approaches

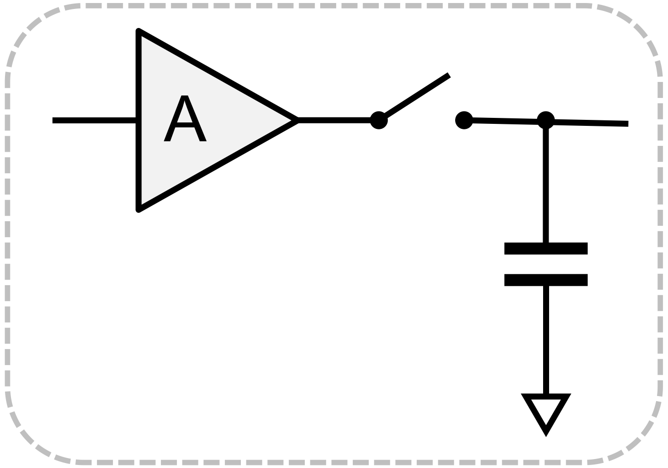
- OTA-based



[Fredenburg, ISSCC 2012]
[Shu, ISSCC 2016]
[Obata, VLSI 2016]

– Sharp NTF ☺
– PVT robust ☺
– High power ☹
– Scaling unfriendly ☹

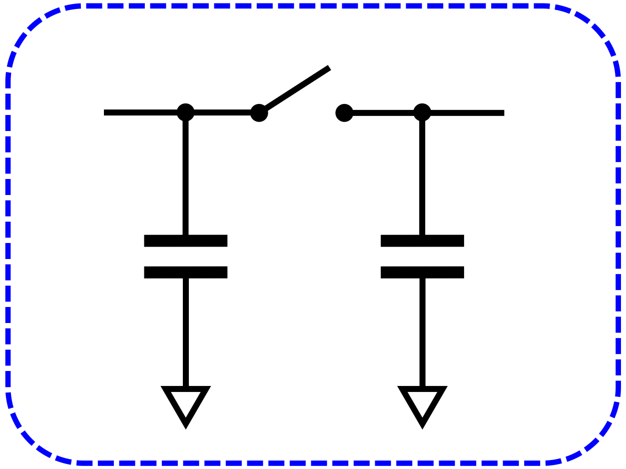
- DA-based



[Liu, ISSCC 2017]
[Miyahara, CICC 2017]
[Li, ISSCC 2018]

– Sharp NTF ☺
– Low power ☺
– Scaling friendly ☺
– PVT sensitive ☹

- Fully Passive

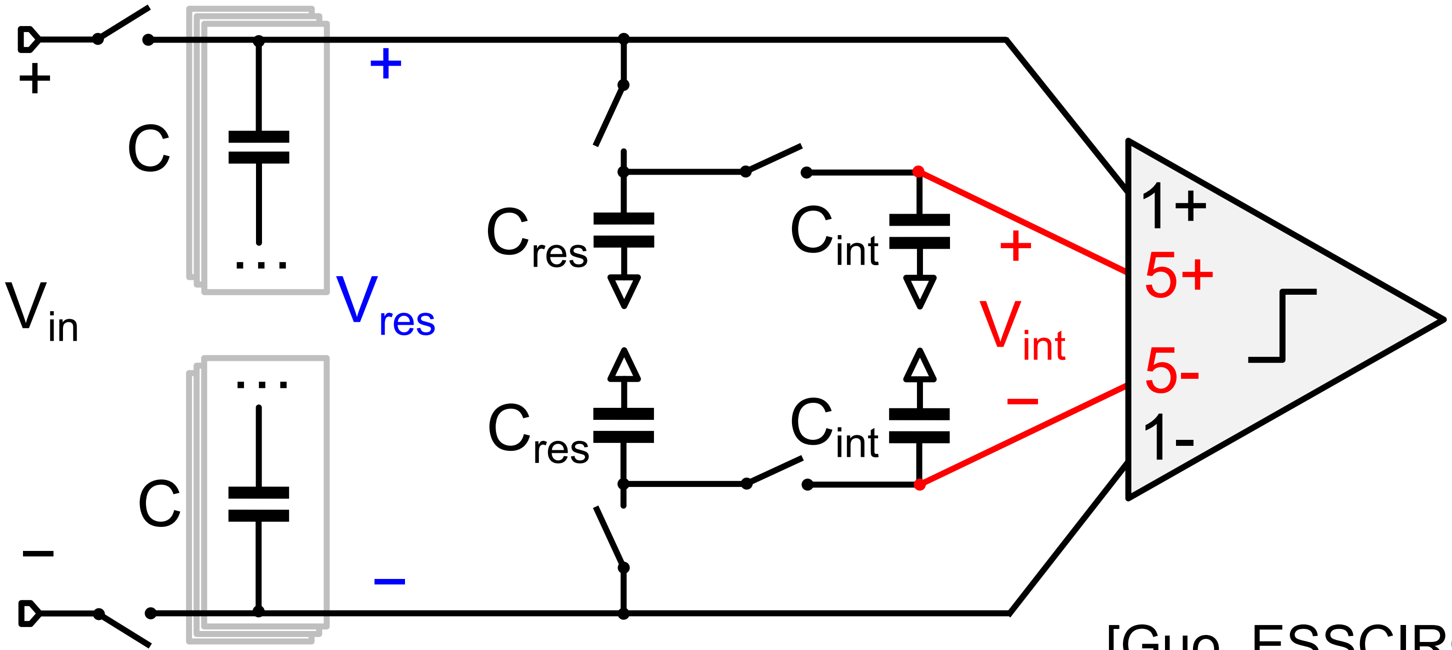


[Chen, VLSI 2015]
[Guo, ESSCIRC 2016]
[Lin, ISSCC 2019]

– Low power ☺
– PVT robust ☺
– Scaling friendly ☺
– Signal attenuation ☹

Prior Passive NS SAR #1

- Residue sampling
  - Small C_{res} (C/4) → Large kT/C noise (18.7kT/C) ☹
- Dynamic summation → need multi-input-pair comparator
  - 1:5 2-input pair comp. → 36× comparator input referred noise power ☹

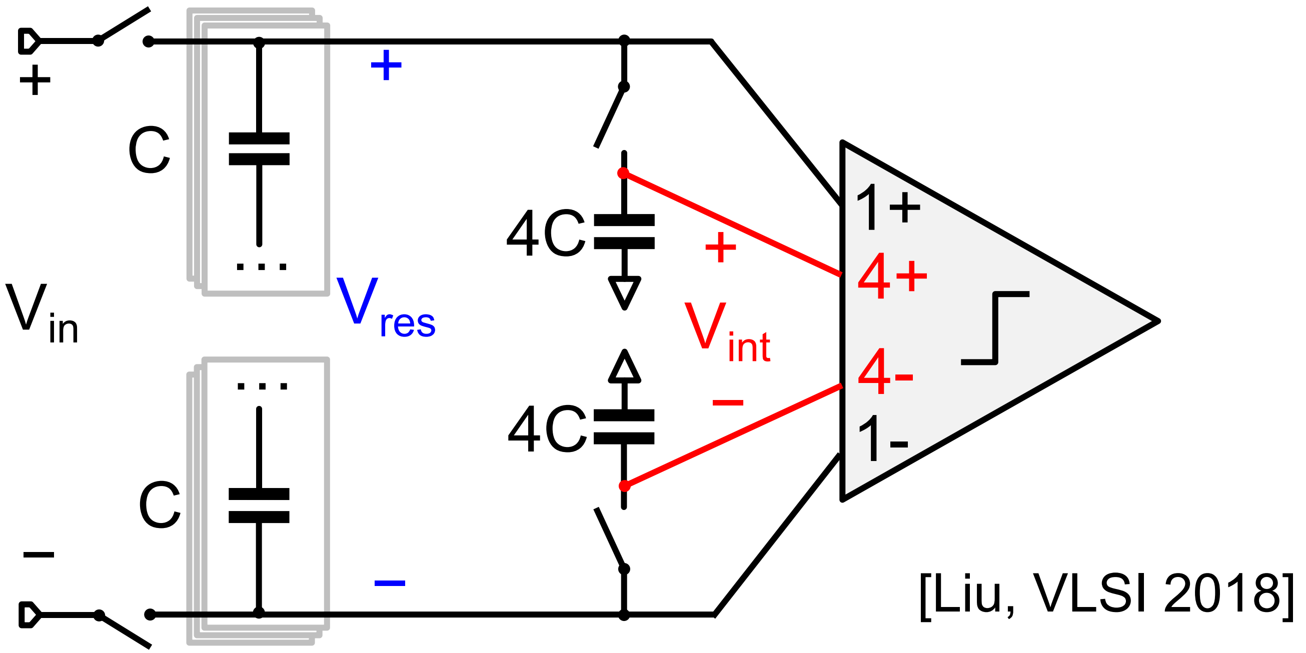


$$NTF = 1 - 0.8z^{-1}$$

[Guo, ESSCIRC 2016]

Prior Passive NS SAR #2

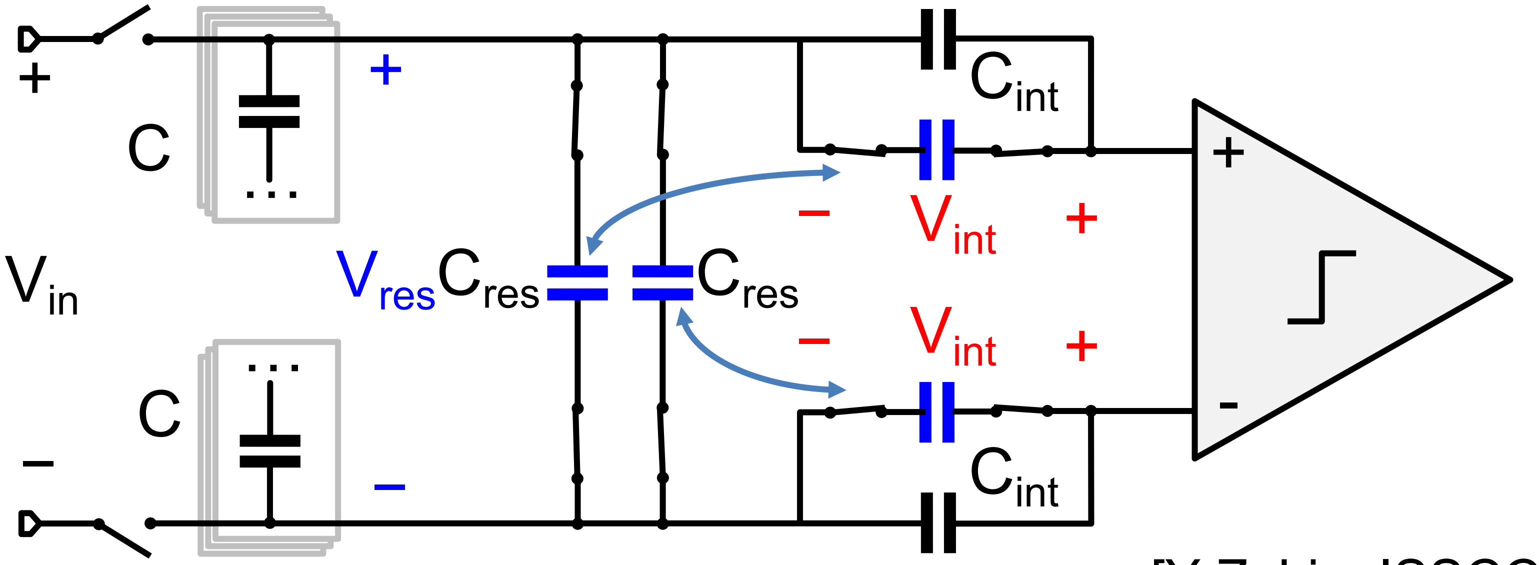
- Remove residue sampling
  - Reduced kT/C noise (3.6kT/C) ☺
- Dynamic summation → Need multi-input-pair comparator
  - 1:4 2-input pair comp. → 25× comparator input referred noise power ☹
  - Large integration cap. → 10C total cap. ☹



$$NTF = 1 - 0.8z^{-1}$$

Prior Passive NS SAR #3

- Passive summation and passive gain of 2
  - 1-input-pair comparator → reduced comparator input referred noise ☺
  - Mild NTF zero of z=0.5 ☹
- Extra residue sampling with Cres
  - Large kT/C noise (~20kT/C) ☹

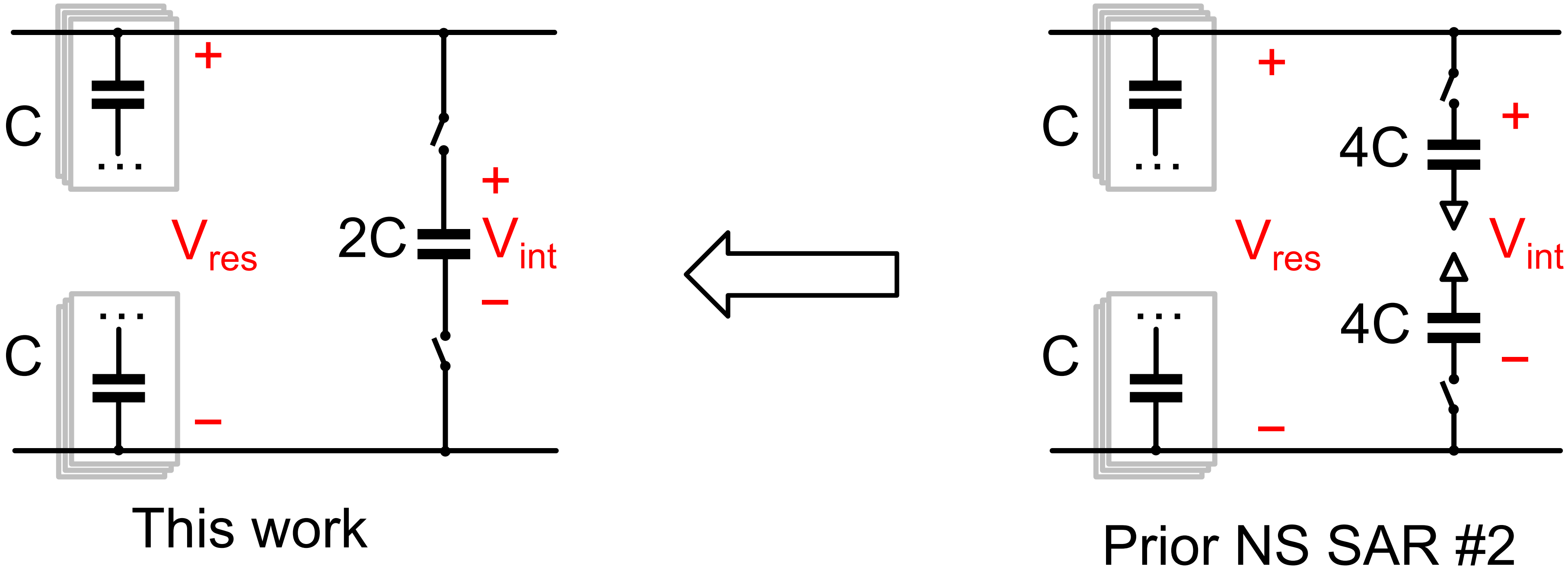


$$NTF = \frac{1-0.5z^{-1}}{1+0.5z^{-1}}$$

[Y.Z. Lin, ISSCC 2019]

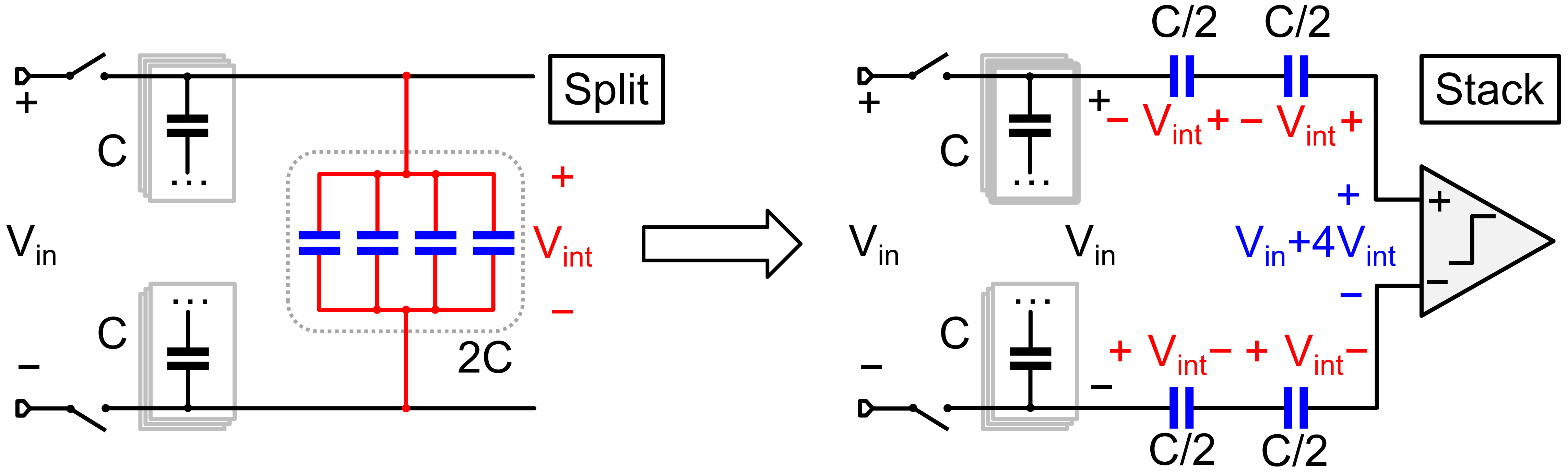
Proposed Passive NS SAR

- Remove residue sampling
  - Low kT/C noise, same with #2 ☺
- Differential integration instead of signle-ended integration
  - 4× reduction of total integration cap. ☺



Proposed Passive NS SAR

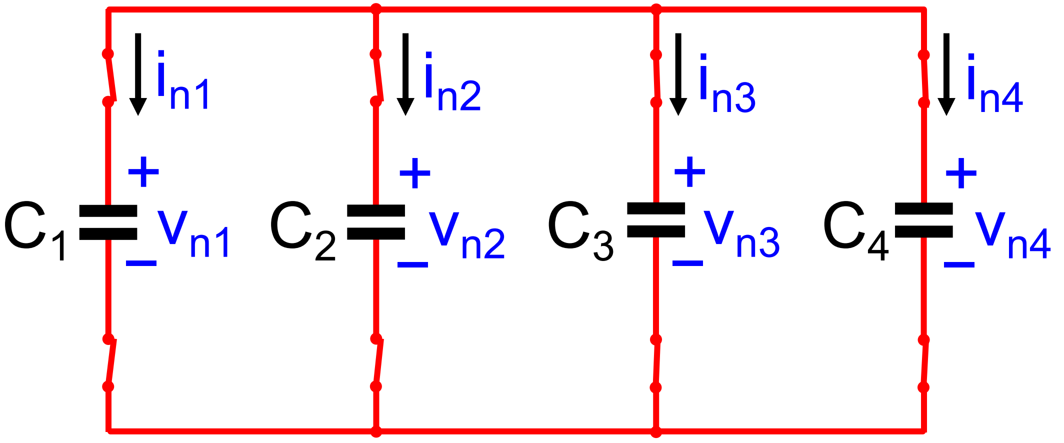
- Split and stack
  - 4× passive gain → NTF zero at 0.8 ☺
  - Passive summation → Only 1-input-pair comp. ☺

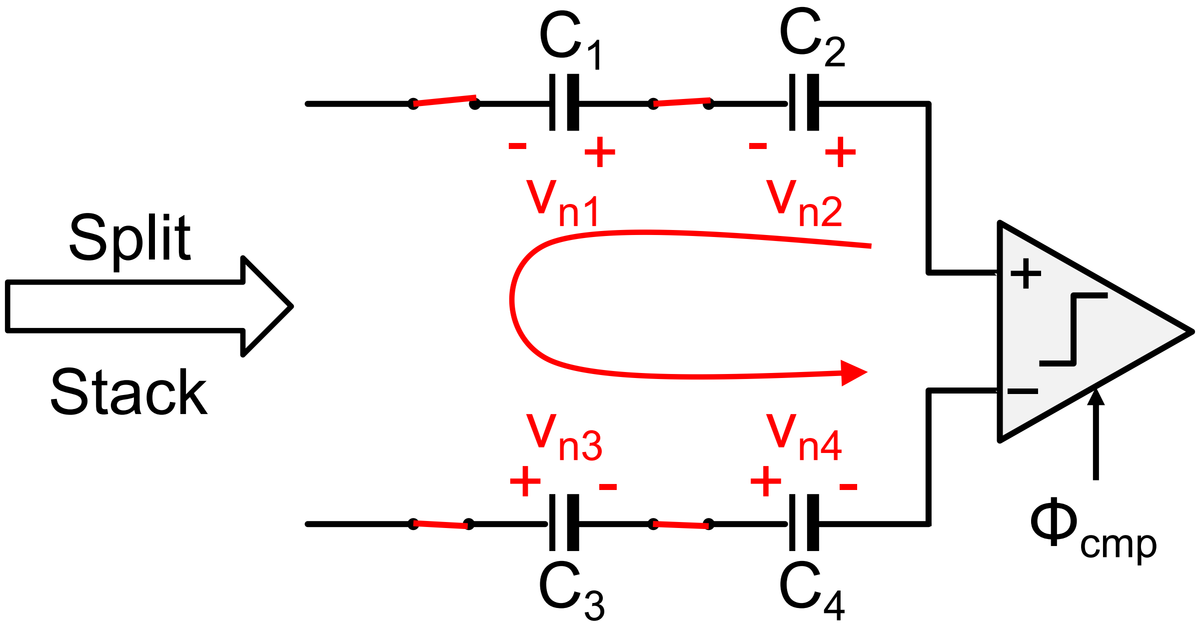


$$H(z) = \frac{0.2z^{-1}}{1-0.8z^{-1}}$$

$$L(z) = 1 + 4\cdot H(z) = \frac{1}{1-0.8z^{-1}}$$

kT/C Noise during Split-and-Stack





$$C_1 = C_2 = C_3 = C_4 = C/2$$

$$i_{n1} + i_{n2} + i_{n3} + i_{n4} = 0$$

$$C_1 \frac{dv_{n1}}{dt} + C_2 \frac{dv_{n2}}{dt} + C_3 \frac{dv_{n3}}{dt} + C_4 \frac{dv_{n4}}{dt} = 0$$

$$v_{n1} + v_{n2} + v_{n3} + v_{n4} = 0$$

- Split noises are cancelled out ☺

Comparison of Passive NS SAR Works

- For the same CDAC capacitor (C) and the same comp. power budget

	Total capacitor	Total kT/C noise	Passive gain	Multi-path comp.	Comp. input ref. noise	NTF zero location
Prior work #1	4.5C	18.7 kT/C	No	Yes	36x	0.8
Prior work #2	10C	3.6 kT/C	No	Yes	25x	0.8
Prior work #3	2.4C	20 kT/C	2	No	2.8x	0.5
This work	**4C**	**3.6 kT/C**	4	No	**1x**	0.8

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- NS SAR with 4× Passive Gain
- 2nd-Order MES with Digital Prediction
  - Prior 1st-order MES
  - Proposed 2nd-order MES
  - Digital prediction
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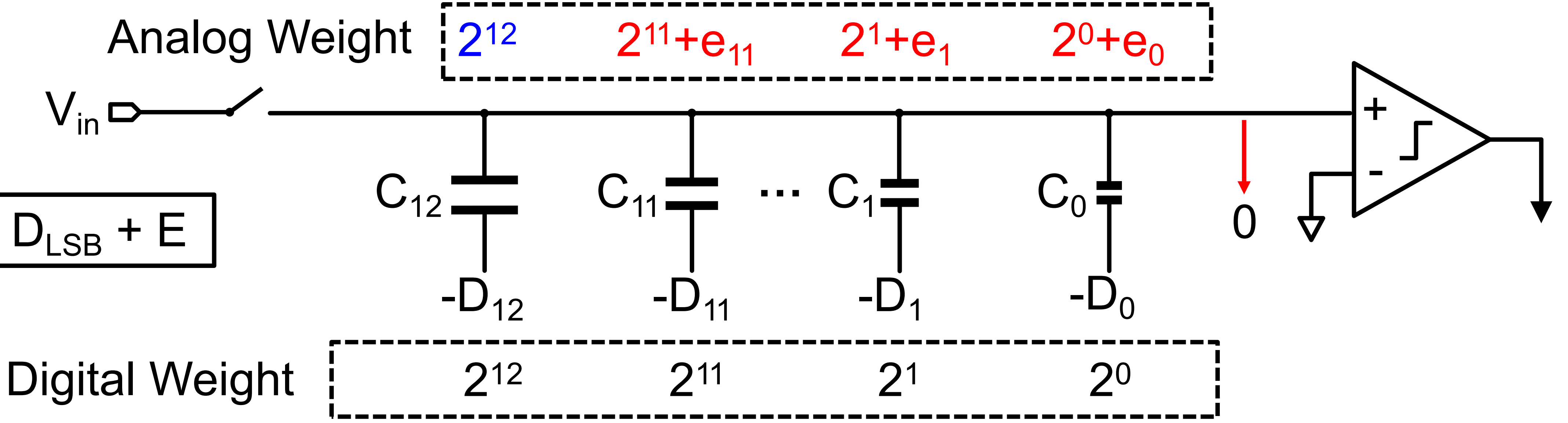
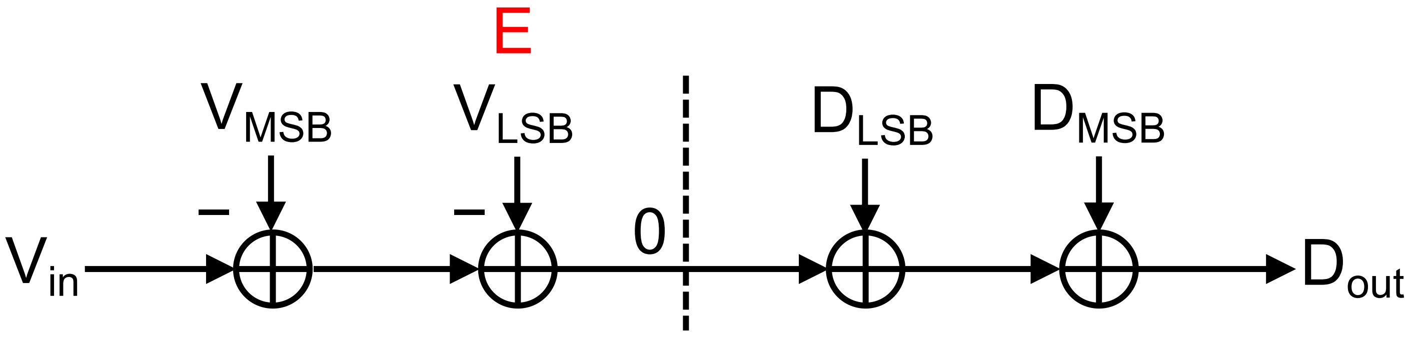
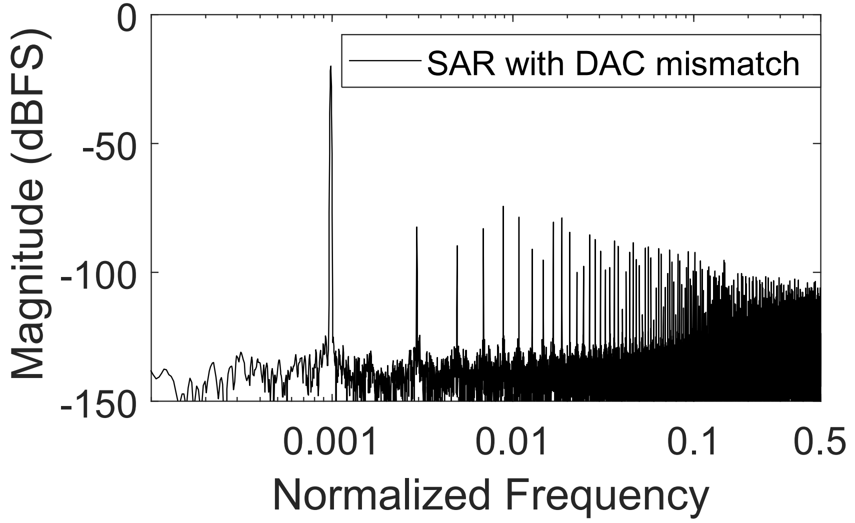
Capacitor Mismatch in SAR ADC



$V_{LSB} = D_{LSB} + E$

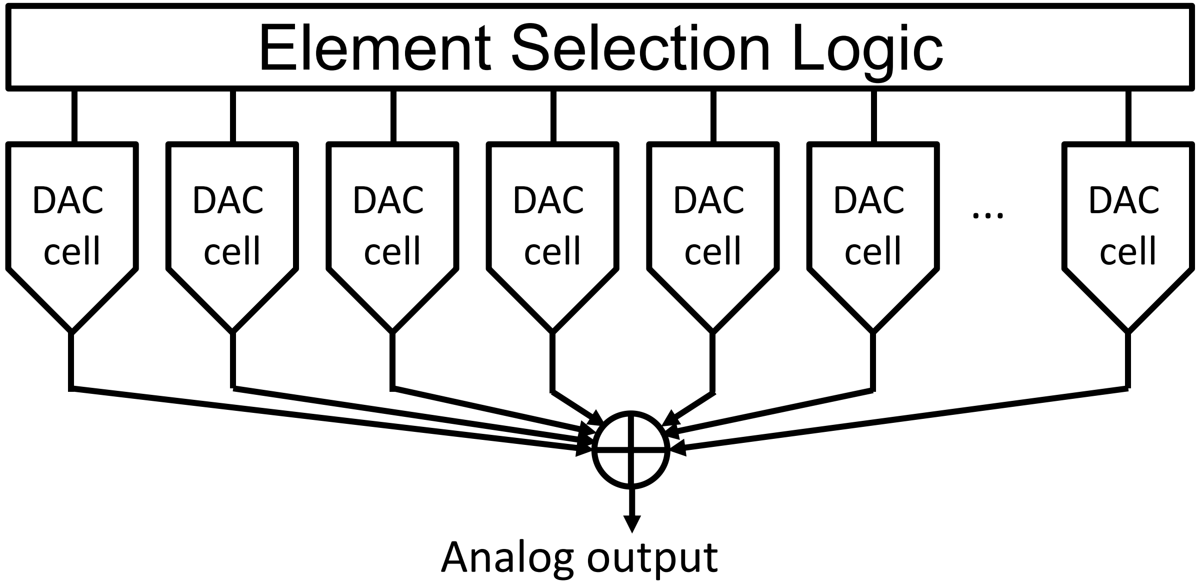


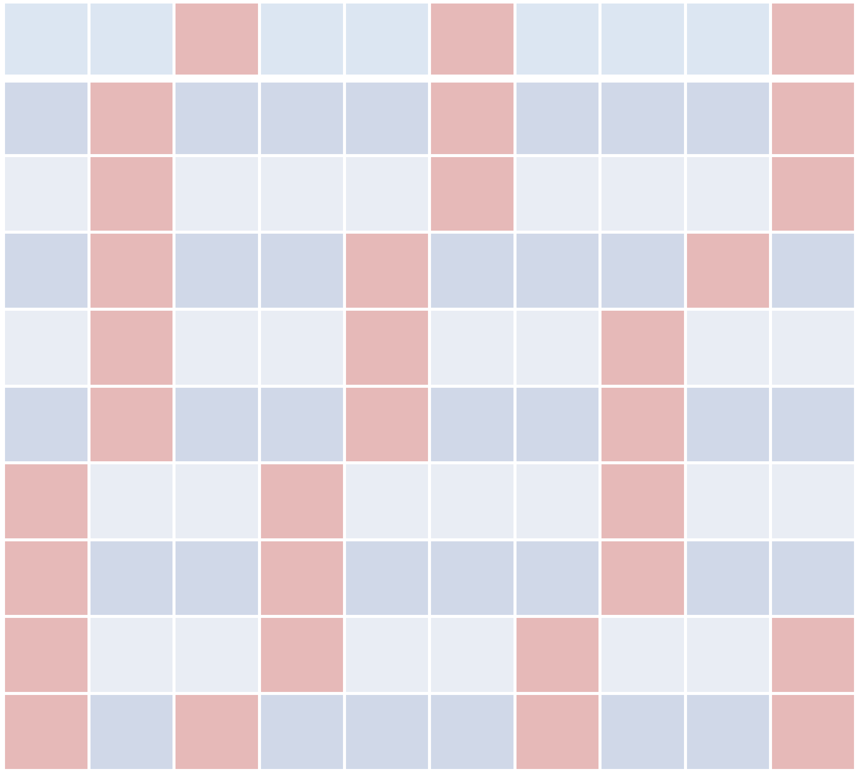
$D_{out} = V_{in} - E$



Classic DAC Mismatch Solution - DWA

- Usually used in ΔΣ ADCs
- Drawbacks:
  - Hardware cost grows exponentially with the number of bits
  - Usually applicable for <5-bit DACs

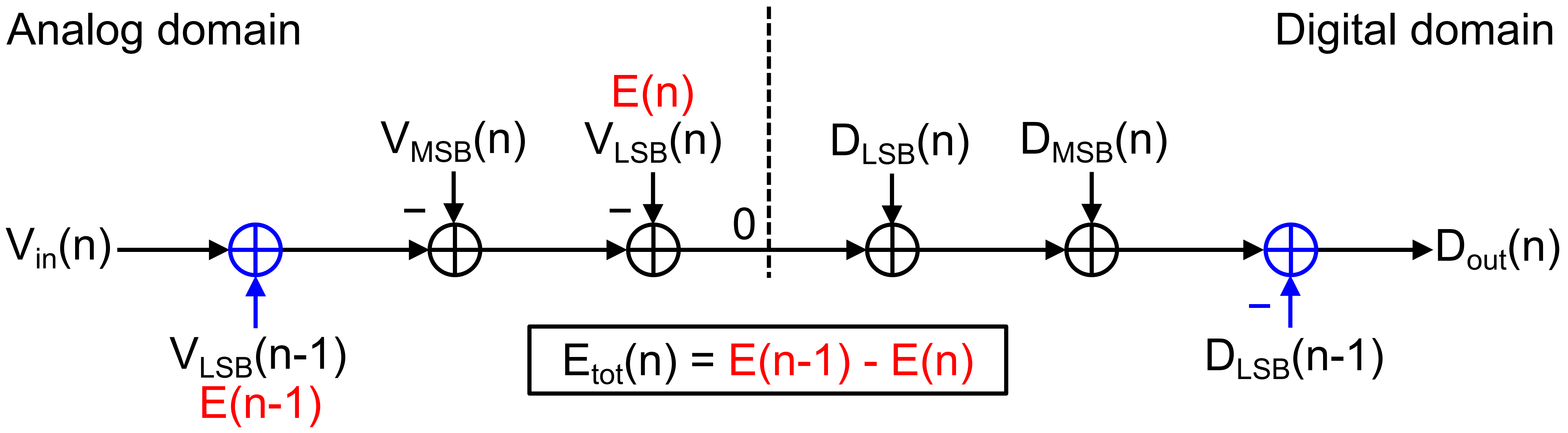




Capacitor uasge pattern of DWA

Feb. 2022 ISSCC Short Course

1^{st}-Order MES

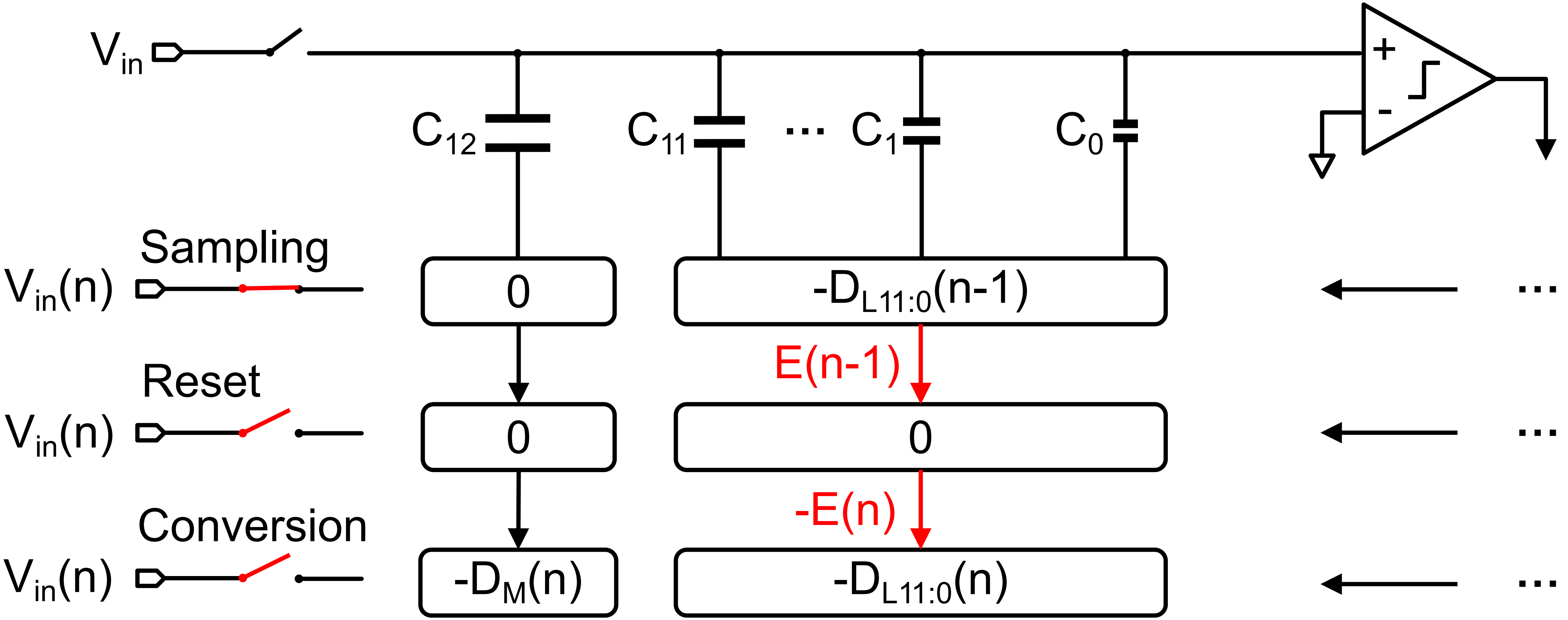


[Shu, ISSCC 2016]

- Operation principle
  - Feed back E(n-1) to the input

1^{st}-Order MES Implementation

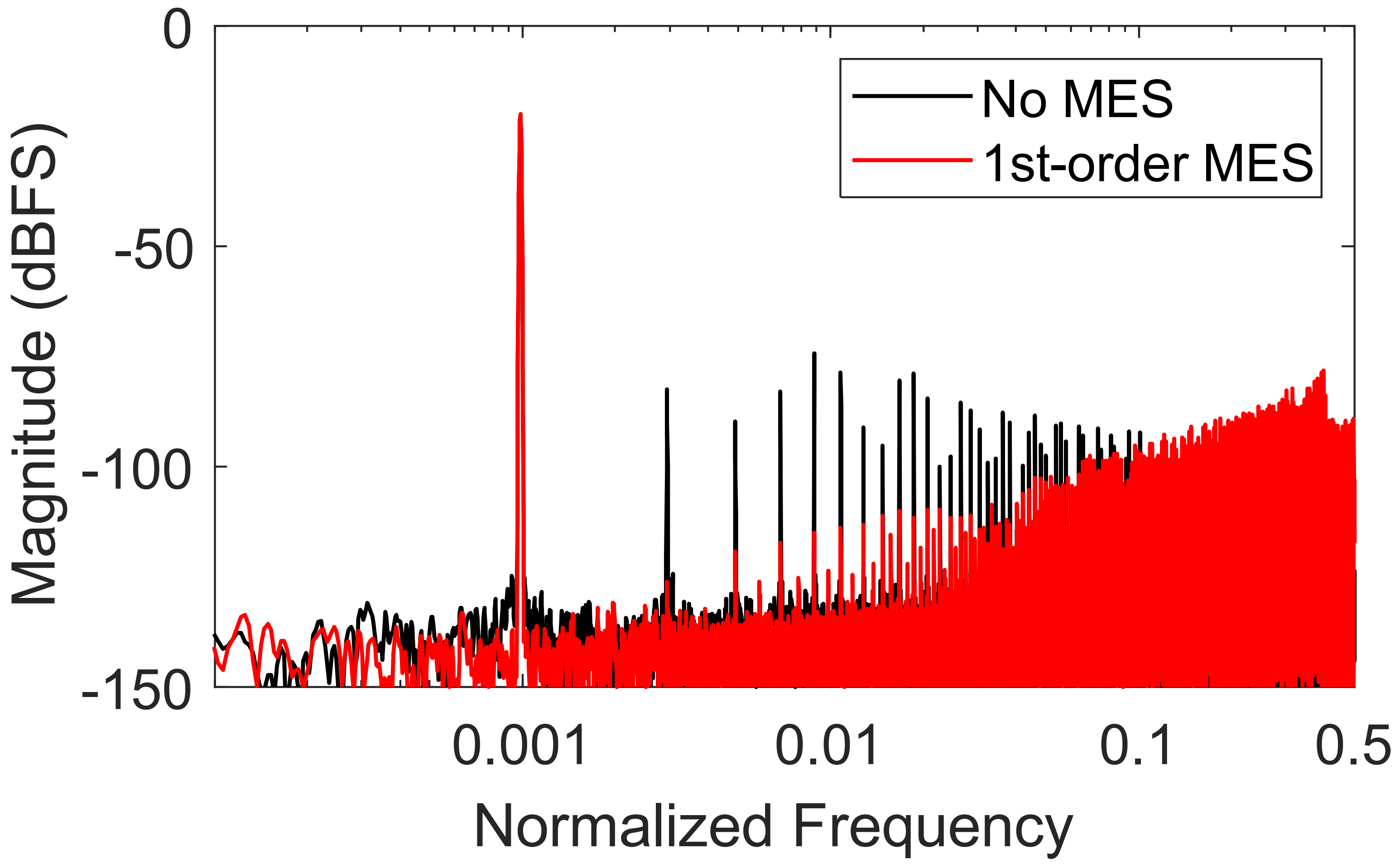
- Low hardware complexity, suit for high-bit DACs ☺



$$E_{tot}(n) = E(n-1) - E(n)$$

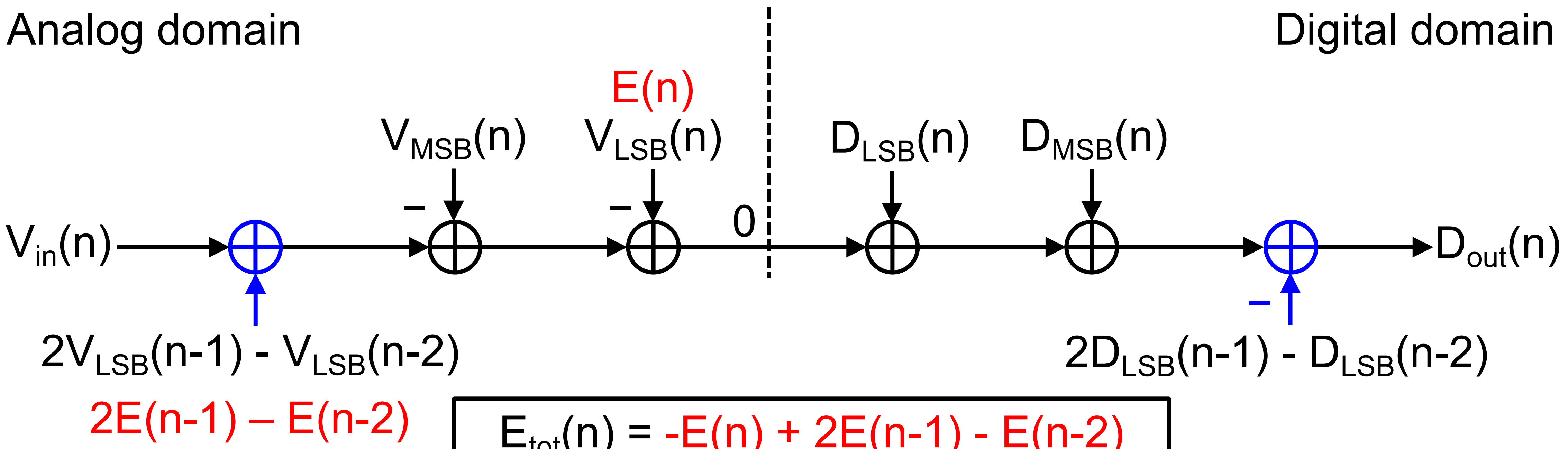
[Shu, ISSCC 2016]

1st-Order MES



- Reduce distortion ☺
- Signal-dependent tones ☹

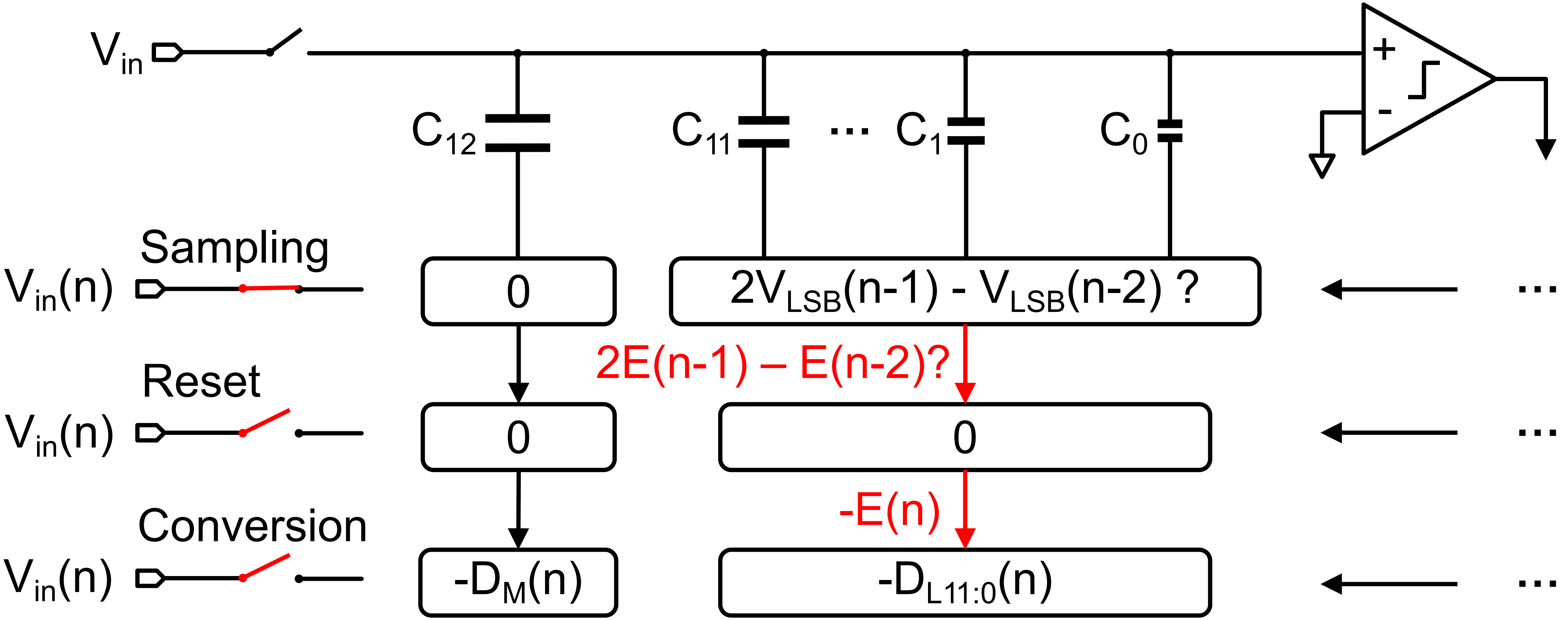
Extend MES to 2nd-Order



$$E_{tot}(n) = -E(n) + 2E(n-1) - E(n-2)$$

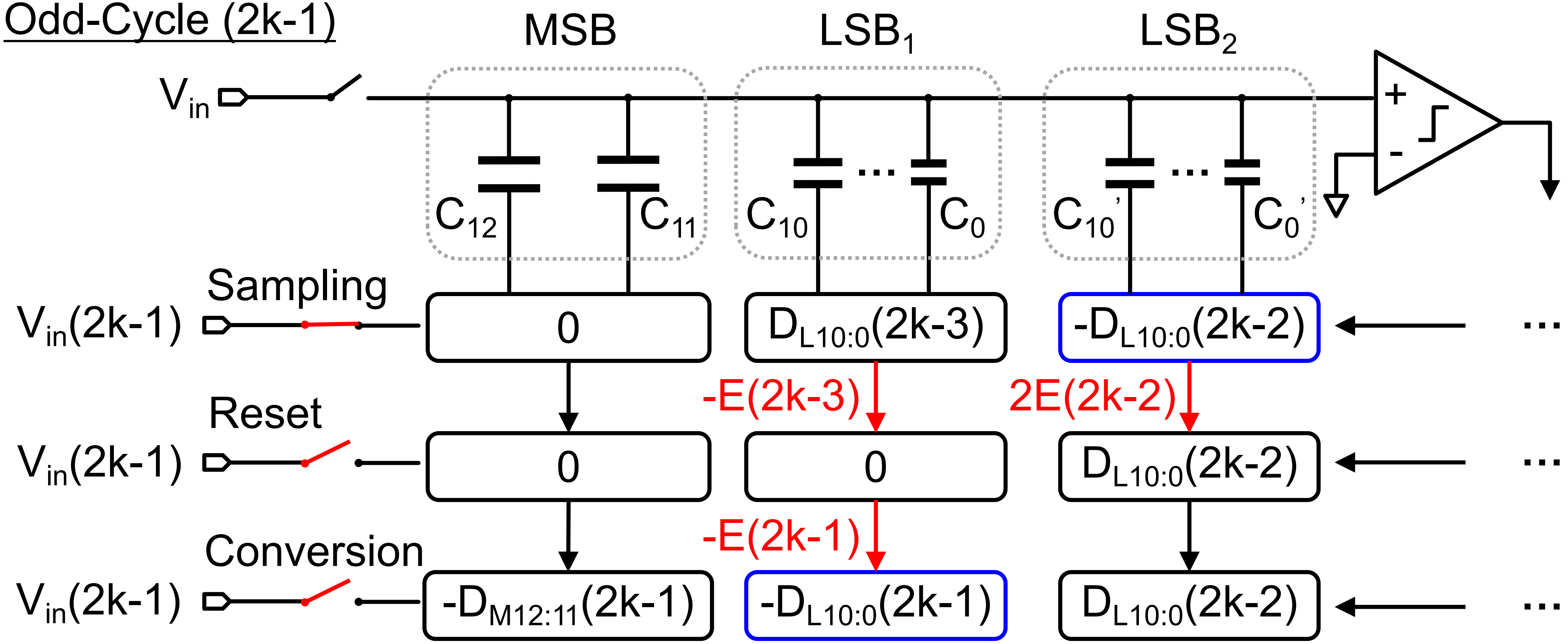
- Operation principle
  - Feed back 2E(n-1)-E(n-2) to the input

Try to Implement 2nd-Order MES



Proposed 2nd-Order MES Implementation

- Odd-Cycle (2k-1)

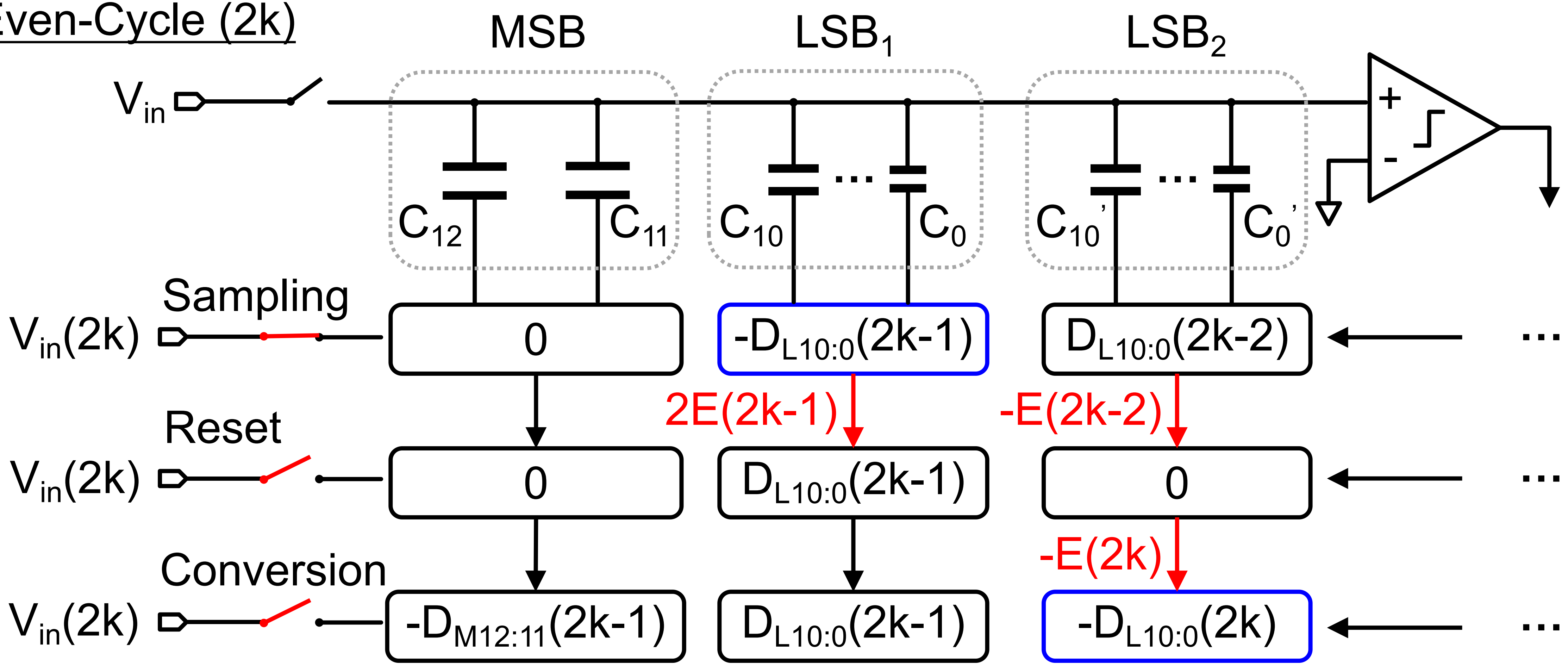


$$E_{tot}(2k-1) = -E(2k-1) + 2E(2k-2) - E(2k-3)$$

[Liu, ISSCC 2020]

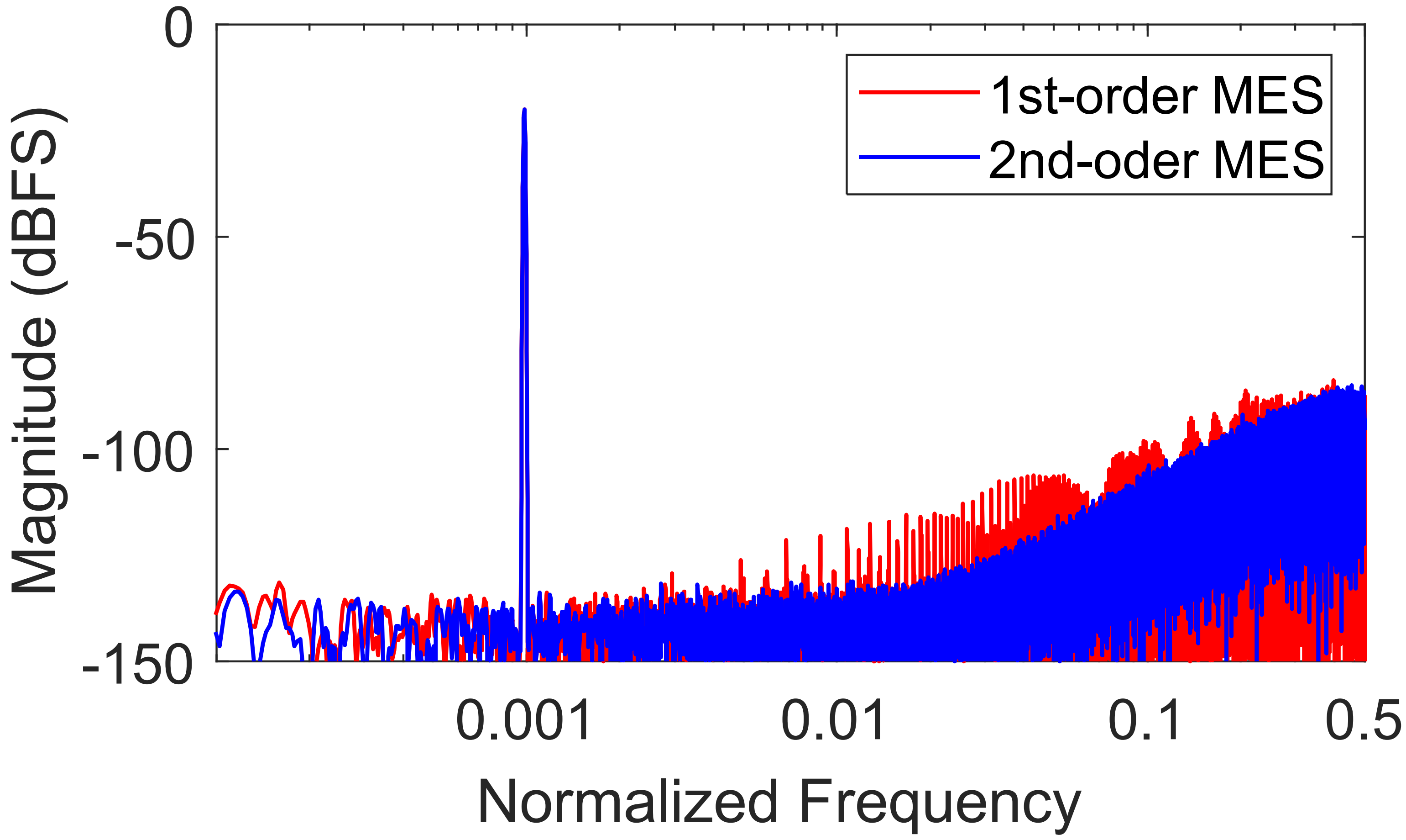
Proposed 2nd-Order MES Implementation

- Even-Cycle (2k)



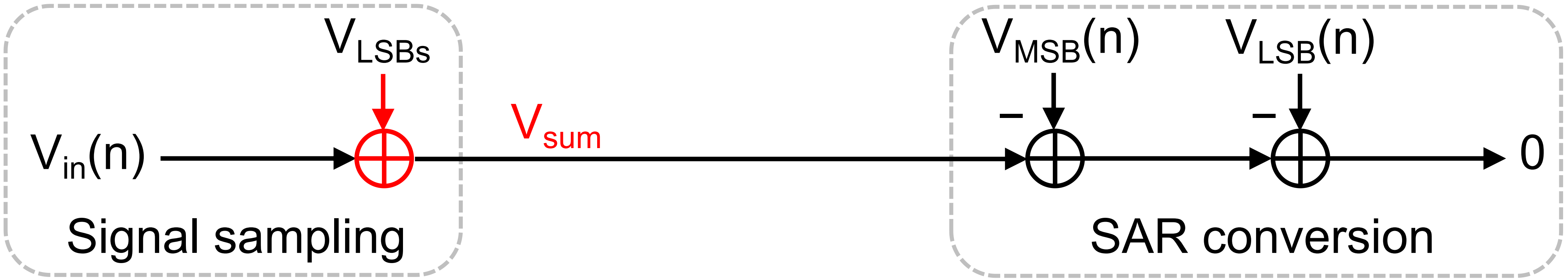
$$E_{tot}(2k) = -E(2k) + 2E(2k-1) - E(2k-2) \rightarrow E_{tot}(z) = -(1-z^{-1})^2 \cdot E(z)$$

Proposed 2nd-Order MES



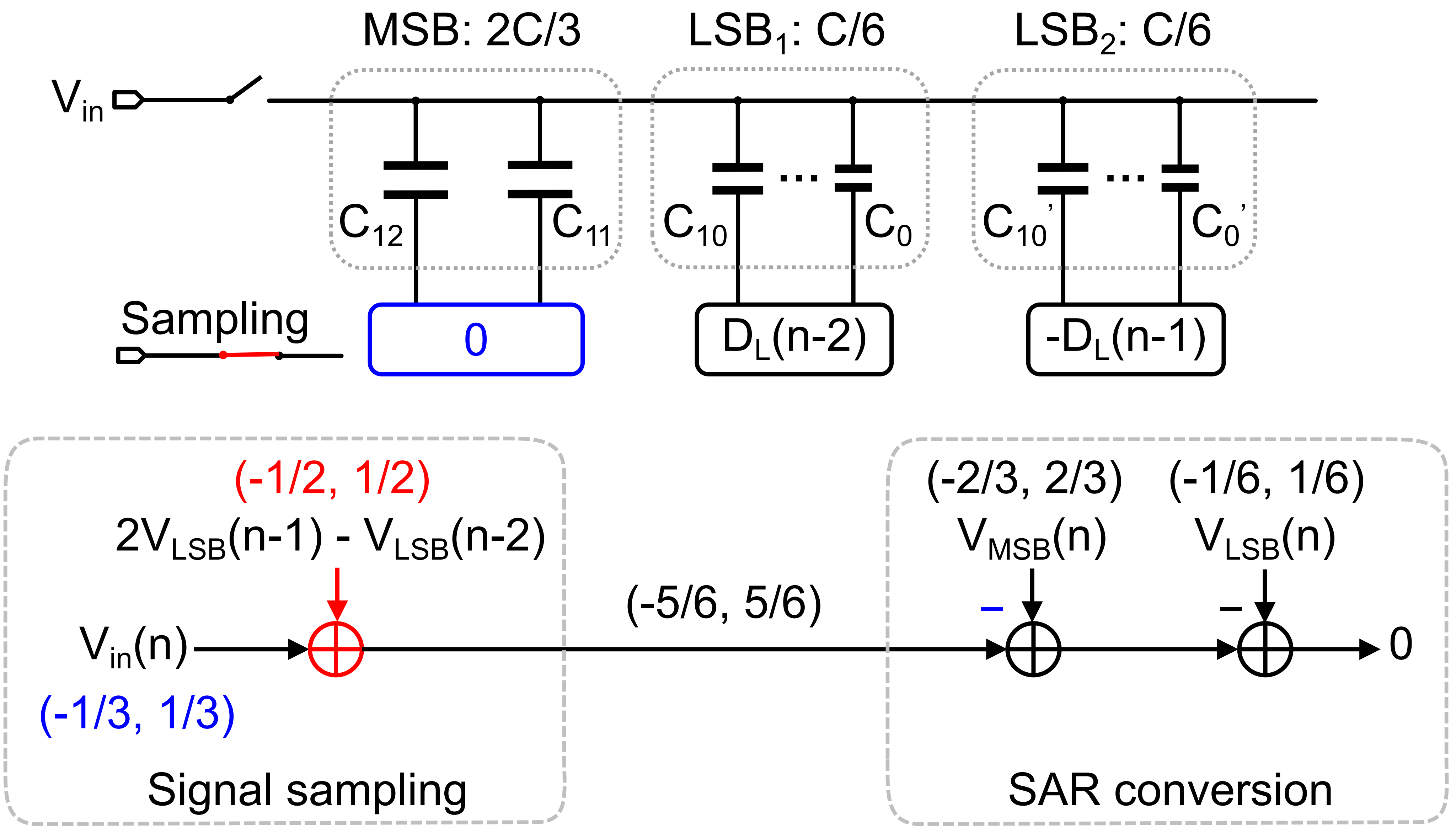
- 2nd-order shaping ☺
- Tone-free ☺

Signal Range Loss Caused by MES

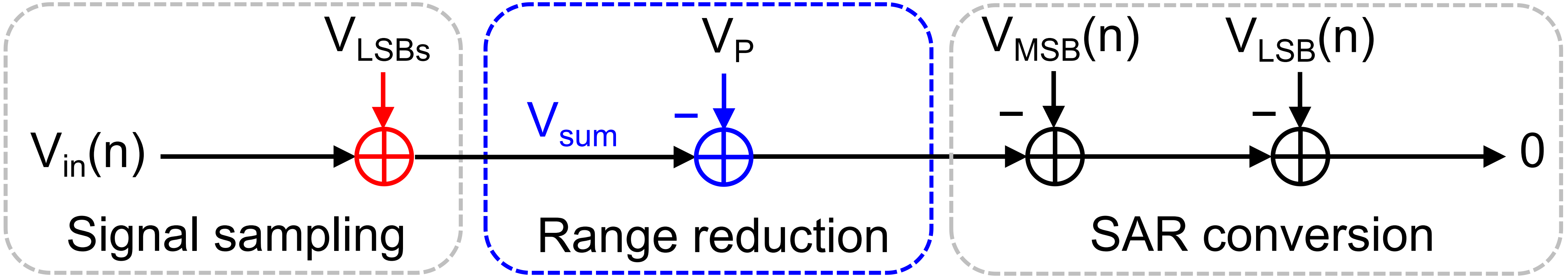


- Injected V_{LSBs} eats up input range

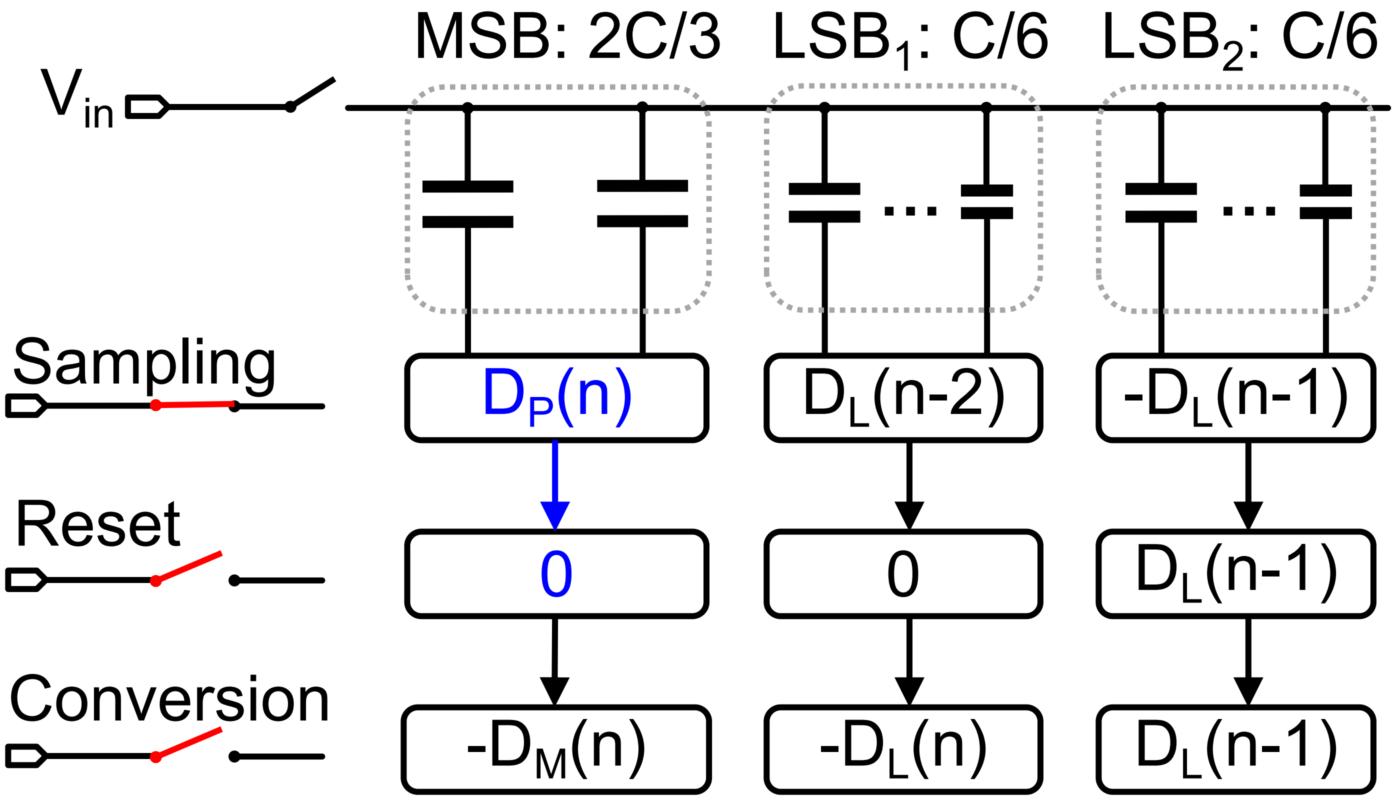
Allowable Input Signal Range



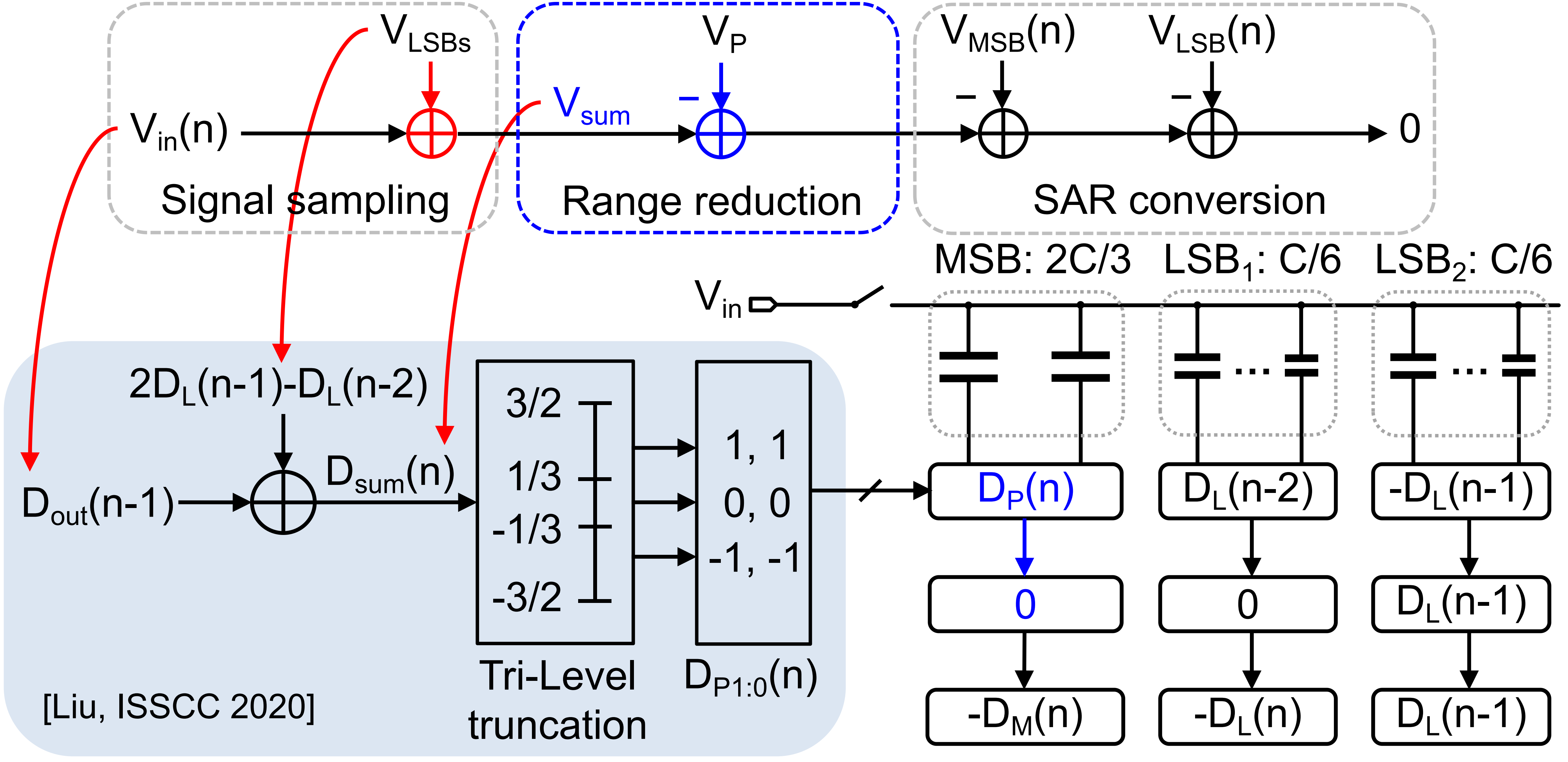
Recover Signal Range



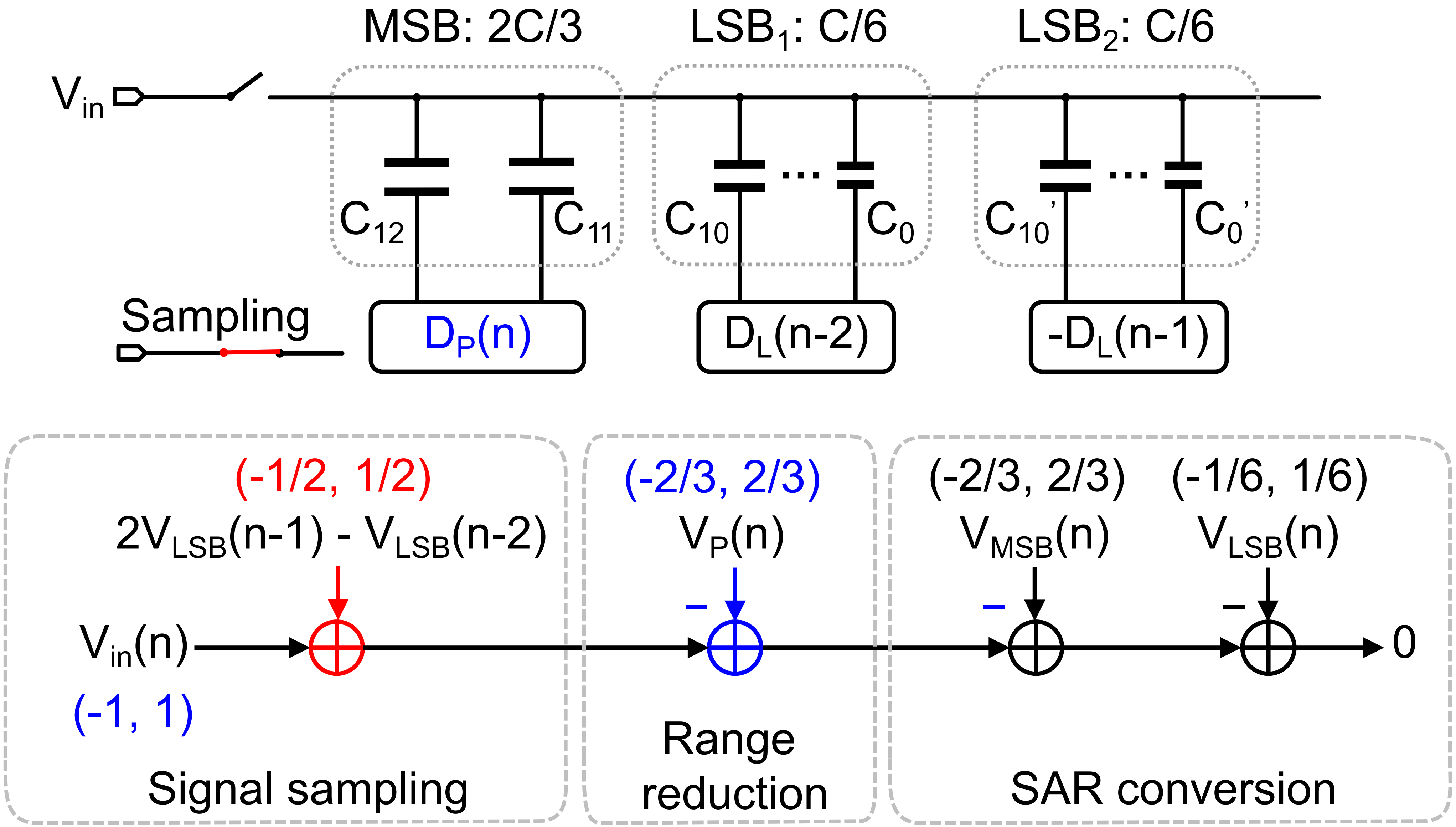
- Reduce V_{sum} by V_P
- V_P need to track V_{sum} ★



Digital Prediction



Allowable Input Signal Range with Prediction



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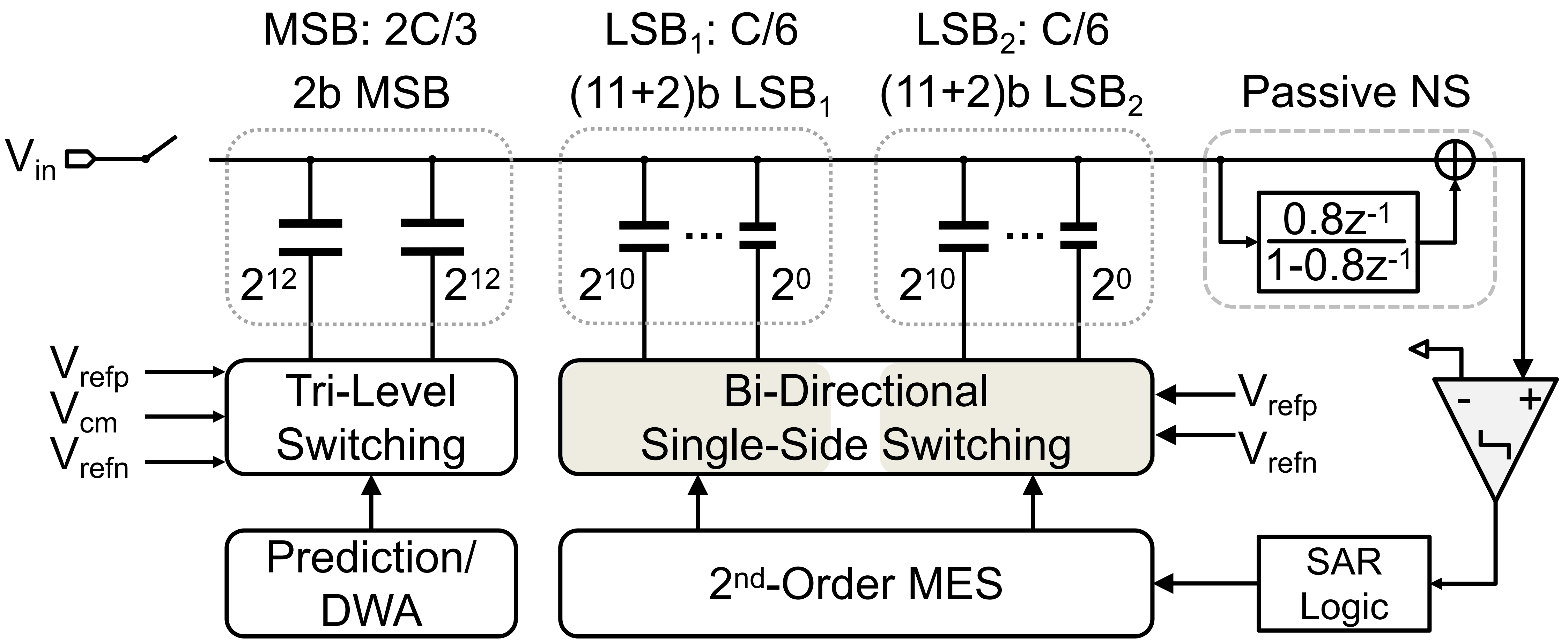
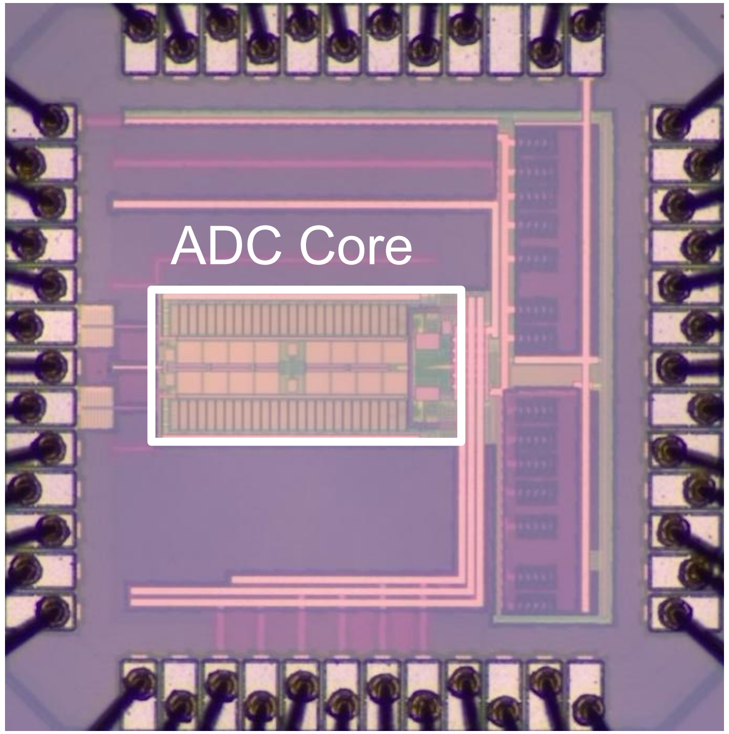
Overall ADC Architecture

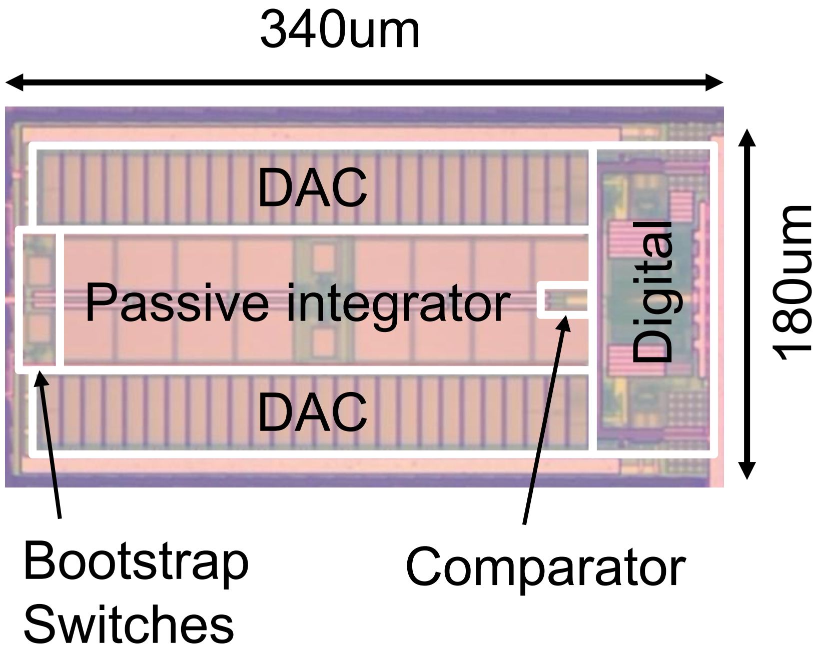


- Use DWA to average MSB cells
- Use 2b equally weighted MSB to simplify DWA

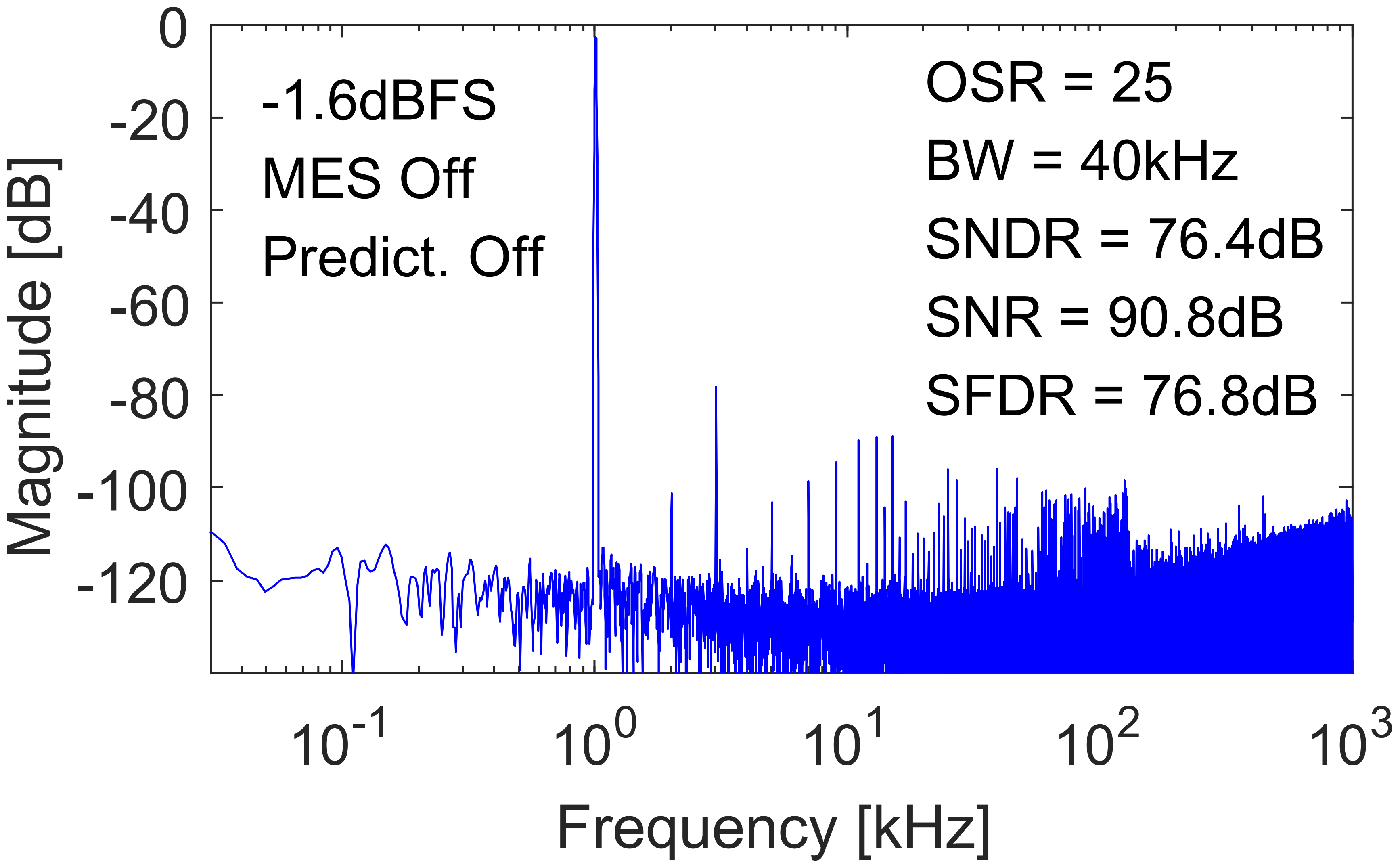
Die Photo

- 40nm LP CMOS
- 0.06mm² active area
- 67.4uW power

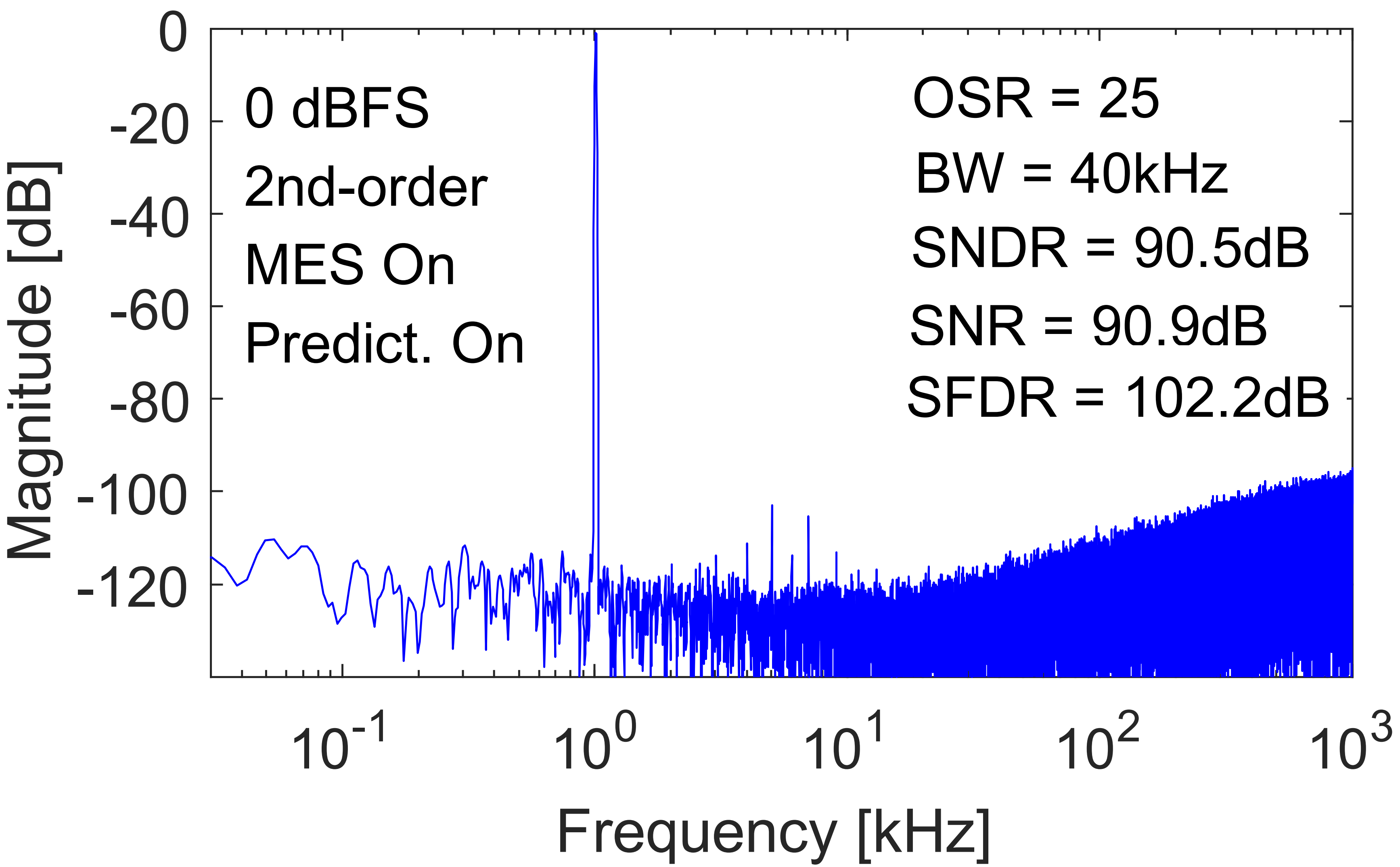




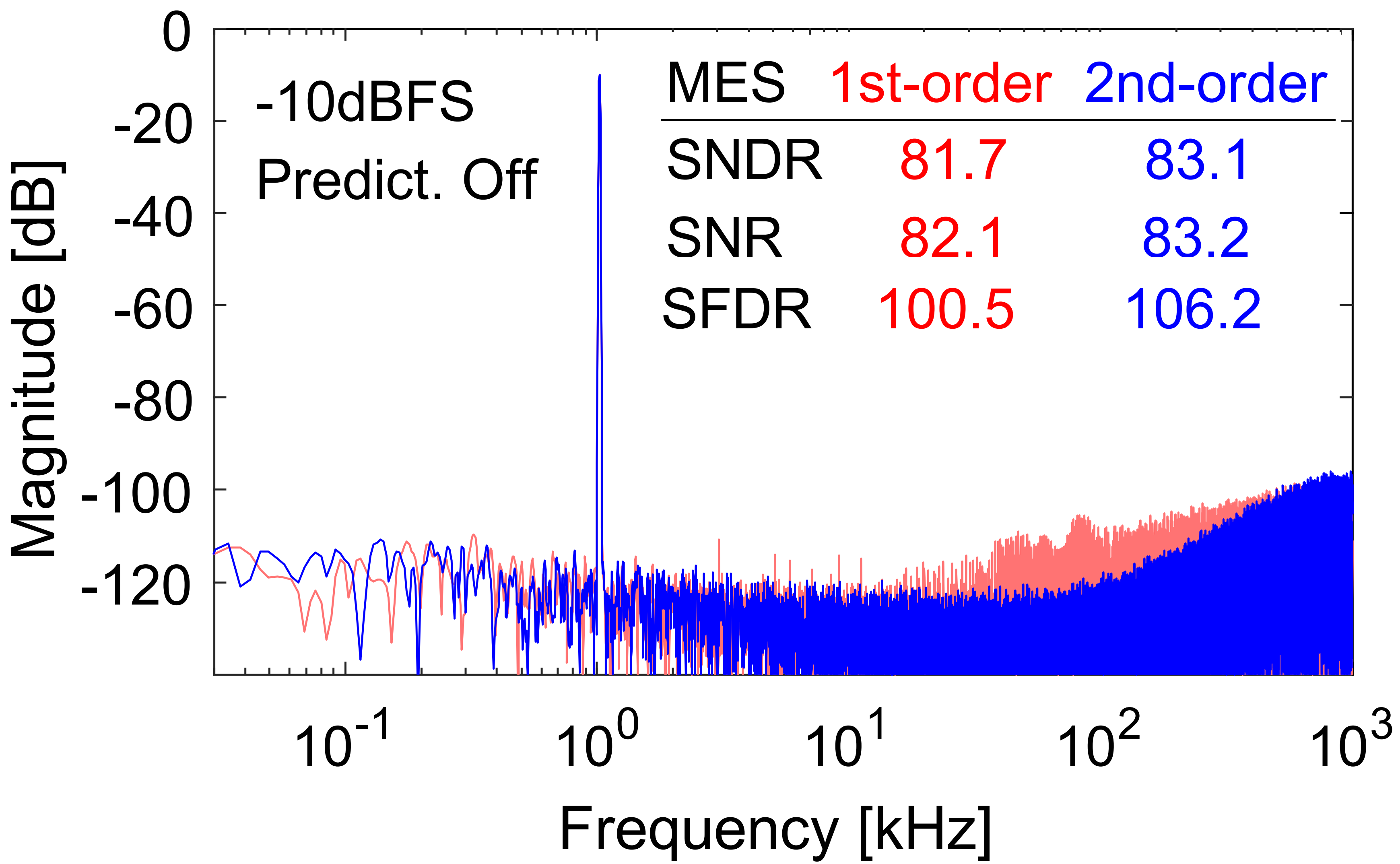
Measured Spectrum Before MES



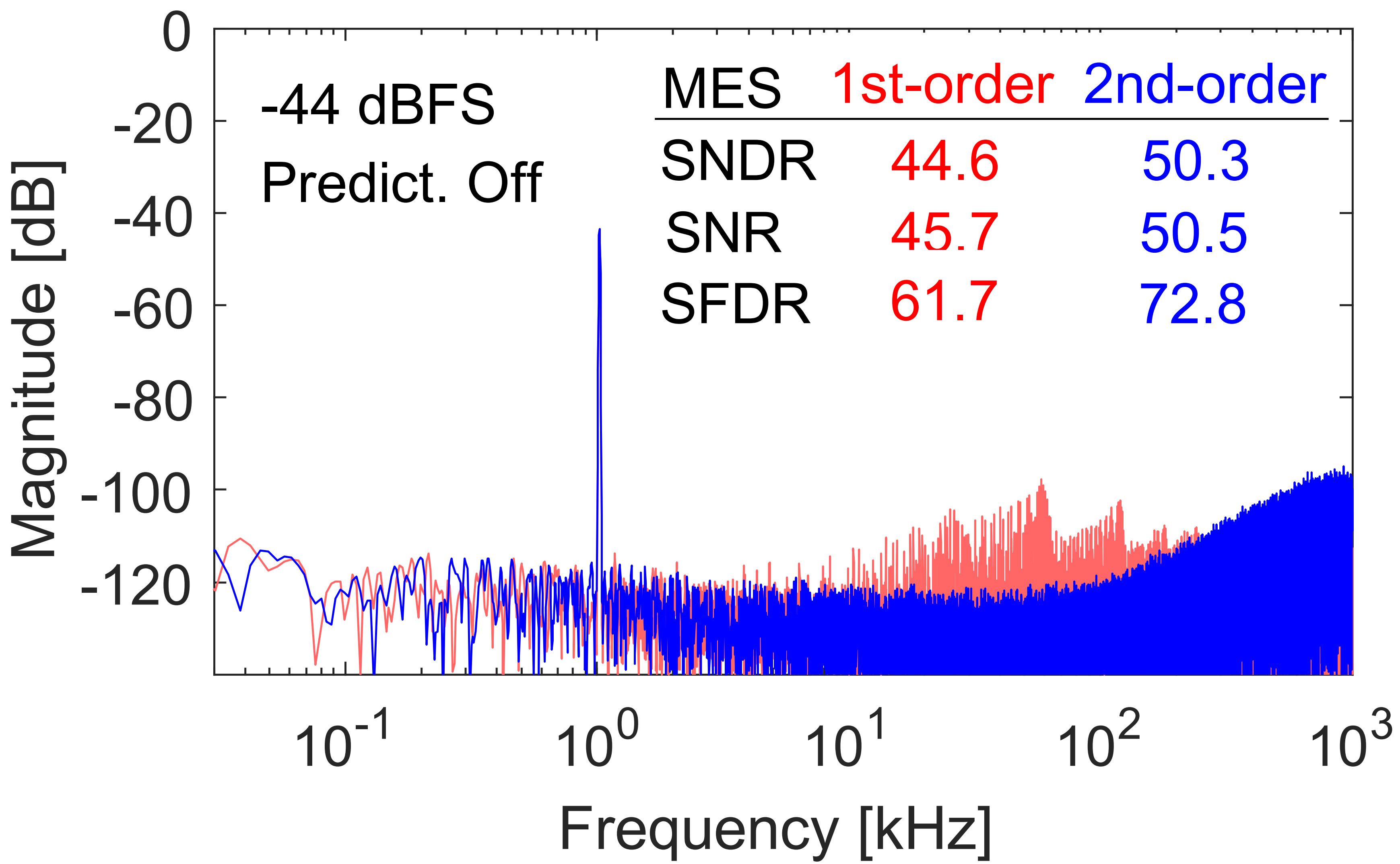
Measured Spectrum After 2^{nd}-Order MES



Comparison Between 1st- and 2nd-Order MES



Comparison Between 1st- and 2nd-Order MES



MES	1st-order	2nd-order
SNDR	44.6	50.3
SNR	45.7	50.5
SFDR	61.7	72.8

Performance Summary and Comparison

	This work		ISSCC 16 Shu [4]		ISSCC 17 Liu [3]	ISSCC 18 Li	ISSCC 19 Lin [2]
Process	**40nm**		55nm		28nm	40nm	14nm
Architecture	**Passive NS SAR**		Active NS SAR		DA-based NS SAR	DA-based NS SAR	Passive NS SAR
Fs (MS/s)	**2**		1		132	10	320
Power (uW)	**67.4**		15.7		460	84	1250
OSR	**25**	**100**	125	500	13.2	8	4
BW (kHz)	**40**	**10**	4	1	5000	625	40000
SFDR (dB)	**102.2**	**102.2**	105.1	105.1	92.6	89	77.4
SNDR (dB)	**90.5**	**95.3**	96.1	101	79.7	79	66.6
FoM_{SNDR} (dB)	**178.2**	**177**	180	178.9	180.1	178	171.7
FoM_{DR} (dB)	**182**	**180.2**	-	179.6	182.2	179.5	-

Conclusion

- **Fully Passive NS SAR ADC with 4× passive gain**
  - Reduced kT/C noise
  - Reduced comparator input referred noise
- **2nd-order MES with digital prediction**
  - Aggressive mismatch shaping capability
  - Support full-swing input signals
- **40nm CMOS ADC prototype**
  - Fully dynamic, PVT robust, calibration-free
  - Highest resolution among passive NS SARs

Thanks for your Attention!