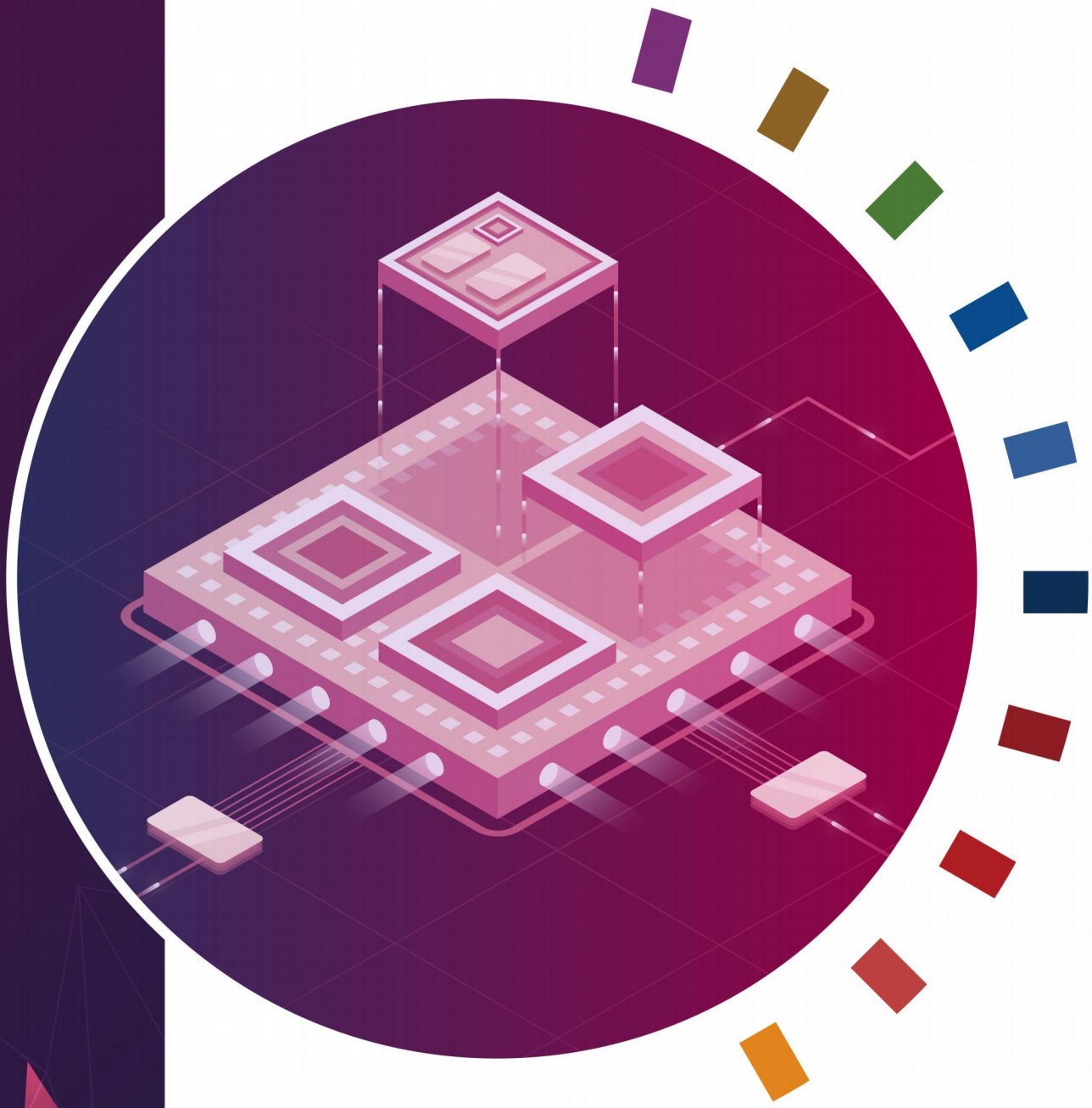
ICAC 2026

会议手册 PROGRAM WORKSHOP



华人芯片设计技术研讨会

WORKSHOP ON IC ADVANCES IN CHINA

中国 上海

2026/3/25-27

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ORGANIZERS & SPONSORS 主办及支持单位

主办单位

复旦大学　清华大学　北京大学　东南大学　澳门大学　汉堡工业大学　香港科技大学

承办单位

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双钻支持单位

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铂金支持单位

中兴微电子　纳芯微科技　硅芯科技　中星联华　义博信息　上海北芯

黄金支持单位

兆易创新　威智科技　速石科技　南京邮电大学南通研究院

CONFERENCE COMMITTEE 会议组委会

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涂锋斌，香港科技大学

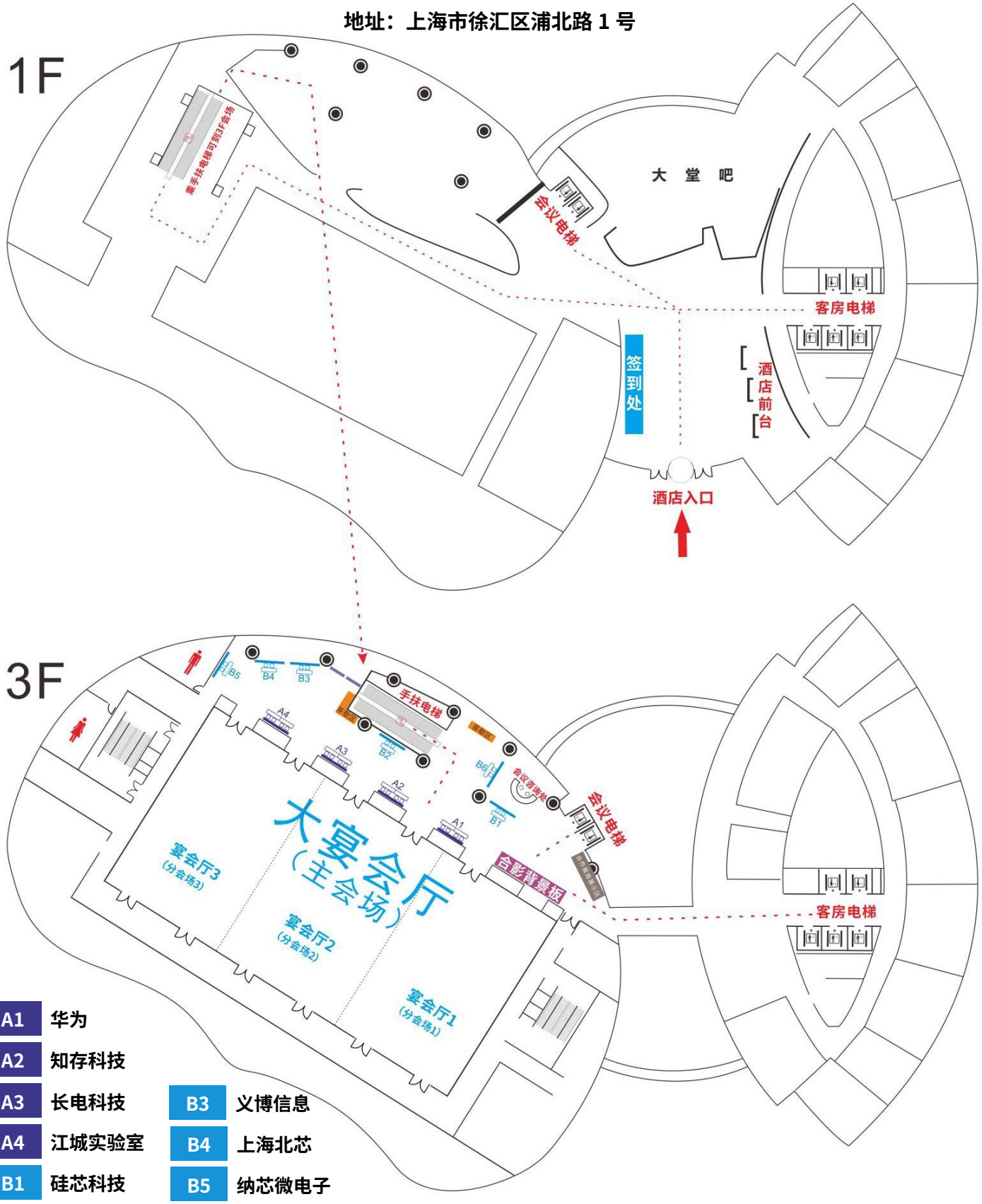
李家明，澳门大学

张奕涵，香港科技大学

CONFERENCE VENUE 会议地点

上海中星铂尔曼大酒店

地址：上海市徐汇区浦北路 1 号



A1	华为	B3	义博信息
A2	知存科技	B4	上海北芯
A3	长电科技	B5	纳芯微电子
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B2	中兴微电子		

PROGRAM AT A GLANCE 会议日程概览

2026 年 3 月 24 日 · 第 0 天		
10:00-20:00	会议签到及会议资料领取	1F 大堂

2026 年 3 月 25 日 · 第 1 天			
	宴会厅 1	宴会厅 2	宴会厅 3
	培训班 1 主持人：陈迟晓	**培训班 2** 主持人：揭路	**培训班 3** 主持人：路延
08:45-10:15	司　鑫	沈林晓	杜思俊
10:15-10:30 | 茶　歇			
	培训班 4 主持人：孙亚男	**培训班 5** 主持人：潘权	**培训班 6** 主持人：明鑫
10:30-12:00	贾天宇	贾海昆	屈万园
12:00-13:30 | 午 休			
	大宴会厅		
13:30-13:45	**ICAC 2026 开幕仪式 & ICAC 2025 最佳报告颁奖**		
13:45-14:15	**大会报告：洪志良，复旦大学** A 71.5-dB SNDR 475-MS/s Ringamp-Based Pipelined SAR ADC With On-Chip Bit-Weight Calibration		
14:15-14:45	**大会报告：任天令，清华大学** A Fully Flexible Compute-in-memory Chip for Edge Intelligence		
14:45-15:15 | 茶 歇			
	宴会厅 1	大宴会厅 2	宴会厅 3
	RF, mm-Wave and Photonic Circuits 主持人：贾海昆	**Precision Analog Interfaces and Sensors** 主持人：张奕涵	**AI Accelerators and DSA** 主持人：岳金山
15:15-15:40	俞　捷	明　鑫	赵　亮
15:40-16:05	李连鸣	沈林晓	张　川
16:05-16:30	毕晓君	李家明	杨　杰
16:30-16:55	耿新林	王　晶	贾天宇
16:55-17:20	王　辉	金　锦	陈卓俊
17:20-17:45	过悦康	余　超	赵元哲
18:00-19:00	合作展商宣传&欢迎冷餐会	/	/
19:00-21:00	/	/	学生海报展示

2026 年 3 月 26 日 · 第 2 天

	宴会厅 1	宴会厅 2	宴会厅 3
	Radar and RF Transceivers 主持人：胡诣哲	**Neuromorphic Processors and Security** 主持人：郭衍束	**Advanced ADC and DAC Architectures** 主持人：唐希源
08:30-08:55	张　慧	陈　虹	陈知行
08:55-09:20	宗志锐	岳金山	李学清
09:20-09:45	楼立恒	贾弘洋	黄琪枫
09:45-10:10	于　锐	程伯骏	揭　路
10:10-10:30 | 茶　歇			
	High Precision CIM Macros 主持人：冯立琛	**Low-Power Edge SoCs** 主持人：李炎	**Resonant and Sigma Power Converters** 主持人：陈映平
10:30-10:55	张　锋	张奥扬	邱　浩
10:55-11:20	杜　力	郭衍束	黄　沫
11:20-11:45	司　鑫	成　凯	屈万园
11:45-12:10	于维翰	董彦池	姜俊敏
12:10-13:30 | 午　休			
	THz and mm-Wave Transceivers 主持人：邓伟	**High-Speed Wireline Interfaces** 主持人：胡诣哲	**Compute-in-Memory and Edge Accelerators** 主持人：林龙扬
13:30-13:55	胡三明	桂小琰	尹首一
13:55-14:20	周培根	潘　权	窦春萌
14:20-14:45	郭　浩	杜　源	陈一鸣
14:45-15:10	江　晨	张　钊	朱浩哲
15:10-15:35	陈文华	倪熔华	冯立琛
15:35-15:45 | 茶　歇			
	RF Frequency Generation Circuits 主持人：胡三明	**Analog Circuits and Sensors** 主持人：王子轩	**Power Converters and Gate Drivers** 主持人：姜俊敏
15:45-16:10	王　燕	宋　爽	詹陈长
16:10-16:35	邓　伟	聂凯明	潘东方
16:35-17:00	黄智强	赵　博	陈映平
17:00-17:25	胡诣哲	赵　健	周泽坤
17:25-17:50	李浩然	罗宇轩	张德生
17:50-18:15	彭亚涛	黄张成	杨佳成

2026 年 3 月 27 日 · 第 3 天			
	宴会厅 1	宴会厅 2	宴会厅 3
	RF Front-End Circuits 主持人：罗讯	**AI and Vision Accelerators** 主持人：涂锋斌	**Energy Harvesting and Power Conversion** 主持人：潘东方
08:30-08:55	王科平	阮家辉	曹　鹏
08:55-09:20	孟凡易	杨　旭	刘　寻
09:20-09:45	王　云	姚　鹏	郭建平
09:45-10:10	亓庚浈	封晓宇	崔　楷
10:10-10:30 | 茶　歇			
	Wideband RF Transmitters 主持人：王科平	**Biomedical Edge-AI Processors** 主持人：朱浩哲	**Delta-Sigma Modulators and Time-Domain Converters** 主持人：冼世荣
10:30-10:55	殷　韵	林龙扬	孙　楠
10:55-11:20	罗　讯	李嘉敏	陈铭易
11:20-11:45	杨秉正	朱建峰	王夏宇
11:45-12:10	周　杰	刘嘉豪	祁　亮
12:10-13:30 | 午　休			
	High-Speed Wireline and Optical Links 主持人：许灏	**Precision Analog Interfaces and Sensors** 主持人：祁亮	**Integrated Power and Low-Power Systems** 主持人：刘寻
13:30-13:55	祁　楠	唐　中	程　林
13:55-14:20	贾海昆	吕良剑	孟　淼
14:20-14:45	郑旭强	刘　彦	王远飞
14:45-15:10	江文宁	石　丹	胡　琛
15:10-15:35	赵潇腾	李海华	路　延
15:35-15:45 | 茶　歇			
	Advanced RF Front-End Circuits 主持人：殷韵	**Processors for Next-Generation AI** 主持人：刘诗玮	**High-Speed Data Converters and Sensor Interfaces** 主持人：江文宁
15:45-16:10	许　灏	陈迟晓	冼世荣
16:10-16:35	文进才	刘　波	仲　易
16:35-17:00	顾　鹏	李潇然	罗　豪
17:00-17:25	唐大伟	王　扬	唐希源
17:25-17:50	/	/	ICAC 2026 闭幕仪式 & ICAC 2026 最佳学生海报颁奖

CONFERENCE SCHEDULE 会议日程详情

2026 年 3 月 24 日 · 第 0 天

1F 大堂

10:00-20:00	签到及会议资料领取

2026 年 3 月 25 日 · 第 1 天

宴会厅 1

08:45-10:15	**培训班 1：Computation-in-Memory Circuits Design** 司鑫，东南大学

宴会厅 2

08:45-10:15	**培训班 2：High Performance Discrete-time Amplifiers Utilizing Time-varying Settling Processes** 沈林晓，北京大学

宴会厅 3

08:45-10:15	**培训班 3：IC Design Meets Piezoelectrics: Energy Harvesting and Resonator-Based DC/DC Converters** 杜思俊，荷兰代尔夫特理工大学

10:15-10:30 | 茶 歇

宴会厅 1

10:30-12:00	**培训班 4：Architecture and Design Methodology of Domain-Specific Accelerators** 贾天宇，北京大学

宴会厅 2

10:30-12:00	**培训班 5：High-Speed SerDes Design** 贾海昆，清华大学

宴会厅 3

10:30-12:00	**培训班 6：Design and Research on DC-DC Converters for Computing Devices** 屈万园，浙江大学

12:00-13:30 | 午 休

大宴会厅

13:30-13:45	**ICAC 2026 开幕仪式 & ICAC 2025 最佳报告颁奖**
13:45-14:15	**大会报告：洪志良，复旦大学** A 71.5-dB SNDR 475-MS/s Ringamp-Based Pipelined SAR ADC With On-Chip Bit-Weight Calibration
14:15-14:45	**大会报告：任天令，清华大学** A Fully Flexible Compute-in-memory Chip for Edge Intelligence

14:45-15:15 | 茶 歇

宴会厅 1

RF, mm-Wave and Photonic Circuits

主持人：贾海昆

15:15 **TALK #2.1**	**Advanced Optical Transmitter and Receiver Design for Short-reach Scale-Out Interconnect Arrays** 俞捷，香港科技大学
15:40 **TALK #2.2**	**CMOS mm-Wave and THz Clock and System for Sensing and Communication** 李连鸣，东南大学
16:05 **TALK #2.3**	**A 2Ø 500Gb/s Monolithic Silicon-Photonic DWDM PAM-4 Transceiver in 45nm CMOS SOI** 毕晓君，华中科技大学
16:30 **TALK #2.4**	**A 20GHz Frequency Synthesizer with Spur-Shaping Modulator Achieving 46.2fs Jitter and -76.5dBc Worst-Case Fractional Spur** 耿新林，电子科技大学
16:55 **TALK #2.5**	**BASS-PLL: A Bandwidth Augmented Sub-Sampling PLL Achieving A Wide Bandwidth Above 30% of the Reference Frequency and A Worst-Case FoMREF of -247.9 dB at 3 GHz with A Ring Oscillator** 王辉，上海交通大学
17:20 **TALK #2.6**	**An Inherently Phase-Tunable Injection-Locked Ring Oscillator for High-Speed Communication Systems** 过悦康，上海交通大学

宴会厅 2

Precision Analog Interfaces and Sensors 主持人：张奕涵	
15:15 TALK #3.1	A ±60mA-Inaccuracy Low-Side Average Current Sensor with Operating-Conditions-Insensitive Control Supporting 0.1-to-3A Load Range and Sub-100ns Sample Time for Automotive USB Charge Application 明鑫，电子科技大学
15:40 TALK #3.2	From Liability to Asset: Harnessing Comparator Resolution Time for Input Amplitude Estimation and Metastability Mitigation 沈林晓，北京大学
16:05 TALK #3.3	A 0.4-V 32-kHz Pulse-Injection Temperature-Compensated Crystal Oscillator With Sub-Cycle CL Modulation and DLL-Reused Temperature Sensor 李家明，澳门大学
16:30 TALK #3.4	A Cryogenic Nano-Watt PVT-Insensitive CMOS Voltage Reference Operating From 4 to 300 K 王晶，中国科学技术大学
16:55 TALK #3.5	A +43.3-dBm IIP3, Low-Power Transimpedance Amplifier Employing a Switched-Capacitor Amplifier-Based Transition-Band Pole-Zero Doublets Compensation Technique 金锦，南京理工大学
17:20 TALK #3.6	A 24-to-27.5GHz Self-Adaptive Load-Modulated Balanced Amplifier for Integrated Communication, Sensing and Power Transfer Scenarios 余超，东南大学

宴会厅 3

AI Accelerators and DSA 主持人：岳金山	
15:15 TALK #4.1	A 14.08-to-135.69Token/s ReRAM-on-Logic Stacked Outlier-Free Large-Language-Model Accelerator with Block-Clustered Weight-Compression and Adaptive Parallel-Speculative-Decoding 赵亮，浙江大学
15:40 TALK #4.2	BayesBB: A 9.6-Gb/s 1.61-ms Configurable All-Message-Passing Baseband-Accelerator for B5G/6G Cell-Free Massive-MIMO Systems 张川，东南大学/紫金山实验室

16:05 **TALK #4.3**	**A 0.00022mm2/electrode 1024-Channel Sparsity-Aware Neural Interface with CIM-Based PredictiveFocused Sampling for Hotspot Spike Tracking** 杨杰，西湖大学
16:30 **TALK #4.4**	**Generative AI Accelerator Design for Visual Autoregressive Model** 贾天宇，北京大学
16:55 **TALK #4.5**	**A Potts Machine With Coefficient Reuse Strategy and Successive Boundary Approximation Annealing for Multi-State Combinatorial Optimization** 陈卓俊，湖南大学
17:20 **TALK #4.6**	**A Hierarchical-Hybrid Floating-Point Compute-in-Memory Macro Using FP-DAC and FP-ADC for Edge-AI Devices** 赵元哲，澳门大学

宴会厅 1

18:00-19:00	**合作展商宣传&欢迎冷餐会**

宴会厅 3

19:00-21:00	**学生海报展示**

2026 年 3 月 26 日 ·第 2 天

宴会厅 1

Radar and RF Transceivers 主持人：胡诣哲	
08:30 TALK #5.1	A 1.6-to-3.8GHz Reconfigurable FMCW Radar SoC with 81.5% Relative-Bandwidth PLL for Real-Time Life Detection in Disaster Response 张慧，北京航空航天大学
08:55 TALK #5.2	Self-Interference Cancellation in Millimeter-Wave Automotive Radar Receivers 宗志锐，香港科技大学（广州）
09:20 TALK #5.3	A 128mW 2Ø4 Radar-on-Chip with Forward-M DPLL-Locked Multi-Injection RTWO in 22nm CMOS Enabling ADC-Free Digitization and PS-Free Beamforming Demonstrated in In-Cabin Vital-Sign Monitoring 楼立恒，中国科学技术大学
09:45 TALK #5.4	A NearLink 2.0 Compliant Dual-Band RF Transceiver for Smart Wireless Personal Audio Applications 于锐，华为新加坡研究所

宴会厅 2

Neuromorphic Processors and Security 主持人：郭衍束	
08:30 TALK #6.1	ANP-OT: A 0.17nW/Synapse 0.46pJ/SOP Neuromorphic Olfactory Processor with On-Chip Transfer Learning for Non-Invasive Cross-Hospital Cross-Pulmonary-Disease Diagnosis 陈虹，清华大学
08:55 TALK #6.2	A 28-nm Computing-in-Memory Processor With Zig-Zag Backbone-Systolic CIM and Block-/Self-Gating CAM for NN/Recommendation Applications 岳金山，中国科学院微电子研究所
09:20 TALK #6.3	Enabling Energy-Efficient Homomorphic Encryption Evaluation via Programmable In-Situ Computing 贾弘洋，清华大学
09:45 TALK #6.4	SpikeRAM: A 48.1pW/Synapse/Bit Event-driven Spiking Compute-Near/In-Memory Processor with Neuromorphic Sensor Enabling Life-Long On-Chip Learning 程伯骏，香港科技大学（广州）

宴会厅 3

Advanced ADC and DAC Architectures 主持人：唐希源	
08:30 TALK #7.1	Reasons for "Not" Engaging in Analog-to-Digital Converter Research 陈知行，澳门大学
08:55 TALK #7.2	A 16-bit 10-GS/s DAC Achieving >67dBc SFDR and <-77dBc IM3 up to the Nyquist in 28nm CMOS 李学清，清华大学
09:20 TALK #7.3	A 5-MS/s 16-bit Low-Noise and Low-Power Split Sampling SAR ADC With Eased Driving Burden 黄琪枫，华为香港研究所
09:45 TALK #7.4	The Renaissance of Common-Gate Amplifiers: A High-Linearity Resistive-Input Pipe-SAR ADC Enabled by Continuous-Time Floating Charge Transferrer 揭路，清华大学

10:10-10:30 | 茶 歇

宴会厅 1

High Precision CIM Macros 主持人：冯立琛	
10:30 TALK #8.1	A 28-nm 88.3-TFLOPS/W POSIT-Approximate-Calculation-Based Digital Computing-in-Memory Macro Incorporating Final-Cycle Fusion and Joint Skipping 张锋，中国科学院微电子研究所
10:55 TALK #8.2	RAC-NAF: A Reconfigurable Analog Circuitry for Nonlinear Activation Function Computation in Computing-in-Memory 杜力，南京大学
11:20 TALK #8.3	A 28nm 127.54TFLOPS/W MXFP6 and 117.42TFLOPS/W MXFP8 Compute-in-Memory Macro with Adaptive-Preserved-Bit-Width and Serial-Dual-Bit-Sliding Schemes 司鑫，东南大学
11:45 TALK #8.4	AFP-CIM: All-Inclusive Floating-Point With Segmented Compute-in-Memory Macro 于维翰，澳门大学

宴会厅 2

Low-Power Edge SoCs 主持人：李炎	
10:30 TALK #9.1	SharpSAT: A Heuristic-Learning-Based SAT Accelerator Achieving 0.8ζs/16.1ζs Solution Time in SAT/UNSAT Cases 张奥扬，清华大学
10:55 TALK #9.2	A 174/756-nW 6-Class Keyword Spotting ASIC With Delta/Successive-Approximation Dual-Mode Quantizer 郭衍束，上海交通大学
11:20 TALK #9.3	A 65nm 0.066pJ/bit Floating-Latch-Based True Random Number Generator Resilient to Power-Noise Injection Attacks 成凯，中国科学院微电子研究所
11:45 TALK #9.4	A Heterogeneous TinyML SoC With Systematic Minimum Energy Searching and Management for Keyword Spotting 董彦池，北京大学

宴会厅 3

Resonant and Sigma Power Converters 主持人：陈映平	
10:30 TALK #10.1	A Galvanic Isolator Achieving 117-Mb /s Forward Data Transfer in the Presence of 181-kV/ζs Common-Mode Transient Interference 邱浩，南京大学
10:55 TALK #10.2	Maximum-360MHz Coupled-OSC-based Converters Achieving 89.5% Peak Efficiency 黄沫，澳门大学
11:20 TALK #10.3	A Compact 4Vin 93.4%-Peak-Efficiency 12A Load and 20mV Undershoot Resonant Sigma Converter with PCB-Embedded Converter-on-Substrate Packaging 屈万园，浙江大学
11:45 TALK #10.4	5-1V DLDO-SC-MConverter 姜俊敏，南方科技大学

12:10-13:30 | 午 休

宴会厅 1

THz and mm-Wave Transceivers 主持人：邓伟	
13:30 TALK #11.1	A 140GHz Full-Duplex CMOS Transceiver with Metasurface-Integrated Self-Interference-Cancelling Antenna Supporting 16Gb/s 16QAM Dual-Mode Bidirectional Communication 胡三明，东南大学
13:55 TALK #11.2	Integrated Transceiver Chip for Terahertz Communication and Sensing 周培根，东南大学
14:20 TALK #11.3	A 436-to-472GHz 4-Element IF Beamforming Phased-Array Receiver in 65nm CMOS 郭浩，香港城市大学
14:45 TALK #11.4	THz-TSI: A 0.33pJ/b 264Gb/s Through-Silicon Interconnect Module for 3D Integration Utilizing Terahertz Coupling 江晨，复旦大学
15:10 TALK #11.5	A 200-to-350GHz broadband SiGe BiCMOS Frequency Doubler with Slotline-Based Mode-Decoupling Harmonic-Tuning Technique 陈文华，清华大学

宴会厅 2

High-Speed Wireline Interfaces 主持人：胡诣哲	
13:30 TALK #12.1	A 112-Gb/s PAM4 SBD Transceiver with Mismatch-Compensated 2xVDD Hybrid and Two-Step Echo Canceller 桂小琰，西安交通大学
13:55 TALK #12.2	A 72Gb/s/pin Single-Ended Simultaneous Bi-Directional Transceiver with C-Peaking Leakage Cancellation and Dual-Loop Hybrid Impedance Calibration for Chiplet Interfaces 潘权，南方科技大学
14:20 TALK #12.3	A 47.0Tb/s/mm 112Gb/s/pin PAM4 Single-Ended Transceiver Featuring 4-Aggressor Crosstalk Cancellation and Supply-Noise Tolerance for Short-Reach Memory Interfaces 杜源，南京大学
14:45 TALK #12.4	Recent Research Progress on the PLL and CDR Forwireless/Wireline Communication 张钊，中国科学院半导体研究所

15:10 TALK #12.5	A 21.6fsrms-Jitter, -260.7dB-FoM Fractional-N PLL Enabled by an Intrinsically Linear Variable-Slope SPD for Quantization Error Cancellation 倪熔华，复旦大学

宴会厅 3

Compute-in-Memory and Edge Accelerators

主持人：林龙扬

13:30 TALK #13.1	A 28nm 47.3TFLOPs/W 894mJ/inference Visual Autoregressive Accelerator with Differential-Amplifier Speculation and Chain-Reaction-like Parallel Generation 尹首一，清华大学
13:55 TALK #13.2	A 12nm 4Mb INT/FP4 Charge-Trap Transistor-Based Computing-in-Memory Macro Using Analog-Predict-Digital-Compute for AI Edge Devices 窦春萌，中国科学院微电子研究所
14:20 TALK #13.3	Hybrid SRAM/ROM Compute-in-Memory Architecture for High Task-Level Energy Efficiency in Transformer Models With 8928-kb/mm^3 Density in 28nm CMOS 陈一鸣，清华大学
14:45 TALK #13.4	A 22-nm 109.3-to-249.5-TFLOPS/W Outlier-Aware Floating-Point SRAM Compute-in-Memory Macro for Large Language Models 朱浩哲，复旦大学
15:10 TALK #13.5	A 28nm 106.85TOPS/W and 77.68TFLOPS/W CIM Macro with Stage-Wise-Enabled Lossless Compressors Based on Sign-Bit-Embedded Transition-Counting-Lines for Edge-AI Devices 冯立琛，西安电子科技大学

15:35-15:45 | 茶 歇

宴会厅 1

RF Frequency Generation Circuits

主持人：胡三明

15:45 TALK #14.1	A 14GHz Chopper-Refolding Sampling PLL Achieving 33.8fsrms and 80.8dBc Reference Spur with a kT/C-Noise-Cancellation SPD 王燕，清华大学
16:10 TALK #14.2	Multi-Reference PLL: Theory and Implementation 邓伟，清华大学
16:35 TALK #14.3	A 14GHz Ring-Based 3rd-Order Fractional-N PLL with 164fsrms Jitter and a 100MHz Reference 黄智强，香港科技大学（广州）
17:00 TALK #14.4	A PLL Technique: Charge-Steering Sampling 胡诣哲，中国科学技术大学

17:25 TALK #14.5	A Low-Jitter mm-Wave Fractional-N Sub-Sampling PLL Using a Polarity-Reversible SSPD for DTC Range Reduction 李浩然，澳门大学
17:50 TALK #14.6	A 17.9-to-22.4GHz 195.6 ± 1.3dBc/Hz FoM Quad-Core Class-F-1 VCO Featuring Improved Synchronization Using a Circular Pentafilar Transformer-Based Tank 彭亚涛，澳门大学

宴会厅 2

Analog Circuits and Sensors

主持人：王子轩

15:45 TALK #15.1	Energy Efficient Amplifier for Driving Large Capacitive Loads 宋爽，浙江大学
16:10 TALK #15.2	A 140-dB Single-Exposure Wide-Dynamic-Range CMOS Image Sensor Combining LOFIC and Selective Overflow Technology 聂凯明，天津大学
16:35 TALK #15.3	A Battery-Free Wireless Electrochemical-Interface SoC Featuring 143dB Dynamic Range for Multimodal Wearables 赵博，浙江大学
17:00 TALK #15.4	Energy-Efficient and Environmentally Resilient Transceivers for Body Channel Communication 赵健，上海交通大学
17:25 TALK #15.5	Energy Efficient Sensor Interface for Digital Microphones 罗宇轩，浙江大学
17:50 TALK #15.6	A 128Ø 96 Multimodal Flash LiDAR SPAD Imager with Object Segmentation Latency of 18ζs Based on Compute-Near-Sensor Ising Annealing Machine 黄张成，复旦大学

宴会厅 3

Power Converters and Gate Drivers

主持人：姜俊敏

15:45 TALK #16.1	A Light-Load Optimized Dual-Output Fly-Buck Converter With an Implicit Feedback of the Isolated Output 詹陈长，南方科技大学
16:10 TALK #16.2	A 24V-to-20V Isolated DC-DC Converter using a Transformer-Based Supply-Generating Technique 潘东方，中国科学技术大学

16:35 TALK #16.3	A Closed-Loop EMI Regulated GaN Power Converter with 500MHz-Sampling-Bandwidth In-Situ EMI Sensing and 9kHz-Resolution Global Excess-Spectrum Modulation 陈映平，复旦大学
17:00 TALK #16.4	A Condition-Insensitive Active SiC Gate Driver With On-Chip di/dt and dv/dt Sensing for Targeted Slew Rate Control 周泽坤，电子科技大学
17:25 TALK #16.5	An Adaptive Three-Stage GaN Gate Driver With Peak Miller Plateau Voltage Tracking and Voltage Tailing Suppression for 36.4% Switching Loss Reduction 张德生，华中科技大学
17:50 TALK #16.6	A Multi-Phase Hybrid Converter with Q Samplers Enabling Simultaneous IL Auto-Balance and Arbitrary Phase Count 杨佳成，澳门大学

2026 年 3 月 27 日 ·第 3 天

宴会厅 1

RF Front-End Circuits 主持人：罗讯	
08:30 TALK #17.1	Reflectionless Blocker-Tolerant Mixer-First Receivers for 5G-Advanced/6G FR3 Communications 王科平，天津大学
08:55 TALK #17.2	Design Practices of a 5G NR FR2 Low-noise Amplifier and a FR3 Power Amplifier 孟凡易，天津大学
09:20 TALK #17.3	Ultra-Wideband Miniaturized RF Amplifier Integrated Circuit Design 王云，复旦大学
09:45 TALK #17.4	A Multi-Band RF Transmitter Employing a Transformer-Based N-Path Switched-Capacitor Modulator for CIM3 Suppression 亓庚浈，中山大学

宴会厅 2

AI and Vision Accelerators 主持人：涂锋斌	
08:30 TALK #18.1	CNN Accelerator Featuring a Memory Stationary Dataflow 阮家辉，澳门大学
08:55 TALK #18.2	A 10 000-Inference/s Bio-Inspired Spiking Vision Chip Based on an End-to-End SNN Embedding Image Signal Enhancement 杨旭，中国科学院半导体研究所
09:20 TALK #18.3	HYDAR: A 390K QPS, 1574K QPS/W Hybrid Analog/Digital Compute-in-RRAM Accelerator for Efficient Recommendation System 姚鹏，清华大学
09:45 TALK #18.4	A 1286fps 0.39mJ/Frame Modeling/Rendering Unified 3D GS Processor with Locality-Optimized Computation and Reconfigurable Architecture 封晓宇，清华大学

宴会厅 3

Energy Harvesting and Power Conversion 主持人：潘东方	
08:30 TALK #19.1	A Three-Mode Single-Inductor Four-Quadrant Converter Achieving 94.6% Peak Efficiency with Seamless Zero-Crossing 曹鹏，南京大学
08:55 TALK #19.2	120V/230V Non-Isolated AC-DC Converter with High Power Density for IoT Devices 刘寻，香港中文大学（深圳）
09:20 TALK #19.3	Piezoelectric Energy Harvesting: From MPP to MPPT 郭建平，中山大学
09:45 TALK #19.4	A Multi-Coil Scalable Energy-Shared Wireless Power Receiver Network for Distributed Time-Division-Multiplexing Somatosensory Cortex Stimulation 崔楷，清华大学

10:10-10:30 | 茶 歇

宴会厅 1

Wideband RF Transmitters 主持人：王科平	
10:30 TALK #20.1	Wideband Digital RF Transmitter Design 殷韵，复旦大学
10:55 TALK #20.2	Digital-RF Transmitter for mm-Wave Application 罗讯，深圳大学
11:20 TALK #20.3	A 0.6-to-0.9GHz, 28.06dBm Pout, 43.73% SE, 6-Phase Switched-Capacitor Power Amplifier Using In-Cell Digital Waveform Synthesis for the 2nd-, 3rd-, and 4th-Harmonic Suppression 杨秉正，深圳大学
11:45 TALK #20.4	A 4.5-to-7.2GHz Beyond Rail-to-Rail Output SCPA with 27.9dBm Pout and 46.2% DE at 5.1GHz Using Periodic Voltage-Pacing Network 周杰，深圳大学

宴会厅 2

Biomedical Edge-AI Processors 主持人：朱浩哲	
10:30 TALK #21.1	Collapsing the Vision Stack: Ultra-Efficient Analog Intelligence for Edge AI 林龙扬，南方科技大学
10:55 TALK #21.2	A Patient-Independent Prototype-Based Spatio-Temporal CNN Processor with Forward-Inference-Based Adaptation for Robust and Low-Latency Seizure Detection 李嘉敏，南方科技大学
11:20 TALK #21.3	A 28-nm 239-bp/ζJ Agile Pangenome Analysis Accelerator for Multi-Scheme Read Mapping 朱建峰，清华大学
11:45 TALK #21.4	A High-Accuracy and Ultra-Energy-Efficient Cardiac Arrhythmia Classification Processor for Wearable Intelligent ECG Monitoring 刘嘉豪，电子科技大学

宴会厅 3

Delta-Sigma Modulators and Time-Domain Converters 主持人：冼世荣	
10:30 TALK #22.1	A Power-Efficient Jitter-Insensitive Wideband 1-bit CT¯ MADC with Direct Charge Dump Feedback 孙楠，清华大学
10:55 TALK #22.2	A 25.8% 3μ/ζ-Accuracy, 0.12%/丈 Temperature Drift Sigma-Delta Modulation Calibrated Pseudo-Resistor With GΣ to TΣ Tuning Range 陈铭易，上海交通大学
11:20 TALK #22.3	A Multi-Event, 7.9-ps Resolution Time Amplification-Based TDC With an Ultra-Low Static Phase Error DLL Using Interpolator Recycling Technique for dToF Applications 王夏宇，西安电子科技大学
11:45 TALK #22.4	Time-Interleaved¯ MADC for Broadband Wireless Applications 祁亮，上海交通大学

12:10-13:30 | 午 休

宴会厅 1

High-Speed Wireline and Optical Links 主持人：许灏	
13:30 TALK #23.1	Monolithically Integrated DWDM Si-Photonic Transceiver for Chiplet Optical I/O 祁楠，中国科学院半导体研究所
13:55 TALK #23.2	Exploring the Speed Limit of Planar CMOS Processes: A 240Gbps 0.7pJ/bit Analog Efficiency PAM4 Transmitter in 65n CMOS Process 贾海昆，清华大学
14:20 TALK #23.3	A 112-Gb/s PAM-4 Retimer Transceiver 郑旭强，中国科学院微电子研究所
14:45 TALK #23.4	A 16Gb/s/pin 0.51pJ/bit Single-Ended NRZ Transceiver with Distributed Dual-Loop VDDQ Ripple Compensation and Dynamic Clock Duty-Cycle Calibration for Memory Interfaces 江文宁，复旦大学
15:10 TALK #23.5	Compatibility and Testability Techniques for High-Speed and High-Density Interfaces 赵潇腾，西安电子科技大学

宴会厅 2

Precision Analog Interfaces and Sensors 主持人：祁亮	
13:30 TALK #24.1	Capacitively-Biased Diode Technique and Its Applications 唐中，西安电子科技大学
13:55 TALK #24.2	A 1ppm/°C and ±0.066% 3μ Accuracy Bandgap Reference with Temperature-Adaptive PTAT Scaling 吕良剑，华东师范大学
14:20 TALK #24.3	PWM-Based Impedance Boosting Technique With Autonomous Background Calibration for VCO-Based Neural Front Ends 刘彦，上海交通大学
14:45 TALK #24.4	A Wire-Metal-Based Temperature Sensor With a Fractional-Discharge FLL and V2T Converter Achieving 45-fJ¸K2 R-FoM in 28-nm CMOS 石丹，广东工业大学
15:10 TALK #24.5	A 0.6V 9.4ζW 1,892ζm2 Current-Pulse-Injection Crystal Oscillator Featuring Capacitively Biased Amplifier with 242.2dBc/Hz PN FoM @1kHz Offset 李海华，澳门大学

宴会厅 3

Integrated Power and Low-Power Systems 主持人：刘寻	
13:30 TALK #25.1	A 100A LLC Resonant Converter with an Embedded Primary-Current-Extracted Regulator 程林，中国科学技术大学
13:55 TALK #25.2	PVT-Robust Wide-Band Backscatter Modulator for Ultra-Low Power IoTs 孟淼，同济大学
14:20 TALK #25.3	A Battery Charger Based On Mesh-Connection 2Ø CF Continuously-Scalable-Conversion-Ratio Converter Achieving 3.2W/mm3 Power Density 王远飞，澳门大学
14:45 TALK #25.4	A 2.5-5V Input 100V Output 86.2% Peak Efficiency Fibonacci-Dickson Hybrid Converter for Acoustic Surface Audio Driver 胡琛，南方科技大学
15:10 TALK #25.5	An Inductor-at-Middle Hybrid Buck Converter with Shared Power-Signal Path for Distributed Vertical Power Delivery 路延，清华大学

15:35-15:45 | 茶 歇

宴会厅 1

Advanced RF Front-End Circuits 主持人：殷韵	
15:45 TALK #26.1	Design of 25–31GHz Power Amplifier and True Power Detection in 40nm CMOS 许灏，复旦大学
16:10 TALK #26.2	A Compact 26/38GHz-Reconfigurable Dual-Band LNA Using Transformer-Based Pole-Zero-Inversion Image-Rejection Technique Achieving >39/41dB IRR for 5G Multi-Band Applications 文进才，杭州电子科技大学
16:35 TALK #26.3	K-/Ka-Band Down/Up Frequency Converter Chipsets for Phased Array SATCOM Ground Terminals 顾鹏，东南大学
17:00 TALK #26.4	Ultra-Broadband Self-Compensated Vector-Modulation Phase Shifter With Over 100-GHz Bandwidth 唐大伟，东南大学

宴会厅 2

Processors for Next-Generation AI 主持人：刘诗玮	
15:45 TALK #27.1	Scalable Compute-in/near-Memory Systems with 2.5D/3D/3.5D Integration 陈迟晓，复旦大学
16:10 TALK #27.2	A 51.6ζJ/Token Subspace-Rotation-Based Dual-Quantized Large-Language-Model Accelerator with Fused Scale-Activation INT Datapath and Rearranged Bit-Slice LUT Computation 刘波，东南大学
16:35 TALK #27.3	A Multicore Programmable Variable-Precision Near-Memory Accelerator for CNN and Transformer Models 李潇然，北京理工大学
17:00 TALK #27.4	A 28nm Speculative-Decoding LLM Processor Achieving 105-to-685ζs/Token Latency for Billion-Parameter Models 王扬，清华大学

宴会厅 3

High-Speed Data Converters and Sensor Interfaces 主持人：江文宁	
15:45 TALK #28.1	Continuous-Time Pipelined Delta-Sigma ADC With DAC Image Prefiltering 冼世荣，澳门大学
16:10 TALK #28.2	A CMOS Hybrid Common-Gate Current-Integrating Sampler with >37dB SNDR Across 51GHz BW in a 128GS/s Front-End 仲易，清华大学
16:35 TALK #28.3	A 14b 20GS/s RF-Sampling DAC Achieving 70.4dBc IMD3 up to 8.9GHz 罗豪，深圳市中兴微电子技术有限公司
17:00 TALK #28.4	High-Performance Time-Domain Capacitance-to-Digital Converters 唐希源，北京大学

宴会厅 3

17:25-17:50	ICAC 2026 闭幕仪式 & ICAC 2026 最佳学生海报颁奖

PLENARY TALK 特邀大会报告

2026 年 3 月 25 日 · 第 1 天

大宴会厅

Talk #1.1 / 13:45-14:15

洪志良

复旦大学

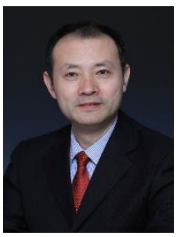
洪志良，博士、复旦大学教授、博导。毕业于中国科学技术大学，瑞士联邦苏黎士高等理工学院(ETHZ)电子工程系获得博士学位后，作为中国第一位博士后研究人员由谢希德先生引进到复旦工作，为国家特殊津贴专家。洪志良教授长期从事模拟集成电路和射频集成电路的研究和教育工作，并为国家培养了 50 多名博士和 300 多名硕士。近年来的主要工作在模拟集成电路，数模混合集成电路和射频的设计和研究，在电源电路研发中富有成果。发表学术论文 300 余篇，出版的书籍有复旦出版社的《计算机系统结构和 RISC 设计》和科学出版社的《模拟集成电路分析和设计》。兼任 2011 年和 2019 年专用集成电路国际会议程序委员会主席，2016-2019 ISSCC 程序委员会委员，澳门大学国家混合集成电路专家委员会专家委员。

TALK

A 71.5-dB SNDR 475-MS/s Ringamp-Based Pipelined SAR ADC With On-Chip Bit-Weight Calibration

This paper presents a single-channel 13-bit 475-MS/s pipelined successive-approximation register (SAR) ADC. To achieve energy-efficient residue amplification, a ring amplifier (ringamp) is exploited in this work with optimized bias scheme and common-mode feedback (CMFB). The inter-stage gain error, mainly due to the finite gain of the ringamp, is calibrated in the background through the proposed auxiliary-latch-based dithering and separate-averaging algorithm. This calibration achieves a fast convergence requiring only 4096 dither-injected samples to be averaged. The DAC mismatch is calibrated by reusing the gain-calibration circuit in the foreground. Fabricated in a 22-nm CMOS process, the ADC consumes 9.93 mW at 475 MS/s and achieves a peak SNDR of 71.5 dB, yielding a Schreier figure of merit (FoMS) of 175.3 dB and a Walden figure of merit (FoMW) of 6.8 fJ/conversion-step. The interleave multi-channel ADC will be presented too!

PLENARY TALK 特邀大会报告



2026 年 3 月 25 日 · 第 1 天

大宴会厅

Talk #1.2 / 14:15-14:45

任天令

清华大学

任天令，教授，清华大学信息科学技术学院副院长，国家杰出青年基金获得者，长江学者特聘教授，IEEE Fellow。2003 年起担任清华大学集成电路学院（微电子所）教授，2011 年至 2012 年为美国斯坦福大学大学访问教授。近年来，承担国家自然科学重点基金、科技部重点研发计划、国家重大科技专项等多项国家重要科技项目，做出一系列具有重要国际影响的学术成果。主要研究领域为智能微纳电子器件、芯片与系统，包括：智能传感器与智能集成系统，柔性智能器件、芯片与系统，二维纳电子器件与芯片等。在国内外重要学术期刊和会议发表论文 750 余篇，包括 Nature、Nature Electronics、Nature Machine Intelligence、Nature Communications、Science Advances、IEEE Electron Device Letters、IEEE Journal of Solid-State Circuits、IEEE Transactions on Electron Devices、IEDM 等，被 Elsevier 等多次评为“中国大陆高被引学者”。拥有中外发明专利 70 余项。担任/曾任 IEEE 电子器件学会副主席（中国大陆首次）、国际微电子领域顶级学术会议 IEDM 执委（中国大陆首次）、IEEE 电子器件学会教育委员会主席（中国大陆首次）、中国微米纳米技术学会理事、IEEE EDS Distinguished Lecturer、IEEE EDTM 执委、IEEE Journal of Electron Device Society 编委、IEEE Transactions on Nanotechnology 编委、《中国科学：信息科学》编委等学术任职。

TALK

A Fully Flexible Compute-in-memory Chip for Edge Intelligence

Flexible electronics, coupled with artificial intelligence, hold the potential to revolutionize robotics, wearable and healthcare devices, human-machine interfaces, and other emerging applications. However, the development of flexible computing hardware that can efficiently execute neural-network-inference tasks using parallel computing remains a substantial challenge. Here we present FLEXI, a thin, lightweight and robust flexible digital artificial intelligence integrated circuit to address this challenge. Our approach uses process-circuit-algorithm co-optimization and a digital dynamically reconfigurable compute-in-memory architecture. Key features include clock frequency operation of up to 12.5 MHz and power consumption as low as 2.52 mW, all while achieving subdollar-per-unit cost and an operational circuit yield of between approximately 70% and 92%. Our circuits can perform 10^10 fixed and random multiplications without error, withstand over 40,000 bending cycles and maintain stable performance for a period exceeding 6 months. A one-shot on-chip neural network deployment eliminates the power consumption and latency associated with sequential weight writing, achieving up to 99.2% accuracy in temporal arrhythmia detection tasks on a single 1-kb chip. In addition, FLEXI demonstrates over 97.4% accuracy in human daily activity monitoring using multimodal physiological signals.

TUTORIAL 芯片设计培训班

2026 年 3 月 25 日 · 第 1 天

宴会厅 1

08:45-10:15

司鑫

东南大学

司鑫，东南大学副教授，博士生导师，国家级青年人才，至善青年学者，紫金青年学者。从事于存算一体 AI 芯片设计，累计发表集成电路领域高水平会议或期刊 60 余篇，包含 17 篇芯片奥林匹克会议论文 ISSCC，11 篇集成电路顶刊 JSSC。主持多项国家省部级科研项目。目前担任电子器件奥林匹克会议 IEDM,亚洲固态电路会议 A-SSCC 等国际会议 TPC。

TUTORIAL

Computation-in-Memory Circuits Design

Computation-in-memory (CIM) has emerged as the most promising solution to the memory wall bottlenecks. The training and inference of LLMs bring new challenges and requirements beyond conventional memory hierarchical structures. This tutorial will introduce the latest CIM solutions for CNNs and Transformers, including floating-point and hybrid CIM designs.

TUTORIAL 芯片设计培训班

2026 年 3 月 25 日 · 第 1 天

宴会厅 2

08:45-10:15

沈林晓

北京大学

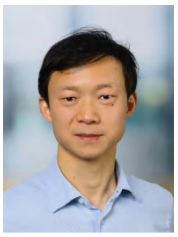
沈林晓，于 2014 年获得复旦大学微电子学院学士学位，2019 年获美国德克萨斯大学奥斯汀分校电气与计算机工程博士学位。现任北京大学集成电路学院助理教授、博士生导师。研究方向涵盖高性能 ADC、模拟/混合信号 IC 设计、智能传感器接口及成像系统，累积在国际顶级期刊与会议发表同行评审论文 60 余篇，其中包括 20 篇 ISSCC 和 20 篇 JSSC 论文。其学术贡献获得多项荣誉，包括 2024 年 IEEE CICC 杰出学生论文奖（通讯作者）、2023 年 IEEE ISSCC Anantha P. Chandrakasan 杰出技术论文奖（通讯作者）、2018-2019 年 IEEE 固态电路学会博士成就奖等。曾担任 ACM/IEEE DAC 技术委员会成员，IEEE TCAS-I 副编辑、现担任 ICAC Workshop TPC 主席，并任职于 IEEE CICC 技术委员会。

TUTORIAL

High Performance Discrete-time Amplifiers Utilizing Time-varying Settling Processes

As a key component of discrete-time ADCs, the discrete-time amplifier often serves as a pivotal determinant of the system's noise and power efficiency. The presentation will start with an overview of the trends and trade-offs associated with various amplifier configurations. It will particularly emphasize the evolution of traditional amplifier designs, where there has been an interesting shift towards leveraging multi-phase time-varying process. This shift aims to accelerate the settling and relax the stringent bandwidth demands. Subsequently, the talk will discuss some popular examples, including the latest developments in ring-amplifier technology and different variants of floating inverter amplifiers.

TUTORIAL 芯片设计培训班



2026 年 3 月 25 日 · 第 1 天

宴会厅 3

08:45-10:15

杜思俊

荷兰代尔夫特理工大学

杜思俊，荷兰代尔夫特理工大学（TU Delft）微电子系副教授。英国剑桥大学（University of Cambridge）电子工程博士，美国加州大学伯克利分校（UC Berkeley）博士后。主要研究方向为高能效电源管理集成电路与系统，涵盖能量采集、无线能量传输以及高效率 DC/DC 功率变换器。现任 ISSCC、ESSERC 等国际会议技术程序委员会（TPC）委员。

TUTORIAL

IC Design Meets Piezoelectrics: Energy Harvesting and Resonator-Based DC/DC Converters

Piezoelectrics are increasingly used in integrated circuits both for kinetic energy harvesting and piezoelectric resonator-based DC/DC conversion, giving rise to two distinct yet closely related circuit design domains. This tutorial provides a circuit-design-oriented overview of ICs based on piezoelectric devices, covering key challenges and solutions in both piezoelectric energy-harvesting interfaces and piezoelectric resonator-based DC/DC power converters. The tutorial highlights representative circuit techniques and design trade-offs when interfacing piezoelectric devices with integrated circuits, illustrated through selected state-of-the-art examples. The goal is to provide practical insights that can guide IC design across a wide range of applications and operating conditions.

TUTORIAL 芯片设计培训班

2026 年 3 月 25 日 · 第 1 天

宴会厅 1

10:30-12:00

贾天宇

北京大学

贾天宇，北京大学集成电路学院助理教授/研究员、博雅青年学者，北京大学集成电路设计系副主任，多模态异构存算一体人工智能芯片北京市重点实验室副主任。美国西北大学博士，哈佛大学博士后，前卡耐基梅隆大学助理研究教授。研究兴趣为数字集成电路设计与 AI 芯片计算架构，在“芯片奥林匹克会议”ISSCC 和芯片领域旗舰会议发表论文 80 余篇，入选国家级青年人才。

TUTORIAL

Architecture and Design Methodology of Domain-Specific Accelerators

Domain-specific accelerator chips have become a significant trend in chip design in recent years. This report will present the cutting-edge development trends by analyzing ISSCC cases, such as near-memory/in-memory computing, Chiplet-based heterogeneous integration, and dedicated computing unit design. The report will also introduce the advancements from design methodology perspectives, covering technologies like agile design methodologies and AI-assisted automated design. The report will reveal that domain-specific chips are rapidly evolving towards a deep integration of "architectural specialization" and "design automation."

TUTORIAL 芯片设计培训班

2026 年 3 月 25 日 · 第 1 天

宴会厅 2

10:30-12:00

贾海昆

清华大学

贾海昆，清华大学集成电路学院副教授。主要研究方向为高速串行接口和硅基毫米波/太赫兹电路设计，包括：高速串行接口、D2D 互连接口、毫米波相控阵、毫米波无线收发机、FMCW 雷达等。作为负责人承担科技部重点研发计划、国家自然科学基金等科研项目。近五年发表学术期刊和国际学术会议论文 100 多篇，包括 ISSCC、JSSC、TMTT、CICC 等集成电路设计顶级学术会议与学术期刊。

TUTORIAL

High-Speed SerDes Design

High-speed Serializer/Deserializer (SerDes) is a core enabling technology for high-bandwidth communication systems, with its rapid evolution from 200G to 400G posing numerous critical technical challenges. Key functions in high-speed data links, including data serialization/deserialization, clock data recovery (CDR), adaptive equalization, and noise suppression, directly rely on high-performance SerDes circuits. High-speed SerDes design is a cutting-edge topic in integrated circuit design, covering mixed-signal circuit implementation, digital signal processing algorithms, and system-level optimization. This tutorial will cover SerDes circuit design from basic concepts and design skills to the latest progress and innovations.

TUTORIAL 芯片设计培训班

2026 年 3 月 25 日 · 第 1 天

宴会厅 3

10:30-12:00

屈万园

浙江大学

屈万园，浙江大学集成电路学院教授，博士生导师，国家级青年人才。博士毕业于韩国科学技术院，2008 年至 2017 年就职于韩国 LG 公司从事集成电路研发工作，历任工程师、资深工程师、责任工程师；2017 年起加入浙江大学并工作至今，长期从事数模混合集成电路设计相关研究工作，主要研究方向为面向三维异构集成的高密度电源管理芯片设计，包括混合电源拓扑的架构构建方法和优化理论、高动态电源环路的控制策略和驱动技术等。领导量产多款高性能电源管理芯片，发表国际固态电路会议及期刊 JSSC 论文多篇，担任多个 IEEE 高水平会议技术委员会成员。

TUTORIAL

Design and Research on DC-DC Converters for Computing Devices

With the rapid development of artificial intelligence technology, the computing power demands of various electronic devices have shown explosive growth. Against this backdrop, high-performance DC-DC converter chips have become the core equipment supporting the development of high-computing-power processors and large-scale data centers. This report will introduce typical DC-DC converter chip designs, summarize and analyze the technical characteristics of existing high-performance DC-DC converters, and analyze the mainstream technical trends in academia by combining current academic technical approaches, providing more technical references for relevant researchers.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 1

TALK #2.1 / 15:15-15:40

俞捷

香港科技大学

俞捷，教授，IEEE Fellow 和 Optica Fellow，他于德克萨斯大学奥斯汀分校获得电子工程学士学位、于斯坦福大学获得电子工程硕士与博士学位。他曾在硅谷和香港联合创立多家科技企业，包括 Atheros、Jetcomm、LiPHY 及 High5 Semi，致力于将科研成果转化为商业化技术。他曾是香港科技大学首任知识转移协理副校长。在二十余载教学生涯中，俞捷教授先后于卡内基梅隆大学（2003-2006）、加州大学圣塔芭芭拉分校（2006-2011）、清华大学（2015-2016）、香港科技大学（2010 至今）及斯坦福大学（1998 年及 2025 年）从事集成电路设计领域的教学科研工作，累计指导超过 30 名博士与 10 余名硕士。俞捷教授的研究涵盖光通信/有线通信/毫米波无线通信集成电路设计、三维计算机视觉模型及智能电网管理系统等多个领域，曾获得 IEEE 超大规模集成电路研讨会时间检验奖（2024）、国际固态电路会议最佳学生论文奖（2003）、IEEE 电路与系统学会杰出青年作者奖（2017）以及中国工程院光华工程科技奖青年奖（2016）。

TALK

Advanced Optical Transmitter and Receiver Design for Short-reach Scale-Out Interconnect Arrays

This talk presents recent advances in high-speed optical transmitter and receiver circuits for short-reach scale-out optical interconnects.

First, a 40-Gb/s 1-to-N VCSEL driver implemented in a 150-nm GaN HEMT process is introduced. Leveraging the high breakdown voltage and broadband capability of GaN devices, the driver directly supports series or parallel VCSEL array configurations without a pre-driver stage. The prototype demonstrates up to 8 mW optical modulation amplitude (OMA) at 40 Gb/s NRZ and supports PAM-4 signaling up to 38 Gb/s while enabling scalable multi-VCSEL operation for higher optical power.

Second, a power- and area-efficient 48-Gb/s PAM-4 optical receiver implemented in 28-nm CMOS is presented. The receiver employs a transadmittance-transimpedance (TAS-TIS) architecture that eliminates inductive peaking and CTLE while maintaining high gain-bandwidth product and linearity. Combined with a 2-tap feed-forward equalizer (FFE) and 2-tap decision feedback equalizer (DFE), the receiver achieves −5.1 dBm sensitivity at 48 Gb/s PAM-4 with 1.28 pJ/bit energy efficiency and only 0.06 mm^2 active area.

Together, these transmitter and receiver designs demonstrate a scalable and energy-efficient optical front-end architecture for next-generation short-reach optical interconnect arrays.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 1

TALK #2.2 / 15:40-16:05

李连鸣

东南大学

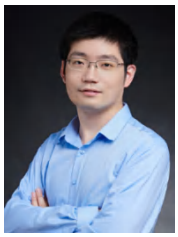
李连鸣，东南大学、紫金山实验室教授，博士毕业于比利时鲁汶大学。个人研究兴趣是毫米波与射频关键电路与系统、天线与先进封装、模拟与数字协同设计等。

TALK

CMOS mm-Wave and THz Clock and System for Sensing and Communication

In this work, we will present our recent works on the CMOS mm-Wave and THz clock and system for wireless sensing and communication applications.

INVITED TALK 邀请报告



2026 年 3 月 25 日 · 第 1 天

宴会厅 1

TALK #2.3 / 16:05-16:30

毕晓君

华中科技大学

毕晓君，华中科技大学教授，博士生导师。长期从事射频模拟集成电路设计方面的研究工作，聚焦超高速光通信收发电路、硅基光电融合集成互连电路及射频毫米波收发电路。入选国家级青年人才计划、主持国家重点研发计划课题 2 项、国家自然科学基金项目 4 项、龙头企业重点合作研究项目 10 多项；带领团队或以主要设计者成功研制：

高能效高密度片间光互连全集成/异质集成收发机芯片（10 x 100 Gbps CMOS DRV+TIA+微环波长锁定的光电全集成芯片、112 Gbps SiGe BiCMOS DRV+MZM+TIA+PD 的光电全集成芯片）；高带宽高线性光通信/光互连收发机电芯片（4 x 128 GBd/2 x 140 GBd/200 GBd+ TIA+DRV，4 x 224 Gbps /448 Gbps TIA 和 DRV、112 Gbps CMOS DFB 驱动放大器、28 GBd CMOS 突发模式时钟数据恢复 CDR 电路，100 GHz 2:1 硅基模拟复接器）；微波光子及毫米波收发机芯片（4-12 GHz 光电振荡器全集成电环路、75-110 GHz 硅基高灵敏度接收机、50-75 GHz 硅基外差式接收机）等。以第一/通讯作者在国际权威会议和期刊（IEEE Trans）发表论文 20 多篇，包括：IEEE ISSCC、T-CAS I/II、T-MTT；以第一作者在 Springer Nature 出版英文专著 2 部；获授权国家发明专利 20 多项，美国专利 2 项。荣获华为火花奖、华科华为先进光技术联合实验室突出贡献奖。任国家自然科学基金重点项目、面上项目评审，华科华为先进光技术联合实验室技术委员会委员，IEEE Access 副主编，IEEE JSSC、T-CAS I、T-MTT 等电路领域权威期刊审稿人。

TALK

A 2×500Gb/s Monolithic Silicon-Photonic DWDM PAM-4 Transceiver in 45nm CMOS SOI

This work presents a monolithic 2×5-λ DWDM microring transceiver in 45-nm CMOS SOI delivering 2×500 Gb/s (100 Gb/s PAM-4/channel). V-groove coupling and a PSR-to-CRR front end enable low loss and tight spacing. A cascaded Q-tamed CTLE yields a TIA of 62 dBΩ, 43.5 GHz, 3.14 μA_rms at 67 mW; the driver delivers 2.5 V_ppd and >30 GHz. A PWM-based WLL locks −5~−6 dB IL. Enabled by electro-photonic co-design, the transceiver achieves <2.5 pJ/bit at 100 Gb/s in end-to-end loopback.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 1

TALK #2.4 / 16:30-16:55

耿新林

电子科技大学

耿新林，电子科技大学讲师，长期致力于硅基射频、毫米波、太赫兹片上时钟产生及分发的理论与设计研究，取得一系列国际领先的原创性研究成果，包括硅基超低抖动超低杂散频率综合器、硅基超高速多相位时钟产生及分发等，在集成电路设计领域顶尖会议/期刊上发表多篇高水平论文，包括 IEEE ISSCC、JSSC、CICC、TMTT 等，相关研究成果入围 2024 年度中国十大半导体研究进展提名。主研多项国家级重点项目，包括国家重点研发计划、国自然重点项目等，获多项中国发明专利与美国发明专利授权。

TALK

A 20GHz Frequency Synthesizer with Spur-Shaping Modulator Achieving 46.2fs Jitter and -76.5dBc Worst-Case Fractional Spur

In this presentation, a frequency synthesizer with ultra-low fractional spur and integrated rms jitter is proposed, which adopts a spur-shaping modulator technique to suppress the nonlinearity caused by inter-slice mismatch, thereby improving the fractional spur mitigation capability.

Implemented in 28nm CMOS process, the prototype is measured to achieve 46.2 fs rms jitter, -76.5 dBc worst-case fractional spur at the near-integer channel, with -251.4 dB FoM and -102.6 dB FoMibs. Notably, the measured rms jitter with and without fractional spur only differs by 0.03 fs.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 1

TALK #2.5 / 16:55-17:20

王辉

上海交通大学

王辉，国家高层次海外青年人才，上海交通大学副教授。分别在上海交通大学和加州大学圣地亚哥分校获得学士和博士学位，博士毕业后在美国斯坦福大学进行博士后研究，回国前在美国高通公司担任射频/混合信号芯片研发工程师，于 2022 年加入上海交通大学。长期从事射频与模拟集成电路设计的研究，在集成电路领域内权威期刊和顶级会议发表多篇关于无线通信芯片、高性能频率芯片、高性能接口芯片等方向的研究成果。多篇论文获得最佳论文提名。授权美国专利多项。担任 CICC 等国际会议 TPC。

TALK

BASS-PLL: A Bandwidth Augmented Sub-Sampling PLL Achieving A Wide Bandwidth Above 30% of the Reference Frequency and A Worst-Case FoMREF of -247.9 dB at 3 GHz with A Ring Oscillator

This work presents a bandwidth augmented subsampling phase-locked loop (BASS-PLL) architecture that features simultaneous out-of-band noise suppression by direct- and multipath-sampling of the ring oscillator's output and in-band noise suppression via an intrinsic sub-sampling mechanism, ultimately combining the benefits of over-sampling PLLs (OSPLLs) and sub-sampling PLLs (SS-PLLs) towards a low jitter compact PLL. A reference multiphase generator is employed to enableMBA sampling paths, each sampling the output of the slope generator that is driven by the ring oscillator for linear- and highsampling gains, enabling stabilized operation at an augmented bandwidth that is >30% of the reference frequency. Meanwhile, each sampling path behaves in a sub-sampling manner without requiring dividers in the feedback loop that consumes additional power overhead and degrades the overall in-band noise performance.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 1

TALK #2.6 / 17:20-17:45

过悦康

上海交通大学

过悦康，上海交通大学长聘教轨助理教授、博士生导师。本科毕业于哈尔滨工业大学，博士毕业于上海交通大学。主要研究方向为混合信号集成电路设计，已发表学术论文 40 余篇，包含 IEEE JSSC、IEEE TCAS-I 等。他曾入选中国电子学会青年人才托举工程、上海市"晨光学者"。

TALK

An Inherently Phase-Tunable Injection-Locked Ring Oscillator for High-Speed Communication Systems

An inherently phase-tunable four-phase injection-locked ring voltage-controlled oscillator (VCO) is presented, proposing an innovative approach that integrates multi-phase generation and clock phase tuning within the oscillator itself. The ring oscillator employs a novel unbalanced feedforward topology, achieving both high power efficiency and high area efficiency. By adjusting the ratio of feedforward current to input current in each stage of the oscillator, the phase of the four-phase output clocks can be precisely and flexibly controlled. The proposed VCO inherently possesses phase tunability/calibration capabilities, enabling direct generation of target phase outputs without the need for additional back-end calibration circuits. This eliminates issues such as noise performance degradation and increased power consumption in the clock path. Combined with injection-locking technology, the oscillator maintains excellent noise performance over a wide frequency range and broad phase tuning range. A prototype oscillator fabricated in a 40-nm CMOS process achieves a frequency tuning range of 3.27–5 GHz. The differential and quadrature phase tuning ranges are -90.0° to 80.9° and -69.6° to 76.5°, respectively, with an average phase tuning resolution of 0.14°/mV. Across the entire phase tuning range, the oscillator achieves a figure-of-merit (FoM) area of 211.1–207.3 dBc/Hz.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 2

TALK #3.1 / 15:15-15:40

明鑫

电子科技大学

明鑫，教授/博导，国家级青年人才、电子科大校百人计划、曾担任功率半导体顶会 ISPSD 技术委员会成员。长期专注于高效、高功率密度电源管理 IC 及硅基 GaN 驱动痛点问题，以提高转换效率、降低 EMI 噪声干扰、实现快速负载响应为目标。多款 GaN 驱动芯片量产，用于快充电源和激光雷达等，产生重要经济价值。近 5 年在 IEEE ISSCC/JSSC、TCAS I/TCAS II、TPE、TIE、ISPSD、CICC 和 ASSCC 等电路旗舰期刊和会议上发表论文 20 余篇；授权美国专利 5 项，中国发明专利 40 余项；参与编著“十三五”国家集成电路设计丛书《功率集成电路设计技术》。2019 年获四川省科学技术发明二等奖。

TALK

A ±60mA-Inaccuracy Low-Side Average Current Sensor with Operating-Conditions-Insensitive Control Supporting 0.1-to-3A Load Range and Sub-100ns Sample Time for Automotive USB Charge Application

A ±60mA inaccuracy low-side average current sensor with operating-conditions-insensitive control is proposed to address accuracy degradation over different operating conditions. It maintains accuracy across varying duty cycles and load currents (0.1-to-3A). An adaptive settling helper reduces settling delay, while a DC level-shift bias improves light-load current sense accuracy. Anti-duty resistor suppress sampling bandwidth variation.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 2

TALK #3.2 / 15:40-16:05

沈林晓

北京大学

沈林晓，2014 年获得复旦大学微电子学院学士学位，2019 年获美国德克萨斯大学奥斯汀分校电气与计算机工程博士学位。现任北京大学集成电路学院助理教授、博士生导师。研究方向涵盖高性能 ADC、模拟/混合信号 IC 设计、智能传感器接口及成像系统，累积在国际顶级期刊与会议发表同行评审论文 60 余篇，其中包括 20 篇 ISSCC 和 20 篇 JSSC 论文，。其学术贡献获得多项荣誉，包括 2024 年 IEEE CICC 杰出学生论文奖（通讯作者）、2023 年 IEEE ISSCC Anantha P. Chandrakasan 杰出技术论文奖（通讯作者）、2018-2019 年 IEEE 固态电路学会博士成就奖等。曾担任 ACM/IEEE DAC 技术委员会成员，IEEE TCAS-I 副编辑、现任职于 IEEE CICC 技术委员会。

TALK

From Liability to Asset: Harnessing Comparator Resolution Time for Input Amplitude Estimation and Metastability Mitigation

Metastability in comparators represents a dominant contributor to elevated bit error rates (BER) in high-speed analog-to-digital converters (ADCs). When the input differential signal approaches the comparator's decision threshold, metastability prolongs the resolution time, potentially exceeding the allocated quantization interval and inducing decision errors.

This presentation proposes an interesting angle that exploits this inherent time-domain characteristic: the resolution time itself encodes supplementary information about the input signal magnitude. By introducing a dedicated time-domain decision criterion alongside conventional voltage comparison, additional amplitude information can be extracted. Based on this principle, two implementations are presented: 1） a dual-path architecture employing precisely background calibrated time-domain thresholds enables concurrent voltage and time-domain comparisons. This approach not only suppresses metastability-induced errors but also enhances effective resolution through the fusion of complementary decision metrics；2）Integration into a pipelined SAR ADC to address inter-stage gain error—a critical performance limiter. Conventional dither-based background calibration entails a trade-off between convergence speed and amplifier swing constraints. Here, real-time time-domain estimation of the input magnitude triggers injection of a large-amplitude dither signal only when the amplifier input swing falls below a defined threshold. This accelerates calibration convergence without expanding the overall input signal range or degrading linearity.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 2

TALK #3.3 / 16:05-16:30

李家明

澳门大学

李家明，博士，现为澳门大学微电子研究院副教授。他于 2016 年从澳门大学获得博士学位。在 2017 至 2019 年间在哈佛大学担任博士后。现在主要研究领域为精准模拟芯片设计、传感器前端电路、核磁共振系统微型化、及芯片跨学科的应用及交叉创新。他已发表超过 60 篇同侪审查期刊及会议文章，当中包括 7 篇发布于 IEEE 国际固态电路研讨会(ISSCC)及 13 篇发布于 IEEE Journal of Solid-State Circuits 都论文。指导的学生获得了 IEEE SSCS Predoctoral Achievement Award、IEEE SSCS Student Travel Grant、IEEE Biosensors Conference Best Paper Award、华人芯片研讨会最佳学生海报等奖项。他现在是 ISSCC ITPC 及 ICTA TPC 成员。

TALK

A 0.4-V 32-kHz Pulse-Injection Temperature-Compensated Crystal Oscillator With Sub-Cycle CL Modulation and DLL-Reused Temperature Sensor

This article presents a 0.4-V 32 kHz pulse-injection (PI) temperature-compensated crystal oscillator (TCXO) that incorporates subcycle capacitive load (CL) modulation for frequency compensation. The proposed TCXO compensates for the crystal's frequency deviation (Δf) by dynamically adjusting the enabling duration of the additional CL within each cycle, thereby ensuring long-term frequency stability. Notably, the design leverages the loop control voltage within a thyristor-based delay-locked loop (DLL) to facilitate energy injection and temperature acquisition for precise compensation. We fabricated the TCXO using the CMOS 65 nm process. Experimental results demonstrate that the TCXO achieves a frequency stability of ±8.5 ppm across a temperature range of −30∘C to 85∘C, while consuming 179.4 nW of power. The achieved Allan deviation (ADEV) of 15.9 parts per billion (ppb) at a 1-s gating interval highlights its superior performance in low-power and high-stability applications.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 2

TALK #3.4 / 16:30-16:55

王晶

中国科学技术大学

王晶，博士，现就职于中国科学技术大学，主要从事宽温度范围低压低功耗模拟集成电路设计及高精度模拟前端（AFE）系统开发。

王博士于 2017 年获得日本早稻田大学（Waseda University）博士学位。2017 年至 2019 年，继续在早稻田大学开展博士后研究工作；2019 年回国加入中国科学技术大学，致力于国家关键领域的高性能模拟集成电路技术攻关。

TALK

A Cryogenic Nano-Watt PVT-Insensitive CMOS Voltage Reference Operating From 4 to 300 K

This work presents a trimming-free, low-power Cryo-CMOS voltage reference for quantum interfaces, operating continuously from 300 K down to 4 K. By compensating for process-dependent threshold shifts, device mismatch, and nonlinearity, the design achieves simultaneous process and temperature compensation over an ultra-wide range.

Fabricated in 180 nm CMOS, 80 test chips demonstrate an average temperature coefficient of 76.9 ppm/K after a one-time model correction. The circuit consumes only 195 to 304 nW while maintaining a stable 1.045 V output with 0.72% fluctuation. Minimum supply voltages are 1.5 V at 300 K and 1.9 V at 4 K. This PVT-insensitive, nanowatt-power reference offers a cost-effective solution for high-accuracy quantum integrated circuits.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 2

TALK #3.5 / 16:55-17:20

金锦

南京理工大学

金锦，南京理工大学电子工程与光电技术学院讲师，博士。2019 年至 2021 年赴意大利帕维亚大学微电子实验室进行学术交流访问，长期从事射频集成电路研究，并获国家自然基金青年基金 C 类、江苏省科协青年科技人才托举工程等项目资助。以第一作者或指导教师身份发表 2 篇一区期刊论文（JSSC）、2 篇二区期刊论文（MWCL 等）。以第一作者或者指导老师在 ISSCC、CICC 等集成电路领域顶级会议上发表 7 篇会议论文。其中以低功耗抗阻塞为主题的一区期刊文章被 JSSC 期刊主席 PAVAN 评为当季度亮点文章。

TALK

A +43.3-dBm IIP3, Low-Power Transimpedance Amplifier Employing a Switched-Capacitor Amplifier-Based Transition-Band Pole-Zero Doublets Compensation Technique

This article proposes a novel zero-pole doublet compensation method for a three-stage operational transconductance amplifier (OTA) used in high-linearity transimpedance amplifiers (TIAs). In the proposed OTA, the first stage employs a switched-capacitor (SC) amplifier, enabling independent and precise control over the frequency locations of the zero-pole doublet. The subsequent second and third stages are formed by a Miller-compensated amplifier incorporating positive feedback, which provides high gain and establishes a high-frequency dominant pole. The proposed compensation method can effectively enhance the gain–bandwidth (GBW) product of the OTA by ten times, resulting in a high input third-order intercept point (IIP3). The designed TIA, fabricated in a 22-nm CMOS process, provides a gain of 5.1 dB with a bandwidth of 20 MHz, and an input-referred noise of 48 μ V (normalized to 10 MHz) with an IIP3 of 43.3 dBm and a 1-dB compression point of 8.3 dBm. The TIA occupies an area of 0.024 mm2 and consumes 4.9 mW from a 1.8-V supply voltage.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 2

TALK #3.6 / 17:20-17:45

余超

东南大学

余超，国家优青，东南大学教授、博导、信息科学与工程学院副院长，中国电子学会高级会员，IEEE 高级会员。2007 年和 2010 年分别于东南大学获信息工程专业学士学位和电磁场与微波技术专业硕士学位，2014 年于爱尔兰国立都柏林大学获电子工程专业博士学位，2015 年完成博士后研究。长期从事无线通信中的射频技术研究，重点深耕高能效射频线性化理论与技术。已发表学术期刊和会议论文 200 余篇，主持国家重点研发计划课题、国家自然科学基金，江苏省自然科学基金等研究项目。曾获 2024 年江苏省行业领域十大科技进展，2024 年江苏省数字经济学会科技进步特等奖，2023 年中国电子学会创新团队奖，2021 年度 IEEE MTT-S Microwave Prize（此次获奖是自 1955 年设立该奖以来中国团队首次获奖），2018 年度《中国科学：信息科学》热点论文奖，2013 年度国家优秀自费留学生奖，以及华为火花奖和中兴通讯优秀项目奖等。指导学生获 APCAP，ICMMT，IWS，ISAP 等国际会议最佳论文奖。

TALK

A 24-to-27.5GHz Self-Adaptive Load-Modulated Balanced Amplifier for Integrated Communication, Sensing and Power Transfer Scenarios

With the emerging sixth-generation (6G) millimeter wave (mm-wave) wireless communication, multi-functional convergence scenarios, such as vehicle-to-everything (V2X) and Internet of Things (IoT), are expected to deliver smarter and more efficient living environments. Consequently, future multifunctional front-ends will extend beyond mere communication capabilities to support sensing and power-transfer functions. There is no doubt that the design of integrated communication, sensing, and power transfer (ICSPT) can largely empower system functionalities and significantly reduce operation costs. The modulated signal with a high peak-to-average power ratio (PAPR) for the communication scenario, which requires the front-ends to support high output-power back-off (OPBO) efficiency. Typically, a wideband frequency-modulated continuous-wave (FMCW) signal is used for the sensing scenario, while a single-tone signal is used for the power-transfer scenario, which both rely on high saturated power, efficiency, and gain. As the most energy consuming devices in the transmitter, power amplifiers (PAs) are required to operate efficiently in both at OPBO and saturation states for ICSPT applications. A 24-to-27.5GHz gallium nitride (GaN) self-adaptive load-modulated balanced amplifier (SALMBA) is proposed for 6G integrated communication, sensing, and power-transfer scenarios. Based on the proposed self-adaptive power divider, the power divide ratio can dynamically change according to the input power levels, and the back-off PAE and saturated performance of the SALMBA can be significantly improved. The SALMBA achieves the saturated PAE of 28.5 to 33%, and 10dB OPBO PAE of 15.3 to 22.1% over 24 to 27.5GHz. And for 2.4Gb/s 64QAM 5G NR signal at 25.5GHz, the SALMBA provides 26.6dBm average output power and 23.3% average PAE.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 3

TALK #4.1 / 15:15-15:40

赵亮

浙江大学

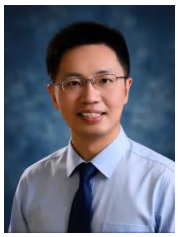
赵亮，浙江大学百人计划研究员，国家级高层次青年人才。本科毕业于清华大学微电子与纳电子学系，博士毕业于斯坦福大学电子工程系，曾任比利时校际微电子中心（IMEC）和香港科技大学人工智能晶片中心（ACCESS）访问学者。曾在知名存储器技术企业担任研发骨干和高级管理职务，作为团队负责人所研发的 RRAM 成套工艺技术进入中芯国际官方路线图并量产 2 亿颗以上。长期从事先进存储器和类脑计算技术研究，在 Nature Communications、Nano Letters、ISSCC、IEDM、VLSI、DAC 等期刊和会议发表高水平学术论文 70 余篇，获发明专利授权 20 项。主持国家重点研发计划重点专项项目、国自然重大研究计划集成项目课题、浙江省重点研发计划项目、浙江省自然科学重大项目等重要科研项目，担任 ICTA、EDTM 等国际会议的技术委员会委员/分会主席，曾获“中国芯”优秀技术创新产品奖、VLSI-TSA 最佳论文奖和 ISSCC 人工智能芯片领域亮点论文。

TALK

A 14.08-to-135.69Token/s ReRAM-on-Logic Stacked Outlier-Free Large-Language-Model Accelerator with Block-Clustered Weight-Compression and Adaptive Parallel-Speculative-Decoding

This work presents a 55nm speculative decoding-based LLM accelerator with bumping-based face-to-face ReRAM-on-logic stacking technology. It features a local rotation unit for outlier-free low-bit quantization, a stacking-aware PNM architecture co-designed with blockwise vector quantization to reduce weight EMA overheads, and an adaptive parallel speculative decoding scheme with out-of-order scheduler for high resource and bandwidth utilization. Our chip achieves 14.08-135.69token/s and 4.46-to-7.17× speedup over vanilla speculative decoding.

INVITED TALK 邀请报告



2026 年 3 月 25 日 · 第 1 天

宴会厅 3

TALK #4.2 / 15:40-16:05

张川

东南大学/紫金山实验室

张川，东南大学教授，紫金山实验室课题联合负责人，国家高层次青年人才。主要从事面向 AI 通信算力需求的算法、芯片与工具链的研究工作。移动信息网络国家科技重大专项首席科学家。获国家自然科学基金重点/优青项目、中国半导体十大研究进展、强国青年科学家、算力中国·青年先锋人物、6G 星辰·青年科学家、中国工程院“中国工程前沿杰出青年学者”、中国青年五四奖章集体等。担任 IEEE 电路与系统学会杰出讲师/CASCOM 技术委员会主席、IEEE JETCAS 高级编委会委员、IEEE TMC 指导委员会委员、及 IEEE ISCAS Tutorial Speaker 等。担任 IEEE TCAS-II/TSP/OJCAS/JETCAS 副主编，IEEE ICCT/WCSP/SiPS（共）主席等。

TALK

BayesBB: A 9.6-Gb/s 1.61-ms Configurable All-Message-Passing Baseband-Accelerator for B5G/6G Cell-Free Massive-MIMO Systems

Cell-free massive multi-input multi-output (CF-mMIMO) has emerged as a promising alternative for the forthcoming beyond 5G and 6G (B5G/6G) systems. As an imperative part of supporting B5G/6G applications, baseband(BB) chips encounter more challenging key performance indicator (KPI) requirements. To achieve the B5G/6G goal of higher than 8-Gb/s/user throughput, less than 2-ms latency, and configurable hardware, a Bayesian inference-based all-message passing baseband-accelerator (BayesBB) is presented in this article. Benefiting from the pipelined and fully unfolded all message-passing architecture, BayesBB delivers three unexplored merits: high throughput (9.6-Gb/s), low latency (1.61-ms), and good configurability. Specifically, a ten-gigabit ethernet (XGE) interface with 10.3125-Gb/s SerDes is used, resulting in 9.6-Gb/s throughput. A fully unfolded MIMO-BP detector achieves a detection latency of 1.44-ms, contributing to chip latency of 1.61-ms. A configurable architecture is designed, supporting various B5G/6G applications, for example, the decoding of both 3GPP low-density parity-check (LDPC) codes and polar codes. As a system-level implementation, tests have verified that 16 arrays of BayesBB can handle the BB processing of a 128 × 128 CF-mMIMO system with commercial setups, delivering 9.6-Gb/s throughput and >100-b/s/Hz spectrum efficiency (SE).

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 3

TALK #4.3 / 16:05-16:30

杨杰

西湖大学

杨杰，博士，西湖大学工学院研究员，脑机接口芯片系统浙江省工程研究中心副主任，IEEE 高级会员。先后入选杭州市“西湖明珠工程”和浙江省高层次人才计划。长期致力于高通量植入式脑机接口芯片与神经信号解码技术研究，主持科技创新 2030 项目课题、工信部揭榜挂帅、浙江省重点研发等多个国家与省部级科研项目。在国际顶级学术期刊与会议（如 ISSCC、JSSC、ICLR 等）发表论文百余篇，积极推动脑机接口、类脑计算与神经解码领域的理论突破、芯片研制与工程转化。

TALK

A 0.00022mm2/electrode 1024-Channel Sparsity-Aware Neural Interface with CIM-Based PredictiveFocused Sampling for Hotspot Spike Tracking

This 1024-ch neural interface solves the power, area, and bandwidth bottleneck by combining low-power panoramic scanning for hotspot prediction withhigh-fidelity spike tracking on active sites. The dynamic allocation is guided by a real-time compute-in-memory (CIM) engine, providing a 16x resolutionboost (10kHz) and a record 0.00022 mm2/elec. efficiency in 40nm CMOS. The design achieves state-of-the-art efficiency, maximizing spike density for itspower and silicon area.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 3

TALK #4.4 / 16:30-16:55

贾天宇

北京大学

贾天宇，北京大学集成电路学院研究员、博雅青年学者，北京大学集成电路设计系副主任。获美国西北大学博士，前哈佛大学博士后，卡耐基梅隆大学助理研究教授。研究兴趣为数字集成电路设计与计算机体系架构，在芯片领域会议和期刊发表论文 80 余篇，包括 ISSCC、VLSI、JSSC、MICRO、DAC 等旗舰刊物。

TALK

Generative AI Accelerator Design for Visual Autoregressive Model

Visual Autoregressive (VAR) is the latest generative model for efficient image generation. This work presents VARSA, a 22nm visual autoregressive accelerator for efficient text-to-image generation. VARSA achieves 503mJ/inference for 512x512 image generation, which is 2.7×-8.9× better than prior Diffusion-based SOTA accelerators.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 3

TALK #4.5 / 16:55-17:20

陈卓俊

湖南大学

陈卓俊，湖南大学半导体学院（集成电路学院）教授、博士生导师。主要研究方向是高能效专用加速器芯片，以及高可靠模拟/数模混合集成电路设计。主持国家自然科学基金面上、青年项目等纵横向项目 20 余项，以第一或通讯作者在 IEEE JSSC, TCASI, TPEL, CICC 等集成电路领域高水平期刊和会议发表论文 30 余篇。曾入选湖南省湖湘青年英才、湖南省青年骨干教师培养对象，获湖南省自然科学二等奖。

TALK

A Potts Machine With Coefficient Reuse Strategy and Successive Boundary Approximation Annealing for Multi-State Combinatorial Optimization

The annealing processor based on the Ising model has attracted significant attention in recent years due to its remarkable ability in solving combinatorial optimization problems (COPs). By mapping a COP to the annealing processor, the optimal or near-optimal solution can be achieved efficiently. However, the Ising model is limited to two spin states, which restricts its application in solving multi-state COPs. To address this limitation, we propose a Potts machine implemented in 65-nm CMOS technology, which is based on a 16 × 16 King's graph topology. The proposed Potts machine supports two to four spin states and is compatible with both the Ising model and the Potts model. Additionally, we introduce an intra- and inter-coefficient reuse strategy, which effectively decreases the coefficient memory area overhead by 68.75%. Furthermore, we propose a successive boundary approximation (SBA) annealing method to address the challenges associated with long convergence time. The measurement results demonstrate that the proposed SBA annealing method achieves a 10× acceleration in comparison to the conventional simulated annealing approach. The proposed Potts machine has a spin area of 4400 μm2 and exhibits an energy consumption of 1.06 nJ when powered by a 1-V supply.

INVITED TALK 邀请报告

2026 年 3 月 25 日 · 第 1 天

宴会厅 3

TALK #4.6 / 17:20-17:45

赵元哲

澳门大学

赵元哲，博士，2020 年获得电子科技大学学士学位，并于 2025 年获得澳门大学博士学位。目前，他在澳门大学模拟与混合信号超大规模集成电路国家重点实验室（AMSV）担任博士后研究员，长期从事存内计算、边缘人工智能芯片等设计研究。在 IEEEJSSC/TCAS-I/CICC/ASSCC 等集成电路领域顶级期刊和会议发表 12 篇论文，其中第一作者发表 8 篇（含共一），并担任 IEEE JSSC/TCAS-I 等期刊审稿人。

TALK

A Hierarchical-Hybrid Floating-Point Compute-in-Memory Macro Using FP-DAC and FP-ADC for Edge-AI Devices

This article presents an energy-efficient FP-CIM macro designed for edge-AI devices. It addresses energy efficiency bottlenecks through three key features: 1) an FP digital-to-analog converter (FP-DAC) simplifies the pre-alignment logic, thereby reducing undesired power overhead throughout the FP process; 2) an FP analog-to-digital converter (FP-ADC) that substitutes uniform quantization steps with FP ones, eliminating redundant conversion power through adaptive quantization range; and 3) a hierarchical-hybrid structure (HHS) refines the balance between accuracy and energy efficiency in FP-CIM using a coarse-to-fine hybrid strategy. Fabricated in a 65-nm CMOS process, the prototype FP-CIM macro achieves 54.4 TFLOPS/W in BF16 mode and 130.9 TFLOPS/W in FP8 mode.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #5.1 / 08:30-08:55

张慧

北京航空航天大学

张慧，研究员，2008 年毕业于加拿大蒙特利尔大学理工学院电子工程专业。随后加入全球知名集成电路企业博通公司工作十余年，历任高级资深工程师、首席工程师、高级首席工程师、硬件设计经理及研发经理等职务。曾担任 IEEE Transactions on Circuits and Systems I（TCAS-I）AE。2021 年，张慧研究员加入北京航空航天大学集成电路科学与工程学院任职，并于同年入选国家级海外人才计划项目。当前团队主要面向通信与感知片上系统（SoC）开展研究，同时覆盖数模混合电路与射频电路设计等方向。

TALK

A 1.6-to-3.8GHz Reconfigurable FMCW Radar SoC with 81.5% Relative-Bandwidth PLL for Real-Time Life Detection in Disaster Response

A 1.6–3.8GHz FMCW radar SoC for real-time non-line-of-sight life detection is implemented in 40nm CMOS. An 81.5% BW ring-VCO PLL with DTC achieves 29.6kHz frequency error and 0.78–400MHz/μs chirp slopes. The TX integrates a 13.43dBm PA, while the RXRF features 8.1dB NF, baseband chain with 100dB-rejection SC-HPF at 1kHz and CT Δ-Σ ADC. A RISC-V core with FPU/VPU enables DSP, detecting people behind 6 walls and vital signs behind 2, occupying 7.65mm2 and consuming 0.395W.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #5.2 / 08:55-09:20

宗志锐

香港科技大学（广州）

宗志锐，香港科技大学（广州）助理教授，国家高层次青年人才，分别于荷兰代尔夫特理工大学、电子科技大学获得博士、学士学位，曾在 NXP 半导体、SiTime 公司担任高级研发工程师。主要研究方向包括射频毫米波集成电路、锁相环与时钟产生电路、高速数据互连电路等。

TALK

Self-Interference Cancellation in Millimeter-Wave Automotive Radar Receivers

Millimeter-wave (mm-wave) frequency-modulated continuous wave (FMCW) radars have become a key sensing technology in advanced driving assistance systems (ADAS). Same as the other full-duplex systems, the FMCW radar transceivers suffer from self-interference effects (also known as spillover). This talk presents an E-band receiver (RX) with spillover cancellation for frequency-modulated continuous-wave (FMCW) radars. To reject spillover from both TX-RX coupling and undesired reflections from radar assembly (such as bumper reflection), a spillover replication method based on frequency-delay translation through a single-sideband (SSB) modulator is introduced. To keep the RX performance immune from strong spillover, we propose an in-LNA common-mode voltage-domain canceller. It provides high isolation between the RX signal chain and cancellation path, minimizing noise figure (NF) degradation. Spillover is rejected in the input voltage domain before entering the critical LNA stage and inducing current, thereby preserving the linearity. Prototyped in 65-nm CMOS, the RX exhibits 5.7 - 7.2 dB NF and -11.4 dBm IP1dB across 69-76.5 GHz range. It demonstrates 38 dB rejection to spillover signals with offset frequency up to 3.6 MHz and power up to -10.4 dBm, while keeping the maximum NF degradation below 1 - 1.5 dB.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #5.3 / 09:20-09:45

楼立恒

中国科学技术大学

楼立恒，中国科学技术大学集成电路学院/微电子学院副研究员，上海海外高层次人才。博士毕业于浙江大学电路与系统专业，先后供职于国内外业界和学界从事芯片开发工作，负责多款用于雷达和通信的系统芯片研发，包括毫米波相控阵、混合 MIMO、FMCW/PMCW、UWB 通感一体，以及光模块芯片，其中包括导航定位、NB-IoT 和光通收发等芯片等量产；多项原创架构和成果发表于 ISSCC、RFIC 及 JSSC、TMTT 等 IC 领域顶级会议和期刊，并多次受邀于 ISSCC 现场演示芯片系统原型。目前研究方向为高速和高频集成电路设计，涵盖先进工艺下数字化、阵列化、多模融合与通感一体技术和架构的实现，面向高阶调制的高速光电融合收发接口芯片开发，以及支持高频/高速宽带应用的先进封装和接口的研发。

TALK

A 128mW 2×4 Radar-on-Chip with Forward-ΔΣ DPLL-Locked Multi-Injection RTWO in 22nm CMOS Enabling ADC-Free Digitization and PS-Free Beamforming Demonstrated in In-Cabin Vital-Sign Monitoring

A 2×4 phased-array SIL radar-on-chip in 22nm CMOS is demonstrated for in-cabin vitalsign monitoring. Built on a forward-ΔΣ DPLL-locked multi-injection RTWO at 20GHz, it concurrently serves as (de)modulator, beamformer, and data converter. The chip delivers 0dBm CW/PMCW for respiration cancellation, boosting SFDR by 9dB for cardiac extraction. RTWO-based beamforming covers ±48° FoV in ~15° AoA step. The 1.42mm2 chip consumes 128mW and achieves RR/HR errors <±6bpm with 1.2mW DSP on-chip

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #5.4 / 09:45-10:10

于锐

华为新加坡研究所

Rui Yu (Senior Member) received the Ph.D. degree in ECE Dept., National University of Singapore, in 2007. He is currently a RFIC design lab director with Huawei Singapore Research Center. His research interests are in the area of RF and mixed-signal IC design for connectivity wireless and wireline applications.

TALK

A NearLink 2.0 Compliant Dual-Band RF Transceiver for Smart Wireless Personal Audio Applications

This work presents a NearLink 2.0-compliant dual-band RF transceiver. Compared with traditional BT/BLE counterparts, this design achieves receiver figures of merit (FOM) of 188.7dB in the 2.4GHz band and 185.2dB in the 5GHz band, exceeding the state-of-the-art by >4dB. Furthermore, it demonstrates a 30.9% 2.4GHz-transmitter system power efficiency with exceptional EVM performance: 3.3% in 3Mbps BT Enhanced Data Rate mode and 3.64% in 4M-16QAM NearLink 2.0 mode (16Mbps).

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #6.1 / 08:30-08:55

陈虹

清华大学

陈虹，清华大学集成电路学院，教授，博导，国家级高层次科技创新领军人才。IEEE 高级会员，IEEE 异步电路国际会议（ASYNC）2023 年大会主席，IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) 副主编，Tsinghua Science and Technology 客座主编。研究方向为极低功耗电路与系统设计，包括异步电路设计、亚阈电路设计、异步脉冲神经网络加速器等，部分成果已产业化。拥有发明专利 40 项，发表国内外期刊及国际会议论文 140 余篇，3 本学术专著。荣获 IEEE ISCAS2013 最佳演示奖，IEEE ASYNC2021 和 ASYNC2023 最佳论文提名，ICCBD+AI2024 最佳论文。2016 年国家级教学成果奖二等奖，2017 中国电子学会科学技术奖二等奖，2019 年北京医学科技进步三等奖，2020 年中华医学科技进步三等奖，2020 年北京市科技进步一等奖，2023 年国家科技进步二等奖。2018、2019 国际大学生类脑计算大赛优秀指导教师等。

TALK

ANP-OT: A 0.17nW/Synapse 0.46pJ/SOP Neuromorphic Olfactory Processor with On-Chip Transfer Learning for Non-Invasive Cross-Hospital Cross-Pulmonary-Disease Diagnosis

This paper shows the first olfactory processor with on-chip transfer learning for cross-hospital and cross-pulmonary-disease diagnosis, which achieves >94% pulmonary disease detection accuracy at 3 different hospitals. This work achieves a 0.46pJ/SOP energy efficiency, and a power density of 0.17nW/synapse.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #6.2 / 08:55-09:20

岳金山

中国科学院微电子研究所

岳金山，中国科学院微电子研究所副研究员，博士生导师。主要从事高能效存内计算架构与人工智能芯片研究，在固态电路与体系架构领域的重要期刊、会议发表论文 80 余篇，包括 JSSC、ISSCC、VLSI、DAC 等。主持国家自然科学基金青年项目、重大研究计划重点项目课题等，入选中国科学院引才计划青年项目、国家“博新计划”、北京市科技新星，担任 A-SSCC、DAC、ICCAD 技术委员会委员。

TALK

A 28-nm Computing-in-Memory Processor With Zig-Zag Backbone-Systolic CIM and Block-/Self-Gating CAM for NN/Recommendation Applications

Computing-in-memory (CIM) chips have demonstrated promising energy efficiency for AI applications such as the neural networks (NN), Transformer and recommendation system (RecSys). However, several challenges still exist. First, a large gap between the macro and system level CIM energy efficiency is observed. Second, several memory-dominate operations, such as embedding in RecSys and non-linear functions in NN/Transformer, require heavy off-chip access. This work presents an energy-efficient CIM-CAM processor for both NN and RecSys applications with three main innovations. First, we propose a reconfigurable Zig-Zag memory access structure, enabling flexible adjacent connections between SRAMs and CIM arrays to minimize SRAM access power. Second, a backbone-systolic CIM array is implemented to avoid long accumulation path with better data reuse between CIM macros. Third, a distribution-aware block/self-gating CAM is proposed to reduce off-chip access and on-chip search power for the memory-dominant embedding operations in RecSys. The fabricated 28nm CIM-CAM chip achieves 37.9-81.5TOPS/W for NN and 12.3-56.1nJ/request for RecSys, and highlights the improvement of system/macro efficiency ratio (SMER) by 9.2% over the trendline of the state-of-the-art system-level CIM processors.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #6.3 / 09:20-09:45

贾弘洋

清华大学

贾弘洋，清华大学电子工程系副教授、博士生导师，于 2014 年在清华大学获得微电子学学士和经济学第二学士学位，并于 2016 年和 2021 年在美国普林斯顿大学电子与计算机工程系获得硕士与博士学位。随后在普林斯顿大学和英伟达研究院担任博士后研究员，并于 2022 年 8 月加入清华大学电子工程系。研究重点为新兴计算技术及其与大规模集成电路和体系架构的融合优化，涵盖近似计算、存算一体、机器人计算加速芯片、隐私计算加速芯片等方向。在集成电路领域顶级会议与期刊 ISSCC、JSSC、VLSI 和 Hot Chips 上以第一作者或通信作者发表论文超 10 篇。担任 DAC、ESSERC、A-SSCC、JSSC 等多个 IEEE 系列会议、期刊技术委员会委员和审稿人，TCAS-I 特刊客座编辑。于 2022 年获得美国普林斯顿大学 Bede Liu 最佳电子与计算机工程博士论文奖，于 2024 年获得美国爱迪生专利奖。

TALK

Enabling Energy-Efficient Homomorphic Encryption Evaluation via Programmable In-Situ Computing

Privacy-preserving computing serves as the foundation for a wide range of emerging applications, including artificial intelligence of things and blockchain. Homomorphic encryption (HE), a novel privacy-preserving technique, enables computation directly on encrypted data without requiring decryption outside the data owner's domain. This approach provides mathematically provable security that surpasses traditional cryptographic methods, positioning HE as a promising alternative for privacy-preserving computing. However, the number-theoretic basis of HE introduces substantial computational and storage overhead, limiting its deployment on both cloud and edge platforms. In addition to these challenges, the increased size of ciphertexts creates communication bottlenecks for edge HE processing, as the energy required to transmit ciphertext from resource-constrained edge devices to the cloud can exceed available energy budgets. This work presents an HE accelerator with programmability for evaluation, encryption, and decryption, utilizing a circuit-architecture-software codesign methodology. The concepts of in-situ computing (ISC), defined as the chaining of HE operators, and digital in-memory computing (IMC) are leveraged to achieve energy-efficient HE processing. The challenges of programmable HE processing are analyzed, focusing on mismatches between HE dataflows and conventional von Neumann architectures. Subsequently, a multi-core HE accelerator architecture is introduced, integrating energy-efficient, high-density IMC HE cores with tightly coupled dynamic computation units, eDRAM bit cells, and data-swapping paths. Finally, strategies for scaling HE cores and integrating them with RISC-V CPU platforms are discussed.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #6.4 / 09:45-10:10

程伯骏

香港科技大学（广州）

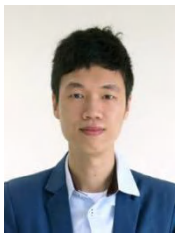
程伯骏，现任香港科技大学(广州)微电子学域助理教授。程伯骏本科毕业于中国科学技术大学少年班学院；硕士博士毕业于瑞士苏黎世联邦理工学院。他主要研究基于新型存储器件的类脑感存算集成电路，以及类脑计算算法和应用。他的研究成果发表于 Nature Electronics、ISSCC、VLSI、IEEE TCAS-I、IEEE TED 等会议及期刊，在类脑计算算法和应用领域在 IEEE TPAMI， ICLR (Spotlight)、ICML (Spotlight)、ICCV、CVPR、ICRA 等期刊和会议发表多篇论文。

TALK

SpikeRAM: A 48.1pW/Synapse/Bit Event-driven Spiking Compute-Near/In-Memory Processor with Neuromorphic Sensor Enabling Life-Long_x000b_On-Chip Learning

Edge perceptual SoCs increasingly demand high energy efficiency, strong privacy protection, and adaptability for real-world tasks involving power-hungry applications, sensitive data, and diverse users and environments. To address these requirements, we propose SpikeRAM, a neuromorphic sense–memory–compute system with on-chip learning, tightly integrated with an event vision sensor. SpikeRAM features three key characteristics: (1) Near-sensor computing with event-driven convolution operations. (2) One time-window triggered e-OTBP learning algorithm. (3) Gray-code encoded weights with ternary gradients for efficient on-chip learning. Benefiting from these designs, SpikeRAM achieves highly energy-efficient real-time inference with a power density of 48.1pW/synapse/bit. Meanwhile, it maintains over 90% learning accuracy while reducing learning memory and computational cost by more than 24 times, and decreasing the average memory programming times by 86.3%. The effectiveness of SpikeRAM is demonstrated on practical applications such as event-based signature verification.

INVITED TALK 邀请报告



2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #7.1 / 08:30-08:55

陈知行

澳门大学

陈知行，出生于中国澳门，2008 年获得美国华盛顿大学电子工程学士学位，并于 2012 年、2015 年先后在澳门大学取得硕士和博士学位。2016 年，他在美国加州大学洛杉矶分校任特殊科学家，2017 年起加入澳门大学，现为澳门大学模拟与混合信号集成电路全国重点实验室副教授，也是澳门大学粤澳模块化电路设计及测试联合实验室执行主任。他在集成电路领域成就显着，指导的模数转换器研究荣获 2024 年 IEEE 国际固态电路会议（ISSCC）“菅野卓雄优秀远东论文奖”。其微电子研究成果获得 2022 年中华人民共和国教育部高等学校科学研究优秀成果奖（自然科学奖）一等奖，并连续五届获得澳门科学技术发展基金技术发明奖。他本人于 2015 年获 IEEE 固态电路协会预博士成就奖，并于 2014 年作为共同作者获得欧洲固态电路会议最佳论文奖。其指导的学生也屡获殊荣，包括国家自然科学基金优秀青年科学基金（海外）、IEEE 固态电路协会预博士成就奖，以及亚洲固态电路会议学生设计竞赛杰出设计奖等。他现为 IEEE 高级会员，并担任 2026 年 IEEE 国际固态电路会议及 2023–2026 年亚洲固态电路会议技术评审委员会委员。他在数据转换器、时钟电路、带隙基準電路及飞时测距感测等领域共有超过 50 篇 ISSCC/JSSC 论文。

TALK

Reasons for "Not" Engaging in Analog-to-Digital Converter Research

Data converters are often regarded as the crown jewels of analog circuit design because they demand exceptional complexity and a broad foundation of interdisciplinary knowledge. Researchers in this field, such as Prof. Sun Nan and Prof. Li Qiang, are extremely smart (unlike the speaker of this talk😮‍💨). Hopefully, through this talk, you will find thought-provoking reasons to pursue data converter research. I will present some design examples to convince you. Believe me there.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #7.2 / 08:55-09:20

李学清

清华大学

李学清，清华大学电子系长聘副教授，中组部青千，IEEE/CCF 高级会员，本科和博士毕业于清华大学电子工程系，美国宾州州立大学的博士后。研究方向包括高性能数据转换器、新型存储和智能计算加速等，负责了多项国家自然科学基金委项目、国家重点研究计划课题、领域基金与企事业单位合作课题，所著教材获评北京市优秀教材，并指导学生获得了多份北京市和清华大学的优秀毕业论文。已发表多篇最佳论文（ASP-DAC/HPCA/TMSCS/IEEE Micro Top Picks 等）在内的百余篇学术论文，获评清华大学先进个人、周炳坤学者等荣誉，任职于 ISSCC、DAC 等国际会议的 TPC，以及 IEEE JSSC/JETCAS 等期刊 Guest Editor、IEEE TVLSI 和 IEEE TETC 等期刊编委（Associate Editor）。

TALK

A 16-bit 10-GS/s DAC Achieving >67dBc SFDR and <-77dBc IM3 up to the Nyquist in 28nm CMOS

This article presents an approach to mitigating both current source unit deviations and inter-symbol interference (ISI) non-linearities in Nyquist current-steering digital-to-analog converters (DACs). A 16-bit 10-GS/s DAC is designed in 28-nm CMOS and mounted in a BGA package. Measurement results show that this DAC achieves spurious-free dynamic range (SFDR) >70 dBc up to 2.86 GHz and SFDR >65 dBc with third-order intermodulation distortion (IM3).

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #7.3 / 09:20-09:45

黄琪枫

华为香港研究所

黄琪枫，2020 年本科毕业于中山大学电子与信息工程学院；2024 年博士毕业于香港科技大学电子与计算机工程系。我的研究方向为模数混合集成电路，如低功耗低噪 PLL、高精度 ADC。目前在华为港研所任职 Senior Analog Researcher。

TALK

A 5-MS/s 16-bit Low-Noise and Low-Power Split Sampling SAR ADC With Eased Driving Burden

This work presents a 16-bit 5-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) with the proposed split sampling (SS) technique. The SS decouples the sampling and conversion operations of the ADC, effectively addressing the tradeoff among the driving burden of the digital-to-analog converter (DAC), sampling noise, power, and bit cycling speed. The SS consists of 2 20-pF sampling capacitors and a 1-pF DAC. The sampling capacitors sample the input with low noise and cancel the kT/C noise of the DAC, avoiding the pre-amplifier saturation issue and easing the noise aliasing. As the sampling capacitors track the input when the DAC is performing bit- cycling, the input driving is eased with the extended tracking time. The small DAC guarantees fast speed and low power. Moreover, statistical residue measurement (SRM) is employed to reduce the pre-amplifie's noise and the quantization noise, efficiently improving the signal-to-noise-and-distortion ratio (SNDR) and the bit weight calibration accuracy. The ADC is fabricated in a 180- nm process and occupies an active area of 0.57 mm2. With the SS and SRM, the ADC samples at 5 MS/s and achieves a 93.7-dB SNDR with a 5.31-mW power consumption, yielding a high Schreier-figure-of-merit (FoM) of 180.4 dB.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #7.4 / 09:45-10:10

揭路

清华大学

揭路，清华大学集成电路学院副教授。 2017 年于浙江大学信息与电子工程学院获学士学位，2021 年于美国密歇根大学（University of Michigan）电气与计算机工程系（ECE）获博士学位，2022 年加入清华大学集成电路学院，获国家青年人才项目和北京市青年人才托举项目支持。主要研究方向为数模混合集成电路设计，重点包括高性能混合架构模数转换器（ADC）、数模混合电路设计自动化、可重构数模混合电路等。提出交织 NS-SAR、级联 NS-SAR 等 ADC 架构。目前已发表会议和期刊论文 30 余篇，担任 CICC、ASSCC、ICTA 会议 TPC，并担任 JSSC、OJ-SSCS、TCAS 等多个期刊的审稿人。

TALK

The Renaissance of Common-Gate Amplifiers: A High-Linearity Resistive-Input Pipe-SAR ADC Enabled by Continuous-Time Floating Charge Transferrer

Over the past decade of high-performance ADC research, novel common-source amplifiers, such as Gm-C, Ring-amp, and FIA, along with the transconductance (gm) based design philosophy, have held absolute dominance in the field. While this philosophy has achieved repeated breakthroughs in FoM, the intrinsic nonlinearity and PVT sensitivity associated with gm circuits remain commonplace challenges. This presentation discusses a fundamentally different design philosophy: native charge-domain circuits based on common-gate amplifiers, specifically Floating Charge Transferrer (FCT). It will explore the design paradigm shift that this circuit brings to ADCs, along with its various features and performance advantages. Finally, a resistive-input Pipe-SAR ADC based on CT-FCT will be discussed. At a sampling rate of 500 MS/s, this design achieves a linearity exceeding 90dB and a buffer-included FoM of 171 dB, while demonstrating robust PVT stability and circuit simplicity.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #8.1 / 10:30-10:55

张锋

中国科学院微电子研究所

张锋，中科院微电子所研究员，博士生导师。从事存储器及存算一体设计。

TALK

A 28-nm 88.3-TFLOPS/W POSIT-Approximate-Calculation-Based Digital Computing-in-Memory Macro Incorporating Final-Cycle Fusion and Joint Skipping

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #8.2 / 10:55-11:20

杜力

南京大学

杜力，南京大学集成电路学院教授，副院长，现任江苏省集成电路学会副秘书长，本科毕业于东南大学，硕士、博士均毕业于美国加州大学洛杉矶分校(UCLA)。曾在美国高通、耐能等公司分别从事人工智能芯片以及通信模拟前端芯片的设计，累计拥有 8 年多集成电路设计领域的工业界工作经验。现阶段主要从事 AI 处理器架构、存算芯片架构与编译部署优化方法的研究。在 IEEE 集成电路设计领域的权威期刊及行业顶级会议上发表论文 30 余篇，研究成果获 2021 年 IEEE 电路与系统协会达林顿（Darlington）最佳论文奖，现为 IEEE 电路与系统协会标准委员会 Domain-Specific Accelerators 组副主席，Sensory System，Machine-Learning Circuits and Systems 方向技术委员会成员。

TALK

RAC-NAF: A Reconfigurable Analog Circuitry for Nonlinear Activation Function Computation in Computing-in-Memory

The emerging computing-in-memory (CIM) architecture shows promise in efficiently processing deep neural networks (DNNs) by minimizing the data movement through analog in-memory computing. Unfortunately, the energy efficiency of CIM is still limited since it struggles to efficiently process the massive nonlinear activation functions (AFs) widely used in DNNs. In the current solutions, AFs require to be fulfilled in the digital domain with co-processors or lookup table (LUT). Therefore, a significant amount of data requires a round-trip conversion between the analog and digital domains at each AF process. The unavoidable analog-to-digital and digital-to-analog (AD/DA) conversions dominate the system's power consumption and reduce the overall energy efficiency. To address these issues, we propose a reconfigurable analog circuitry for nonlinear AF computation, named RAC-NAF. It is a pure analog circuitry that utilizes Taylor approximation (TA) to fit the arbitrary AFs, thereby reducing AD/DA conversions. To enhance the accuracy, RAC-NAF adopts a segmentation calculation method (SCM) based on the characteristics of nonlinear AFs. Moreover, the RAC-NAF provides the capability for reconfiguration to support various AFs and can be easily integrated with the existing CIM accelerators. The experimental results show that the proposed RAC-NAF significantly improves the performance of the CIM accelerators and reduces the energy consumption. When performing inference on various CIM accelerators, the energy consumption of AD/DA conversions can be reduced up to 12.31× , while the overall energy efficiency can be increased by 2.34× – 5.20× , and the accuracy loss is below 1%.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #8.3 / 11:20-11:45

司鑫

东南大学

司鑫，东南大学副教授，博士生导师，国家级青年人才；主要研究存内计算电路和存算 AI 芯片设计，累计发表集成电路领域会议期刊论文 60 余篇，其中包含 17 篇 ISSCC 和 11 篇 JSSC 等；主持多项国家级科研项目；目前担任 IEDM,A-SSCC 等国际会议 TPC。

TALK

A 28nm 127.54TFLOPS/W MXFP6 and 117.42TFLOPS/W MXFP8 Compute-in-Memory Macro with Adaptive-Preserved-Bit-Width and Serial-Dual-Bit-Sliding Schemes

Conventional FP-CIMs suffer from fixed preserved bit-width (PBW), limiting their adaptability and efficiency. This work proposes the firstMXFP-CIM macro enabling wide-range adaptive PBW, featuring: (1) A serial dual-bit-sliding scheme; (2) A harmless data mapping scheme with a hierarchical hidden-bit decoder; (3) An adjustable-PBW MXFP-MAC circuit via twin-stage allocation. The 28nm MXFP-CIM macro achieves a peak energy efficiency of 127.54 TFLOPS/W in the MXFP6/6 mode.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #8.4 / 11:45-12:10

于维翰

澳门大学

于维翰，博士，从 2009 年开始从事微电子研究。在 2010 年、2012 年和 2017 年分别获取澳门大学电机及计算机工程系的学士，硕士及博士学位。 2018 年起，于博士受聘为澳门大学濠江学者，并于 2019 年前往史丹佛大学担任访问学者，2021 年后回澳门后任教于澳门大学模拟与混合信号超大规模集成电路国家重点实验室。

于博士在澳门及国际上获得十多项荣誉奖项，其中包括 IEEE SSCS Pre-Doctoral Achievement Award、STGA Award 和澳门特别行政区科学技术发明奖。发表顶级学术论文近 50 篇，包括 12 篇 IEEE Journal of Solid-State Circuits (JSSC)和 7 篇 IEEE ISSCC。于博士现在是 IEEE SSCS Young Professional Committee，IEEE JSSC、T-CASI、T-CASII 等期刊审稿人、IEEE VLSI Mentor。

TALK

AFP-CIM: All-Inclusive Floating-Point With Segmented Compute-in-Memory Macro

This article reports an all-inclusive floating-point (AFP) with the segmented 8T-static random access memory (SRAM) compute-in-memory (CIM) macro. It features: 1) a segmented read-wordline (SRWL) to efficiently support the AFP formats including the AFP4/6/8/16 with all of the exponent–mantissa ratios (EMRs); 2) a bit-wise accumulation first (BWAF) circuit structure with a segmented in-memory accumulator (SIMA) for computing the parallel processing of the exponent and mantissa (Parallel-EM) to double the throughput of AFP operations; and 3) a reconfigurable weight-activation ratio (WAR) in AFP-CIM for supporting heterogeneous dataflow within CIM (HD-CIM) to minimize the external memory access (EMA) among various layers and models. Prototyped in 28-nm CMOS, the proposed AFP-CIM exhibits a peak throughput density of 0.9TFLOPS/mm2 and a peak energy efficiency of 22.7 TFLOPS/W with AFP4 operations. Evaluated with ResNet-50 and ViT-B for ImageNet classification, the AFP-CIM with HD reduces 90.2% and 43.3% EMA, respectively. It achieves the inference accuracy of 75.4% and 80.6% with the AFP4/6/8 operations, respectively.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #9.1 / 10:30-10:55

张奥扬

清华大学

张奥扬，清华大学集成电路学院副教授，博士生导师。2014 年本科毕业于浙江大学竺可桢学院，2020 年博士毕业于美国南加州大学（University of Southern California）电子与计算机工程系。2021 年至 2023 年在美国哈佛大学（Harvard University）从事博士后研究。2023 年加入清华大学集成电路学院任职助理教授。主要研究方向为 1）高能效可重构数模混合/射频集成电路设计，2）高性能计算和硬件安全集成电路设计。具体包括：高能效可重构数字无线收发机芯片设计，高效率数字功率放大器设计，模拟与数模混合计算芯片设计，可重构计算与硬件安全芯片设计。近年来在 ISSCC，VLSI，JSSC，Nature Electronics，Nature Communications 等国际会议和期刊发表论文 30 余篇，其中 ISSCC/JSSC 发表论文 16 篇。现任 ICCAD 2023/2024 技术委员会成员。曾获 IEEE SSCS Predoctoral Achievement Award，美国南加州大学电子系最佳博士论文奖，Ming Hsieh Institute Scholar 等奖项。

TALK

SharpSAT: A Heuristic-Learning-Based SAT Accelerator Achieving 0.8µs/16.1µs Solution Time in SAT/UNSAT Cases

The Boolean satisfiability (SAT) problem, as a foundational NP-complete problem, stands at the epicentre of modern computational logic, serving as the critical engine for high-stakes applications such as hardware formal verification, cryptographic analysis, and AI planning. While the demand for high-speed SAT solving is paramount, traditional software solvers are often bottlenecked by exponential search spaces, and existing ASIC accelerators frequently rely on local search heuristics that are inherently incomplete—meaning they cannot provide the mathematical guarantee of unsatisfiability (UNSAT) required for rigorous system validation. To address these limitations, this paper proposes SharpSAT, a high-performance complete SAT accelerator that integrates a heuristic-driven learning architecture to systematically prune the search space. By implementing a rapid conflict-driven clause learning (CDCL) unit to prevent redundant variable flips and a dedicated dual-BCP engine to accelerate the primary computational bottleneck of Boolean constraint propagation, SharpSAT achieves a sophisticated balance between exploration and exploitation. Furthermore, its smart assignment strategy introduces strategic randomness to diversify the search without compromising completeness. Fabricated in a 28nm CMOS process, the SharpSAT prototype demonstrates superior efficiency, reaching average solution times of 0.8 µs for SAT and 16.1µs for UNSAT cases for instances with 50 variables and 218 clauses. This architecture achieves a 70.67x and 6.17x speedup over the MiniSAT software solver on SAT/UNSAT tasks respectively, while outperforming prior complete hardware accelerators by up to 21.11x, establishing a new benchmark for hardware-accelerated automated reasoning.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #9.2 / 10:55-11:20

郭衍束

上海交通大学

郭衍束，上海交通大学集成电路学院副教授，入选国家青年人才计划。2021 年毕业于清华大学集成电路学院获博士学位。2021-2026 年在新加坡南洋理工大学电气与电子工程学院集成电路与系统中心任博士后研究员。主要从事超低温、高能效集成电路研究，研究方向包含面向量子计算的超低温专用集成电路、AI 驱动的低温芯片设计方法以及高能效无线收发机芯片等。近年来，在包含 ISSCC、JSSC 在内的集成电路设计领域权威期刊及国际会议发表论文 50 余篇。

TALK

A 174/756-nW 6-Class Keyword Spotting ASIC With Delta/Successive-Approximation Dual-Mode Quantizer

An ultra-low-power (ULP) six-class keyword spotting (KWS) ASIC is presented in this article, which can be used in always-on speech-based human–machine interface applications. The ASIC is composed of a sampling frequency and resolution adaptive (SFRA) dual-mode analog-to-digital quantizer and a power-gated KWS engine with a multiplier-less processing element (PE) array. The dual-mode quantizer mainly operates as a 1.5-bit delta quantizer (DQ), providing inherent robustness against dc drift. It adaptively switches to high-resolution successive-approximation register (SAR) quantization mode upon detecting a sound event based on the DQ output. In the KWS engine, the multiplier-less PE array is reused for both feature extraction and gated recurrent unit (GRU)-based keyword classification. To unveil the tradeoffs between power consumption and flexibility, two versions of the classifier have been implemented, with ROM-based on-chip weight memory (WM) and SRAM-based WM. Fabricated in 180-nm CMOS technology, the proposed KWS ASIC with ROM and SRAM-based WM achieves six-class classification accuracies of 87.3% and 90.1%, respectively, on the Google Speech Command dataset (GSCD) while consuming 174 and 756 nW long-term average (LTA) power with a decision latency of 14 ms at a clock frequency of 256 kHz.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #9.3 / 11:20-11:45

成凯

中国科学院微电子研究所

成凯，2024 年博士毕业于澳门大学 AMSV，现为中国科学院微电子研究所在站博士后。主要研究方向为硬件安全芯片、模数转换器芯片和时钟芯片设计。以一作/通讯累计发表 ISSCC 等会议期刊论文 5 篇。入选中国科学院特别研究助理资助，博士后海外引进等人才项目。

TALK

A 65nm 0.066pJ/bit Floating-Latch-Based True Random Number Generator Resilient to Power-Noise Injection Attacks

A floating-latch-based true random number generator (FL-TRNG) is presented that achieves an energy efficiency of 0.066pJ/b by leveraging a floating reservoir capacitor as its power supply. This architecture inherently offers strong resilience against power-supply noise injection attacks. Furthermore, current-starved inverters are employed within the latch to perform mismatch compensation and enhance PVT tolerance.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #9.4 / 11:45-12:10

董彦池

北京大学

董彦池，2018 年于哈尔滨工业大学获得学士学位，2021 年、2025 年先后于北京大学获得硕士、博士学位，现就职于华为海思。主要研究方向为智能芯片异构架构与电路设计、功耗建模与管理。

TALK

A Heterogeneous TinyML SoC With Systematic Minimum Energy Searching and Management for Keyword Spotting

This work presents a low-power heterogeneous TinyML SoC for keyword spotting with systematic minimum energy searching and management. Comprehensive fully synthesizable monitors are developed to be aware of the runtime energy, event, and performance for each computing block and guide the system-level minimum energy point (MEP) search. Hierarchical voltage regulation is designed with in-block power switches and on-chip switched capacitor regulators. Additionally, a 2-stage CIM-based event-driven wake-up scheme is developed to reduce the standby energy. Fabricated with 55nm CMOS technology, the systematic energy management approach obtains an average of 51% energy saving, which is 28% higher than a single block MEP management. Meanwhile, the SoC achieves a minimum power consumption of 3.5μW and a peak-to-idle power ratio of 30000×. Overall, the presented TinyML SoC is suitable for edge AI applications with state-of-the-art low-power features.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #10.1 / 10:30-10:55

邱浩

南京大学

邱浩，南京大学电子科学与工程学院副教授，国家级青年人才。南京大学本/硕，东京大学博士。以第一/通讯作者在 Nature Electron.、Sci. China Inf. Sci.、集成电路顶刊 IEEE JSSC、三大顶会 ISSCC、IEDM、VLSI 等发表论文 30 余篇，1 篇获得 ISSCC Silkroad Award，3 篇入选 ESI 高被引论文，单篇他引最高超 1000 次，入选爱思维尔中国高被引学者。申请美国/日本发明专利 4 项，中国发明专利 15 项，其中授权 5 项。曾获江苏省科学技术一等奖、中国安全生产协会安全科技进步二等奖、日本十大创新科技奖。主持国家自然科学基金重点项目、首批优秀青年（海外）项目、面上项目、是创新研究群体、重大项目的核心成员、参与科技部国家重点研发计划等项目。担任江苏省集成电路协会-模拟集成电路专委会副主任、日本应用物理学会-SSDM 技术委员会成员等，曾担任日本学术振兴会（JSPS）特别研究员、应用物理学会（JSAP）理事、电子情报通信学会（IEICE）《Electronics Express》编委。

TALK

A Galvanic Isolator Achieving 117-Mb /s Forward Data Transfer in the Presence of 181-kV/μs Common-Mode Transient Interference

Targeting a high data rate (DR) in the presence of common-mode transient (CMT) interference in the isolated gate driver application scenario, we presented an inductively galvanic isolator (GI) consisting of transmitter (TX) and receiver (RX) dies. To eliminate the destructive effects of CMT interference, an adaptive transconductance enhancement (ATE) technique was proposed on the TX side, which enables real-time detection of CMT events and contributes to an enhanced gm to stabilize the oscillator's operation. For the data transfer, we observed the problem of unequal data symbol durations using the conventional frequency-shift keying (FSK) demodulator, which can lead to shoot-through current or large reverse conduction loss. This problem was solved by the proposed compensated FSK demodulator. Both TX and RX dies in the proposed GI were fabricated in a 0.18 μm BCD process. Experimental results verified that the proposed GI demonstrates static CMT immunity (CMTI) up to 299 kV/μs. Furthermore, even in the presence of a severe CMT interference of 181 kV/μs, the GI supports a high DR of 117 Mb/s, corresponding to a data rate ratio (DRC) of 67 %, with a low bit error rate (BER) of 10-8. This extends the state-of-art by 3.72× in DRC and 1.24× in dynamic CMTI.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #10.2 / 10:55-11:20

黄沫

澳门大学

黄沫，于 2014 年分别在中山大学微电子学与固体电子学专业获得博士学位。2008 至 2014 年，任职于广晟微电子有限公司，作为项目经理参与了 TD-LTE，TD-SCDMA 等多款商用芯片的研发设计。2014 年 12 月至 2016 年 9 月，在澳门大学 AMSV 国家重点实验室任博士后。2016 年 10 月至 2019 年 8 月，任职于华南理工大学电子与信息学院，任副教授。2019 年 9 月至今，加入澳门大学 AMSV 国家重点实验室，现在担任副教授。主要研究方向为电源管理和能量 IC 设计。获授权 23 项中国发明专利，2 项美国专利。
黄沫博士获得了 ISSCC2017 营野卓雄远东杰出论文奖(中国大陆和港澳地区首次)，CICC2025 最佳论文奖。指导的博士生和博后获得 SSCS 博士成就奖（2 人次）、海外优青（1 人次）、优青（1 人次）。现担任 ISSCC 和 CICC 的 TPC 成员，以及 JoS，MEJ 的副主编。

TALK

Maximum-360MHz Coupled-OSC-based Converters Achieving 89.5% Peak Efficiency

This work proposes coupled-OSC-based high-frequency converters. Retaining gate-charge recycling in prior single-phase design, this work achieves inherent even phase interleaving, per-phase and per-inductor current balance. It reduces inductor count per phase, while enables high-speed ON-OFF control and improves load-transient performance by fast startup scheme. It achieves 89.5% peak PCE at 61MHz with air-core inductors, and 80% peak PCE and 1.82W/mm2 density at 360MHz using bondwire inductors.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #10.3 / 11:20-11:45

屈万园

浙江大学

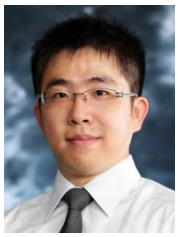
屈万园，浙江大学集成电路学院、工程师学院教授，国家级青年人才。博士毕业于韩国科学技术院（KAIST），2008 至 2017 年就职于韩国 LG 公司，于 2017 年起加入浙江大学，长期从事模拟集成电路设计相关研究工作，主要研究方向为面向三维异构集成的高密度电源管理芯片设计，包括混合电源拓扑的架构构建方法和优化理论、高动态电源环路的控制策略和驱动技术等。领导量产了多款国际领先的电源管理芯片，获授权美国专利 10 项、中国专利 4 项，韩国专利 5 项。发表集成电路设计领域最高水平国际固态电路会议（ISSCC）及固态电路期刊（JSSC）论文多篇，发表浙江大学首篇 ISSCC 论文，指导获评 ISSCC 2021 年度丝绸之路奖、ISSCC 2022 年电源管理亮点论文，目前担任多个 IEEE 高水平会议技术委员会成员。

TALK

A Compact 4Vin 93.4%-Peak-Efficiency 12A Load and 20mV Undershoot Resonant Sigma Converter with PCB-Embedded Converter-on-Substrate Packaging

This work presents a 4V input 12A load resonant sigma converter which consists of a 10MHz high-side switched-capacitor Buck (SCB) and a 5MHz low-side direct resonant switched-acapacitor (ReSC) converter. The proposed converter features a low V·A metric, a compact volume, and more importantly, a fast response by providing an ~0.5A/ns current slew rate during the transient. The measurements show 93.4% peak efficiency, 20mV undershoot under a 6A load step and 0.38A/mm2 system current density.

INVITED TALK 邀请报告



2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #10.4 / 11:45-12:10

姜俊敏

南方科技大学

姜俊敏，南方科技大学副教授，国家级和深圳市海外高层次人才，于 2011 年获浙江大学电子信息工程学士学位，于 2017 年获香港科技大学电子及计算机工程博士学位。于 2018-2021 年就职于美国德州仪器公司硅谷基尔比实验室，于 2021 年加入南方科技大学电子系。主要研究方向包括模拟与功率集成电路设计。在集成电路设计领域顶尖期刊和会议上共发表学术论文 50 余篇，包括 8 篇 ISSCC，8 篇 JSSC，拥有专利 40 余项，包括美国专利 8 项，与重点企业开展技术合作。2015 年获 ADI 公司杰出学生设计师奖；2017 年获 IEEE 固态电路学会博士生成果奖、2023 年获深圳市产业发展与创新人才奖、2024 年获南方科技大学优秀教学奖等。曾任 TCAS2 副编辑和客座编辑，现任 IEEE CAS Shenzhen Chapter 学会主席、CICC 技术委员会委员等。

TALK

5-1V DLDO-SC-Σ Converter

This talk presents a switched-capacitor (SC) sigma converter with a digital low dropout (DLDO) regulator and an auxiliary loop for efficiency improvement for high-density power delivery applications. The proposed converter has the input-series and output-parallel feature, and it consists of a hybrid SC converter on the high side for high density and high efficiency, and a DLDO on the low side for fast voltage regulation. To further improve overall efficiency, an auxiliary control loop is proposed to guarantee a minimized dropout voltage for the DLDO across a wide range of input and output voltages. The DLDO-SC-Sigma converter was fabricated in a 40 nm CMOS process. It can deliver 5 A maximum current from 3 to 5 V input to sub-1 V output and achieves a peak efficiency of 92%. A 1.6 μs response time and 36 mV voltage droop are achieved with a 2 A load transient. The converter achieves a system power density of 101.3 W/cm3.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #11.1 / 13:30-13:55

胡三明

东南大学

胡三明，东南大学教授，毫米波全国重点实验室副主任，紫金山实验室课题负责人。2009-2015 年历任新加坡 A*STAR 微电子研究院科学家、德国洪堡学者、英国爱丁堡赫瑞瓦特大学助理教授，曾短期访问剑桥大学及香港城市大学。主持国家自然科学基金重点项目、国家重点研发计划课题等。发表学术论文 190 余篇，包括 ISSCC、JSSC、TMTT、TCAS、TAP 以及多篇封面/封底等。获 IEEE 汇刊 CPMT 年度最佳论文奖（一作），并指导学生多次获最佳学生论文奖。入选中央网信办网信创新人才、优青、青千、江苏省杰青、双创人才等，获江苏省青年科技奖及“十大青年科技之星”称号。

TALK

A 140GHz Full-Duplex CMOS Transceiver with Metasurface-Integrated Self-Interference-Cancelling Antenna Supporting 16Gb/s 16QAM Dual-Mode Bidirectional Communication

This paper presents a 140GHz CMOS transceiver for both full-duplex and frequency-division duplex communication. By proposing self-interference (SI)-cancelling antenna and dual-polarized metasurface, the design achieves measured EIRP of 26.8dBm and SI suppression of >49dB, therefore relaxing the challenges at RF/digital domains. A 16Gb/s 16QAM simultaneous bidirectional communication over 1m is demonstrated, achieving the highest data rate reported for full-duplex dual-mode transceivers in the comparison table.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #11.2 / 13:55-14:20

周培根

东南大学

周培根，东南大学毫米波全国重点实验室副研究员，主要研究方向为毫米波太赫兹通信/雷达收发芯片及异质/异构集成技术，发表芯片方向论文 100 余篇，含芯片领域顶刊 IEEE ISSCC、JSSC 论文 8 篇，微波领域顶刊 IEEE TMTT、RFIC、IMS 论文 18 篇。兼/曾任多个国际会议分会场主席，IEEE JSSC、TMTT、TCAS-I 等 10 多个 SCI 期刊审稿人。主持江苏省科技重大专项项目课题、JKW 创新特区重点项目课题、JKW 创新特区主题项目、国家自然科学基金、江苏省自然科学基金、通信领域知名企业华为中兴预研项目等。

TALK

Integrated Transceiver Chip for Terahertz Communication and Sensing

With breakthroughs in silicon-based semiconductor technology and the development of the terahertz frequency band, a new generation of integrated communication and sensing technology has ushered in significant opportunities. This report focuses on cross-disciplinary innovation in terahertz communication and sensing, with emphasis on the design of miniaturized transceivers based on silicon-based processes. The unique ultra-wide bandwidth characteristics of the terahertz frequency band provide a physical foundation for high-precision physical sensing and ultra-high-speed data exchange, while silicon-based integration technology promotes the evolution of transceiver systems toward miniaturization. This report introduces a mode-tunable transceiver chip operating in the 180–230 GHz frequency band. The transmitter achieves a saturated output power exceeding 10.5 dBm and a 3 dB bandwidth greater than 50 GHz, while the receiver exhibits a single-sideband noise figure of 12 dB. A single-channel transmitter module delivers a peak equivalent isotropic radiated power (EIRP) above 28 dBm. In communication mode, the measured data transmission rate exceeds 16 Gbps using non-return-to-zero (NRZ) modulation. In sensing scenarios, based on stepped-frequency continuous-wave (SFCW) mode signals, the system achieves a range resolution better than 6 mm over a sweeping bandwidth of 40 GHz.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #11.3 / 14:20-14:45

郭浩

香港城市大学

郭浩，2020 年本科毕业于华中科技大学电子与信息工程专业，2025 年博士毕业于香港城市大学电子工程系。目前在香港城市大学太赫兹与毫米波全国重点实验室担任博士后研究员，主要研究方向为硅基毫米波与太赫兹相控阵收发机芯片设计。

TALK

A 436-to-472GHz 4-Element IF Beamforming Phased-Array Receiver in 65nm CMOS

This paper presents a 436-to-472GHz 4-element IF beamforming phased-array receiver in 65nm CMOS. A two-step mixing architecture reduces layout overhead. The LO frequency multiplier chain provides >-1dBm over 180 to 214GHz to drive the THz mixer. The 6-bit phase shifter covers 51 to 66GHz with 2.5° phase error. The on-chip stacked patch antenna array enables 10dBi gain and 91GHz 3dB gain-bandwidth. The receiver achieves ±35° scanning range, 36GHz system operating bandwidth and 27.5dB noise figure.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #11.4 / 14:45-15:10

江晨

复旦大学

江晨，复旦大学青年研究员，博士生导师。2010 年和 2013 年于复旦大学分别获得微电子学学士和微电子与固态电子学硕士学位。2018 年于美国康奈尔大学(Cornell University)电子与计算机工程专业获得博士学位。2018 年至 2021 年在美国联发科从事公司新一代无线通信芯片的研发工作。2021 年至 2023 年在美国创业公司 Lassen Peak 从事业界首个可实现电子扫描的低功耗便携太赫兹片上雷达系统的研发工作。2022 年入选国家和上海市海外高层次青年人才引进计划。2023 年加入复旦大学任教。江晨的主要研究方向为应用于感知、成像和通信的硅基太赫兹集成电路与系统的研究设计。

TALK

THz-TSI: A 0.33pJ/b 264Gb/s Through-Silicon Interconnect Module for 3D Integration Utilizing Terahertz Coupling

A through-silicon interconnect module for 3D integration utilizing THz coupling is presented, which achieves a record high data rate of 264Gb/s and efficiency of 0.33pJ/b. Both bi-directional point-to-point link and broadcast mode are successfully demonstrated. This scheme offers highly competitive bandwidth and density with significantly simpler fabrication and lower cost. Furthermore, its high flexibility enables real-time adjustable interconnect topology to effectively reduce latency.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #11.5 / 15:10-15:35

陈文华

清华大学

陈文华，教授，现任清华大学电子工程系长聘教授、北京信息科学与技术国家研究中心副主任、国家杰出青年基金获得者、IEEE-MWCL 编委，曾任 IEEET-MTT、RFMiCAE 等期刊编委。主要研究领域包括射频功放与线性化技术、集成毫米波与太赫兹电路等。2001 年在电子科技大学获学士学位，2006 年在清华大学获博士学位，2010 年至 2011 年在加拿大卡尔加里大学智能射频实验室从事博士后研究。承担国家 973、重点研发计划和国家重大专项等项目 20 余项，共发表学术论文 200 余篇，研制的射频功放和数字预失真算法在新一代宽频基站中获得规模应用，曾获 2018 年中国电子学会和 2021 年中国通信学会科技一等奖。

TALK

A 200-to-350GHz broadband SiGe BiCMOS Frequency Doubler with Slotline-Based Mode-Decoupling Harmonic-Tuning Technique

This talk presents the analysis and design of push-push frequency doublers (PPFDs) with second-harmonic source tuning for broadband terahertz generation. Using a simplified large-signal transistor model, we analyze the doubling mechanism and show that the second-harmonic input-controlled by the common-mode source impedance-significantly affects performance, particularly bandwidth. To achieve broadband operation, we introduce a source-tuning design scheme employing a mode-decoupling harmonic source/load-pull approach to determine optimal common-mode source and second-harmonic load impedances. A slotline-based second-harmonic source-tuning technique then realizes the desired impedance while enabling broadband input matching. As proof of concept. An H-band amplifier-doubler chain in 130-nm SiGe BiCMOS demonstrates 4.7-dBm saturated output power, 1.13% dc-to-RF efficiency, 37-dBc fundamental suppression, and only 3.6-dB power variation from 200 to 350 GHz.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #12.1 / 13:30-13:55

桂小琰

西安交通大学

桂小琰，西安交通大学微电子学院教授，博士生导师，IEEE 高级会员，陕西省中青年科技创新领军人才。博士毕业于加州大学尔湾(UC Irvine)，2008-2012 年在芯片设计公司 Broadcom 任设计工程师和主任科学家，现任陕西省电子器件与高端芯片重点实验室副主任，主要研究领域为高速有线通信/光通信接口芯片和无线通信集成电路设计。

在国际固态电路会议(ISSCC)、IEEE 固态电路学报(JSSC)等国际权威学术期刊和会议发表论文 70 余篇，授权中国发明专利 8 项，美国发明专利 1 项；近 5 年在主要研究领域主持国家自然科学基金等各类纵向科研项目和华为、中兴、阿里等企业资助，完成 112-Gb/s、200-Gb/s SerDes 收发机、112-Gb/s 全双工 SerDes 收发机系列芯片等国际领先研究成果，包括全球首款异质共封装的 200-Gb/s 收发芯片。获得国家级教学成果二等奖 1 项，陕西省高等教育教学成果特等奖 1 项，二等奖 1 项，华为技术有限公司火花奖 1 项，陕西省高等学校科学技术研究优秀成果二等奖 1 项。

TALK

A 112-Gb/s PAM4 SBD Transceiver with Mismatch-Compensated 2xVDD Hybrid and Two-Step Echo Canceller

A 112Gb/s PAM-4 simultaneous bidirectional (SBD) transceiver in 28nm CMOS is presented. It features a hybrid with a 2×VDD stacked driver to restore signal swing, a joint delay and slew-rate matching scheme to eliminate dynamic glitches, and a two-step echo canceller to mitigate reflections. The transceiver achieves BER < 1E-10 over a 12.7dB loss channel (equivalent to 24.4dB at Nyquist), with 1.73pJ/b energy efficiency and an FoM of 0.14pJ/b/dB.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #12.2 / 13:55-14:20

潘权

南方科技大学

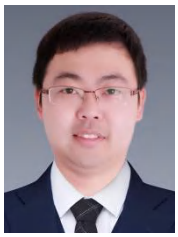
潘权，南方科技大学长聘教授，博士生导师。2005 年毕业于中国科学技术大学电子科学与技术系，获理学学士学位；2014 年毕业于香港科技大学电子及计算机工程学系，获哲学博士学位。主要研究工作集中在高速模拟/射频集成电路设计，主要包括：高速有线通信集成电路、光通信集成电路和硅光互连研究。作为负责人不仅在国际主流会议/期刊上发表 80 多篇高水平学术论文，同时有超过 8 年丰富的国内外工作经验，包括 4 年硅谷业界最前沿的工作经验。曾获得 IEEE 电路系统协会杰出青年作者奖，南方科技大学校长青年科研奖、优秀教学奖和优秀书院导师奖。

TALK

A 72Gb/s/pin Single-Ended Simultaneous Bi-Directional Transceiver with C-Peaking Leakage Cancellation and Dual-Loop Hybrid Impedance Calibration for Chiplet Interfaces

This paper presents a 72Gb/s/pin single-ended simultaneously bi-directional (SBD) TRX in 28nm CMOS. Capacitive peaking leakage cancellation (CPLC) suppresses the high-frequency leakage due to the main and hybrid driver mismatch in SBD links by 63%. Dual-loop hybrid impedance calibration reduces the coefficient errors of the hybrid circuits under PVT variations by 92%. The TRX achieves a 72Gb/s data rate with an eye-opening of 0.45UI and 243mV and an energy efficiency of 1.5pJ/b.

INVITED TALK 邀请报告



2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #12.3 / 14:20-14:45

杜源

南京大学

杜源，南京大学副教授，国家级青年人才计划获得者。本科毕业于东南大学，硕士、博士均毕业于美国加州大学洛杉矶分校(UCLA)。现阶段主要从事高速芯片互联与新兴异构计算方面的科研工作。在 IEEE 权威期刊及行业顶级会议上发表论文 60 余篇，包括 ISSCC、JSSC、TCAS-I/II、TVLSI、TMTT 等高水平国际期刊和会议，并获 IEEE 电路与系统协会达林顿（Darlington）最佳期刊论文奖，高速光电互联方面的相关研究成果入选“2025 年度中国第三代半导体技术十大进展”。

TALK

A 47.0Tb/s/mm 112Gb/s/pin PAM4 Single-Ended Transceiver Featuring 4-Aggressor Crosstalk Cancellation and Supply-Noise Tolerance for Short-Reach Memory Interfaces

This talk presents a five-lane 112Gb/s/pin four-level pulse amplitude modulation (PAM-4) single-ended (SE) transceiver for high-density short-reach interfaces. It features low-power front-end designs, including resistor-feedback amplifier (RFA)-based termination and triple equalization; 4-aggressor shape-fitting crosstalk cancellation (XTC) and supply-noise (SN)-tolerant clock distribution network are also proposed to improve signal integrity. The transceiver with the on-chip 2-mm channels is fabricated in 28-nm CMOS; it achieves an energy efficiency of 0.52 pJ/b and an edge density of 47.0 Tb/s/mm.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #12.4 / 14:45-15:10

张钊

中国科学院半导体研究所

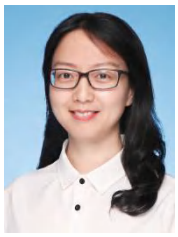
张钊，男，博士，中国科学院半导体研究所研究员，博士生导师。2022 年国家自然科学基金“优秀青年科学基金”获得者，2022 年入选中国科学院高层次人才引进计划。研究工作围绕高性能锁相环和时钟生成器、高速高能效光通信/有线通信收发器等高速高频集成电路设计技术的难点展开。近五年在相关领域共发表学术论文 80 余篇，包括 JSSC, ISSCC, VLSI 十余篇；主持多项国自然、国家重点研发计划、北京市科技计划、知名企业横向等项目；完成芯片设计与流片验证 40 余款，部分技术已用于产品中。担任知名 SCI 期《Electronics Letters》的编委。

TALK

Recent Research Progress on the PLL and CDR Forwireless/Wireline Communication

In this presentation, we will present two workspublished in ISSCC 2026. One is a 50-70-fs low-jitterPLL featuring a low-jitter performance over a widesupply range of 0.65-1V. The other one is a 112Gb/sPAM4 receiver incorporating the first reported over-100Gb/s referenceless PAM4 CDR.

INVITED TALK 邀请报告



倪熔华

复旦大学

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #12.5 / 15:10-15:35

倪熔华，复旦大学微电子学院研究员、博士生导师。2013 至 2020 年就职于国际知名半导体公司，从事射频收发集成电路及高速接口电路的研发与量产。2021 年至今的主要研究领域为高性能数模混合系统芯片的设计，包括：高性能振荡器、锁相环、频率综合器及时钟电路；高速串行数据接口电路及光电收发机的低功耗技术等。在 ISSCC、JSSC、CICC、VLSI、RFIC、MWTL 等会议及期刊发表 20 余篇论文。

TALK

A 21.6fsrms-Jitter, -260.7dB-FoM Fractional-N PLL Enabled by an Intrinsically Linear Variable-Slope SPD for Quantization Error Cancellation

This work presents a fractional-N PLL with an intrinsically linear variable-slope sampling phase detector for quantization error cancellation. Linearity, noise, and power efficiency are improved by eliminating the edge-restoration buffer. Combined with the proposed charge injection based nonlinearity compensation, the 14GHz prototype PLL achieves 21.6fs rms jitter, -260.7dB FoM and -67.4dBc worst-case spur in fractional-N mode with 18.1mW power consumption in 28-nm CMOS process.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #13.1 / 13:30-13:55

尹首一

清华大学

尹首一，清华大学教授，集成电路学院副院长，IEEE Fellow，国家杰出青年科学基金获得者，中国高被引学者。研究方向为可重构计算、人工智能芯片设计。 已发表学术论文 200 余篇，包括 ISSCC、VLSI、ISCA、MICRO、HPCA、DAC 和 IEEE JSSC、TPDS、TCSVT、TVLSI、TCAS-I/II 等集成电路和体系结构领域学术会议和权威期刊。出版《可重构计算》、《人工智能芯片设计》专著 2 部。曾获国家技术发明二等奖、中国电子学会技术发明一等奖、中国发明专利金奖、教育部技术发明一等奖、江西省科技进步二等奖、中国电子学会优秀科技工作者奖、中国电子信息领域优秀科技论文奖。现任集成电路领域国际会议 ISCA、MICRO、FPGA 和 A-SSCC 的技术委员会委员，《中国科学：信息科学》编委，国际期刊《ACM Transactions on Reconfigurable Technology and Systems》及《Integration, the VLSI Journal》的 Associate Editor。

TALK

A 28nm 47.3TFLOPs/W 894mJ/inference Visual Autoregressive Accelerator with Differential-Amplifier Speculation and Chain-Reaction-like Parallel Generation

To accelerate Visual Autoregressive (VAR) applications, this work implements a 28nm VAR accelerator achieving 47.3TFLOPs/W and <0.6% FID loss. A differential visual attention amplifier speculates critical tokens for selective execution; a full-path optimized MXINT PE adapts to biased data distribution; and, a chain reaction-like parallel generation exploits spatial correlation. The 5.76mm2 chip runs at 400MHz, accelerating DeiT/ViT VAR by 37.6× with 2.75TFLOPs/mm2 area efficiency.

INVITED TALK 邀请报告

窦春萌

中国科学院微电子研究所

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #13.2 / 13:55-14:20

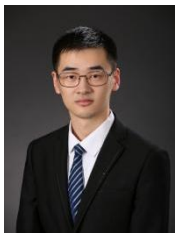
窦春萌，中国科学院微电子所研究员，博士生导师；2009 年本科毕业于南京大学，2014 年于东京工业大学取得博士学位；此后，先后在剑桥大学、中芯国际等地从事研究工作；2018 年加入中国科学院微电子所微电子器件与集成技术研发中心，主要从事新型非易失存算一体电路设计的研究工作；以第一/通讯作者发表 Nature Electronics、Nature Communication、JSSC、ISSCC、VLSI、IEDM 等具有影响力的期刊及会议论文，相关成果入选“2023 年度中国芯片科学十大进展”。

TALK

A 12nm 4Mb INT/FP4 Charge-Trap Transistor-Based Computing-in-Memory Macro Using Analog-Predict-Digital-Compute for AI Edge Devices

Previous nonvolatile CIM (nvCIM) macros suffer from low storage density, unnecessary multiply-and-accumulate (MAC) operations, and large hardware cost for floating point computations. A fabricated 12nm 4Mb CTT nvCIM macro supports INT/FP4 MAC operations with the analog-predict-digital-compute scheme for power saving, achieving an energy-efficiency of 137.75TFLOPS/W and >40 times improved density FoM (storage density×computing density). This work is the first 12nm CTT nvCIM design.

INVITED TALK 邀请报告



陈一鸣

清华大学

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #13.3 / 14:20-14:45

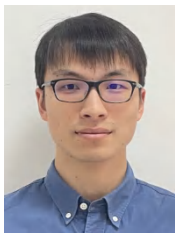
陈一鸣，2021 年毕业于清华大学电子工程系，获学士学位；2025 年于清华大学电子系获电子科学与技术专业工学博士学位。博士阶段从事存算一体架构的软硬件协同优化研究，现阶段核心研究兴趣为面向大语言模型的专用神经网络加速芯片设计，聚焦智算芯片领域的软硬件协同创新。

TALK

Hybrid SRAM/ROM Compute-in-Memory Architecture for High Task-Level Energy Efficiency in Transformer Models With 8928-kb/mm^2 Density in 28nm CMOS

This article reports the first ultra-high-density hybrid static random access memory (SRAM)/read-only memory (ROM) compute-in-memory (CiM) architecture for multibit multiply-accumulate (MAC) operations of transformer models. It features several techniques that enhance the on-chip weight density, energy efficiency, and flexibility, namely: 1) the hybrid CiM structure of 6T SRAM and 1T multi-level cell (MLC) ROM for ultra-high memory density to improve the limited on-chip memory capacity and alleviate the frequent weight reload from dynamic random access memory (DRAM); 2) 2-/5-b adaptive-resolution analog-to-digital converters (ADCs) for energy reduction and low accuracy loss; and 3) post-fabrication 1-of-4 capacitor selection (PFCS) to reduce the capacitance of computing capacitors, which was originally limited by the capacitor variation. This leads to lower energy and higher accuracy. A record-high 22-Mb ROM CiM and 896-kb SRAM CiM macro has demonstrated the 8×8 b MAC operations of one transformer layer, featuring ultra-high weight density of 8928 kb/mm2 and significantly reduced DRAM access activities toward high inference energy efficiency.

INVITED TALK 邀请报告



2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #13.4 / 14:45-15:10

朱浩哲

复旦大学

朱浩哲，复旦大学芯片与系统前沿技术研究院助理教授、博导。2022 年从复旦大学获博士学位。他的研究方向是面向前沿人工智能的集成电路和体系结构协同设计，包括具身智能专用芯片、三维空间计算芯片、多芯粒三维集成芯片系统等。

近年来已在相关领域高水平学术会议或期刊论文发表三十余篇，其中第一/通讯作者(含共同)论文包括 ISSCC、JSSC、MICRO、HPCA、DAC、A-SSCC、TCAS-1 等。获得 2024、2025 年 IEEE A-SSCC 杰出设计奖、2025 年 IEEE ICCAD 最佳论文提名奖等。

TALK

A 22-nm 109.3-to-249.5-TFLOPS/W Outlier-Aware Floating-Point SRAM Compute-in-Memory Macro for Large Language Models

Large language models (LLMs) excel at complex AI tasks but suffer from heavy overhead due to surging parameters, impairing AI processors' energy efficiency (EEF) and memory footprint. Compute-in-memory (CIM) relieves bandwidth bottlenecks and boosts EEF, yet INT/FP CIM variants face accuracy-memory trade-offs in LLM deployment. Outlier-aware quantization (OAQ), using low-precision formats for normal values and FP for outliers, becomes mainstream by matching full-FP accuracy.

This work presents OA-CIM, an SRAM-based digital CIM macro for hybrid BF16 outlier and INT4 normal value processing. Its key contributions are: (1) a LUT-based FP/INT-compatible MAC circuit; (2) an xor-sharing exponent gating scheme reducing latency/area via bypassing redundant comparisons; (3) a sparsity-aware readout circuit with distribution-offset weight encoding to cut bitline power consumption. A 22-nm 512-kB 8T SRAM prototype achieves 346.6 TOPS/W (INT4) and 249.5 TFLOPS/W (outlier mode), outperforming state-of-the-art mixed-precision CIMs by 2.7–3.1×.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #13.5 / 15:10-15:35

冯立琛

西安电子科技大学

冯立琛，西安电子科技大学，副教授。分别于 2014 年、2020 年获西安交通大学学士、博士学位。2020 年入职西安电子科技大学集成电路学院-模拟集成电路教育部重点实验室，隶属朱樟明教授课题组。
主要研究面向传感器端的智能化需求，基于模型-电路协同优化的轻量化人工智能芯片设计，主持国自然面上项目、青年项目，参与国自然-区域联合基金重点项目、科技部科技创新 2030 等课题研究。
相关研究以第一/共同作者身份发表 SCI 论文 10 余篇，包括 ISSCC、ASSCC、TCSVT、TCAS-I/II。

TALK

A 28nm 106.85TOPS/W and 77.68TFLOPS/W CIM Macro with Stage-Wise-Enabled Lossless Compressors Based on Sign-Bit-Embedded Transition-Counting-Lines for Edge-AI Devices

This paper presents a 28nm bit-parallel digital CIM macro with stage-wise-enabled lossless compressors based on sign-bit-embedded transition-counting lines, achieving 106.85TOPS/W (INT8) and 77.68TFLOPS/W (BF16).

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #14.1 / 15:45-16:10

王燕

清华大学

王燕，清华大学长聘教授、博士生导师。分别于 1988 年 6 月和 1991 年 6 月获得西安交通大学电子工程系工学学士学位和工学硕士学位，1995 年 4 月在中国科学院半导体研究所获得半导体物理与器件专业理学博士学位。1999 年进入清华大学微电子学研究所 CAD 技术研究室工作，2004 年晋升为教授。现为 International Journal of Computational Electronics 副主编、中国仿真学会集成微系统建模与仿真专业委员会副主任，EDA 开放创新合作协会技术管理委员会副主席，北京工业人工智能芯片器件-电路协同仿真技术重点实验室副主任。长期从事半导体器件建模与参数提取、射频毫米波集成电路设计等方面的工作。主持的“集成电路建模与仿真关键技术”(EDA)项目获得 2018 年中国仿真学会科技进步一等奖（排名第一）。现已发表论文 200 余篇，曾 7 次在重要国际会议上获得最佳论文奖，其中包括 CICC'2012，DATE'2018，RFIC'2024，ISCAS'2024 等。

TALK

A 14GHz Chopper-Refolding Sampling PLL Achieving 33.8fsrms and 80.8dBc Reference Spur with a kT/C-Noise-Cancellation SPD

A 14GHz chopper-refolding sampling PLL is implemented in 28nm CMOS, integrating a kT/C-noise-cancellation sampling phase detector (SPD) and a self-injection VCO with harmonic-impedance expansion. The SPD decouples jitter and phase-detection gain, while the chopper-refolding scheme filters flicker noise. The VCO enables a high FoM without manual tuning, achieving 33.8fsrms jitter, -80.8dBc spur, 16.9mW power, and competitive jitter performance among integer-N PLLs.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #14.2 / 16:10-16:35

邓伟

清华大学

邓伟，清华大学长聘副教授，入选国家高层次人才计划和国家青年人才计划。电子科技大学学士和硕士，日本东京工业大学博士，曾任美国苹果公司总部资深主任工程师，负责面向高速无线通信 SoC 的射频芯片设计。现任职清华大学集成电路学院，主要研究方向为硅基射频芯片设计与系统集成。现任/曾任 ISSCC、VLSI、RFIC、CICC、A-SSCC 和 ESSCIRC 的技术委员会成员，IEEE SSCS 杰出讲师，以及 IEEE JSSC、IEEE SSC-L、半导体学报等期刊副主编或客座编辑，负责射频和无线方向。在 JSSC、IEEE T-CAS I、IEEE T-MTT 等期刊以及 ISSCC、VLSI 等国际会议发表论文 160 余篇，其中在 JSSC 和 ISSCC 发表论文 40 余篇；主持射频芯片领域的多项国家重大科研项目。

TALK

Multi-Reference PLL: Theory and Implementation

The limitation of reference phase noise causes problems for the very low-jitter PLLs, which is increasingly critical and may be an impediment toward 10 fs jitter. This article presents a multireference PLL architecture featuring the ability to reduce reference PN by using more reference clocks. The architecture evolution, noise model analysis, and circuit design considerations are presented. The prototype of the multireference PLL is implemented in a 65-nm CMOS process and achieves 16.1 fs jitter.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #14.3 / 16:35-17:00

黄智强

香港科技大学（广州）

黄智强，教授，国家高层次青年人才计划入选者，于 2017 年取得香港科技大学博士学位，并获得 IEEE 固态电路学会博士生成就奖。博士毕业后在三星半导体（美国）从事 SerDes、WiFi 和 5G 毫米波收发机的研发工作，并于 2022 年加入香港科技大学（广州）微电子学域任教。研究领域包括模拟、数模混合、射频、毫米波和太赫兹集成电路设计。

TALK

A 14GHz Ring-Based 3rd-Order Fractional-N PLL with 164fsrms Jitter and a 100MHz Reference

This work presents a 14 GHz ring-based 3rd-order fractional-N PLL with 164fsrms Jitter and a 100MHz reference. A sub-sampling DLL is cascaded at a type-II PLL output for extra phase noise and supply noise suppression. A narrow-pulsed integrator is used in sub-sampling DLL to reduce integrated jitter. A tri-state polarity-reversible SSPD is used to reduce DTC range and bandwidth degradation. A delay calibration is used to reduce VCDL delay range and allow VCDL duty-cycle calibration.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #14.4 / 17:00-17:25

胡诣哲

中国科学技术大学

胡诣哲，现任中国科学技术大学教授，博士生导师，入选国家级青年人才项目（海外）。师从全数字锁相环（ADPLL）与数字化射频集成电路（Digital-RF）创始人 R. Bogdan Staszewski 教授，专注于数字化射频集成电路与架构的研究工作。他提出了“极低闪烁相噪数控振荡器”和“极低抖动电荷域全数字锁相环”技术，并系统性阐述了“振荡器闪烁相噪”与“超宽带频综相噪与杂散”机理。目前，他以第一作者或通讯作者身份发表 ISSCC/JSSC 8 篇，TCAS-I/OJSSCS/TCAS-II 7 篇，以及 VLSI/ESSCIRC/CICC 7 篇等若干高水平论文。胡诣哲教授曾担任华为海思技术顾问（兼职）和台积电技术顾问（兼职），拥有多项美国专利、欧洲专利局专利和 WIPO 专利，其研究成果已应用于华为基站芯片中。胡诣哲教授还担任 IEEE JSSC、TCAS-I/II、TMTT 等期刊的审稿人。

TALK

A PLL Technique: Charge-Steering Sampling

With the rapid arrival of AI and the 6G era, ultra-high-speed wireline/wireless technologies are becoming increasingly important. In this context, ultra-low-jitter integer-N and fractional-N phase-locked loop (PLL) chips play a critical enabling role. This report introduces a low-jitter all-digital PLL (ADPLL) architecture based on charge-steering sampling (CSS). The architecture integrates three key techniques: high-gain, high-linearity phase detection enabled by CSS; reduced quantization noise achieved through mid-rise encoding; and ΔΣ quantization-error compensation implemented in the charge domain using a capacitive DAC. As a novel charge-domain ADPLL solution featuring architectural simplicity and excellent performance, this technology shows strong potential for future wireline/wireless communication systems.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #14.5 / 17:25-17:50

李浩然

澳门大学

李浩然，2020 年获得电子科技大学学士学位，并于 2025 年获得澳门大学博士学位。他目前在澳门大学模拟与混合信号超大规模集成电路国家重点实验室（AMSV）担任博士后研究员。他的研究兴趣包括毫米波至太赫兹频率的产生、应用于高速有线和无线通信系统的锁相环设计，以及时钟产生与分配相关技术。他于 2025 年获得 IEEE 固态电路学会（SSCS）博士成就奖（Predoctoral Achievement Award）。

TALK

A Low-Jitter mm-Wave Fractional-N Sub-Sampling PLL Using a Polarity-Reversible SSPD for DTC Range Reduction

This talk presents a mm-Wave band fractional-N sub-sampling PLL that achieves an rms jitter of 57.9 fs and fractional spurs below -55.2 dBc at the near-integer fractional-N channel around 27GHz, corresponding to an excellent FoM of -249.7 dB. The proposed polarity-reversible sub-sampling phase detector reduces the digital-to-time converter range, improving its noise and nonlinearity performance, resulting in low in-band phase noise and fractional spurs.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 1

TALK #14.6 / 17:50-18:15

彭亚涛

澳门大学

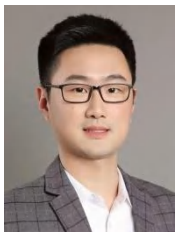
彭亚涛，2015 年于中国科学院微电子研究所获博士学位，2016~2021 分别在澳门大学，瑞士洛桑联邦理工学院从事博士后研究工作，2022 年至今为澳门大学微电子研究院助理教授。研究方向为低温电子学与面向量子应用的超低温集成电路。

TALK

A 17.9-to-22.4GHz 195.6±1.3dBc/Hz FoM Quad-Core Class-F-1 VCO Featuring Improved Synchronization Using a Circular Pentafilar Transformer-Based Tank

A 17.9-to-22.4GHz quad-core inverse-Class-F VCO achieving PN of -145.6 to -141dBc/Hz and an FoM of 194.3 to 196.9dBc/Hz is reported. The VCO features a circular pentafilar transformer tank that provides high Q1/Q2 without requiring extra CM resonators. Multipath synchronizations—in-phase at gates, out-of-phase at drains, and an auxiliary dualpath coil-equalize impedances at both f0 and 2f0. A segmented alignment technique is proposed to preserve 1D tuning with improved robustness against PVT variations.

INVITED TALK 邀请报告



2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #15.1 / 15:45-16:10

宋爽

浙江大学

宋爽，浙江大学集成电路学院研究员，博士生导师，于 2010 年和 2015 年分别获得荷兰埃因霍温理工大学混合信号集成电路设计专业的工程博士（P.D.Eng.）及博士学位。他于 2009 年至 2010 年在荷兰恩智浦半导体（NXP）担任模拟集成电路设计工程师；2015 年至 2020 年任职于欧洲时微电子研究中心（imec），担生物医疗集成电路与系统方向高级研究员。2020 年，加入浙江大学微纳电子学院任教。他的研究方向主要为模拟及混合信号集成电路、生理信号处理、生物医疗与物联网系统接口电路、数据转换器，以及电源管理和电池管理电路与系统，在国际主流学术期刊和会议上发表论文 50 余篇，并持有多项美国、欧盟及中国专利。他于 2019 年荣获集成电路领域国际顶级会议 ISSCC（国际固态电路会议）的优秀论文奖（Distinguished-Technical-Paper Award）。

TALK

Energy Efficient Amplifier for Driving Large Capacitive Loads

The presentation discusses a low-power two-stage amplifier for large capacitive load driving. A closed-loop gm -boosting stage with complementary devices is exploited to reduce the output resistance, and thus, makes the output pole non-dominant with minimum power overhead. Therefore, the amplifier has the dominant pole internally with a small capacitor, achieving a high gain-bandwidth (GBW). Meanwhile, a current-mirror-based slew rate (SR) enhancement circuit is implemented to increase the current driving capability. This circuit leverages the gain of a cross-coupled pair to generate an SR-enhancing current with a fixed ratio to its bias, featuring high PVT robustness compared with voltage-based enhancement. The proposed amplifier is implemented in a standard 55-nm CMOS technology, with an active area of 0.009 mm2. It achieves a GBW of 1.6 MHz with a 12nF CL , achieving an IFoMS of 9 84 615 that advances the state of the art by 1.4X. It provides an SR of 0.19V/μ s with an IFoML of 1 16 923, exceeding the state of the art by 2X. The excellent GBW and SR with a quiescent current of only 19.5 μA make this amplifier suitable for large capacitance driving applications.

INVITED TALK 邀请报告

聂凯明

天津大学

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #15.2 / 16:10-16:35

聂凯明，博士，教授，国家级青年人才，主要从事高端 CMOS 图像传感器芯片设计与模拟集成电路设计与研究，负责和领导设计完成十余款大规模高端 CMOS 图像传感器芯片。 主持包括国家重点研发计划课题、国家自然科学基金联合基金重点项目、国家自然科学基金面上项目和青年项目在内的科研项目 10 余项。作为第一作者或通讯作者发表在本领域高水平期刊 IEEE JSSC、IEEE TCASI 和 IEEE TCASVT 上在内的学术论文 40 余篇，获得中国发明专利授权 10 余项，获得美国发明专利授权 2 项。获评 2018、2022、2023 年天津市科技进步一等奖、2023、2024 年中国国际大学生创新大赛国家级金奖指导教师等荣誉。

TALK

A 140-dB Single-Exposure Wide-Dynamic-Range CMOS Image Sensor Combining LOFIC and Selective Overflow Technology

This report presents a wide-dynamic-range (WDR) CMOS image sensor (CIS) integrating lateral overflow integration capacitor (LOFIC) technology and selective overflow architecture, achieving a 140-dB dynamic range (DR) in a single exposure. The proposed pixel architecture modulates the barriers of overflow paths to enable saturated charges overflow through two distinct pathways: effective overflow (captured by LOFIC) and ineffective overflow (discharged via VDD). This unique selective overflow mechanism equivalently enhances the charge storage capacity of the LOFIC capacitor, strengthening high-light detection capabilities and thereby extending DR. In addition, we propose a count-range-selectable single-slope (SS) analogto-digital converter (ADC) circuit to resolve the dual-channel readout issue caused by inconsistent readout sequences between high-gain and low-gain signals in LOFIC architectures. This design achieves single-channel readout while maintaining digital correlated double sampling (DCDS) functionality. The prototype chip is fabricated using an 110-nm backside illumination (BSI) CIS process, featuring a 5×5 μm pinned photodiode (PPD) pixel and a 14.32-fF LOFIC capacitor. Compared with conventional LOFIC architectures, the proposed selective overflow mechanism extends DR from 101 to 140 dB, with a switching-point signal-tonoise ratio (SNR) of 20.5 dB. By selecting appropriate overflow gate parameters, the photo-response non-uniformity (PRNU) at the half-full code for the high-conversion-gain (HCG) output is measured at 0.50%, while PRNU for the low-conversion-gain (LCG) output is 0.89%. At an ambient temperature of 60 ◦C, the dark current of the HCG signal is 181 e−/s, and that of the LCG signal is 621 e−/s.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #15.3 / 16:35-17:00

赵博

浙江大学

赵博，浙江大学集成电路学院副院长，长聘教授、求是特聘教授，国家级高层次人才，带领团队近五年共流片 40 余款芯片，应用于脑机接口、无源物联网、可穿戴设备、等等。牵头承担国家重点研发计划项目、国家自然科学基金重点项目、等等。获 IEEE 国际电路与系统协会顶级奖项“达林顿奖”、IEEE TCAS-I 最佳副主编奖、ISLPED 最佳芯片设计奖、等等。2022 年当选 IEEE 国际生医电路与系统技术委员会主席，并带领团队于 2023 年获得“杰出委员会”奖。2024 年入选被誉为“集成电路奥林匹克”的顶级国际会议 ISSCC 的组委会。担任芯片领域三大旗舰期刊 IEEE TCAS-I、IEEE TBioCAS、IEEE TCAS-II 的副主编，以及 IEEE 智能制造标准审查委员会委员。

TALK

A Battery-Free Wireless Electrochemical-Interface SoC Featuring 143dB Dynamic Range for Multimodal Wearables

A battery-free wireless electrochemical-interface SoC is implemented and demonstrated in a sweatband prototype for physiological monitoring in body sweat, where the proposed techniques improve the dynamic range with a high linearity and low power consumption: 1) A self-adaptive stepwise-sinking technique for an OTA-less potentiostat extends the dynamic range to 143dB with 23.3μW power. 2) A frequency-digital-hybrid structure helps to ensure a high linearity of R2=0.99997 across the 143dB range.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #15.4 / 17:00-17:25

赵健

上海交通大学

赵健，上海交通大学集成电路学院长聘副教授。围绕生物医疗、惯性导航等应用，开展高能效集成电路设计的研究工作。入选 IEEE 电路与系统协会杰出讲师（Distinguished Lecturer）、国家级青年人才计划。担任 IEEE TBioCAS 编委（2024-至今），曾任 IEEE TCAS-I 编委（2020-2023）。

TALK

Energy-Efficient and Environmentally Resilient Transceivers for Body Channel Communication

Body-Channel Communication (BCC) has emerged as a promising interconnect technology in Wireless Body-Area Networks (WBANs), offering advantages such as low transmission loss and enhanced physical security. This tutorial provides a comprehensive overview of BCC transceivers (TRXs), beginning with the fundamental principles of BCC and channel modeling techniques. It then delves into design methodologies for highly energy-efficient and environmentally robust TRX circuits, covering both narrowband and wideband implementations. Additionally, measurement techniques and future research directions will be explored. This tutorial aims to equip designers of wearable healthcare SoCs and other low-power WBAN devices with practical insights and technical expertise.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #15.5 / 17:25-17:50

罗宇轩

浙江大学

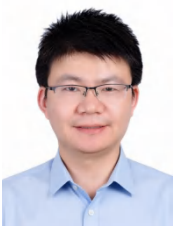
罗宇轩，2014 年获得电子科技大学学士学位，并于 2018 年获新加坡国立大学博士学位。2018 年至 2020 年，他在新加坡国立大学从事博士后研究工作，现任浙江大学集成电路学院百人计划研究员，他的研究方向主要为高精度集成电路设计。罗博士目前担任 IEEE 亚洲固态电路会议（A-SSCC）和 IEEE 国际集成电路技术与应用会议（ICTA）技术程序委员会委员，并于 2024 年起担任 IEEE 电路与系统学会职业发展中心主席，于 2018 年获得新加坡工程师学会（IES）杰出工程奖，于 2024 年入选浙江省高层次科技人才，于 2025 年入选国家级青年人才。

TALK

Energy Efficient Sensor Interface for Digital Microphones

With the rise of voice-enabled applications, digital microphones are increasingly demanded for both high performance and ultralow power consumption. However, power consumption of a sensor interface circuit typically trades off with its key performance metrics such as dynamic range (DR). This presentation reports a co-optimization methodology for MEMS-ASIC design that employs electrostatic force feedback to effectively decouple this trade-off. Through co-optimization of the MEMS transducer and the readout interface at the system level, the proposed solution achieves a wide dynamic range of 107 dB while drawing only 430 μA of supply current.

INVITED TALK 邀请报告



2026 年 3 月 26 日 · 第 2 天

宴会厅 2

TALK #15.6 / 17:50-18:15

黄张成

复旦大学

黄张成，复旦大学研究员，博士生导师，国家级青年拔尖人才。南京大学本科毕业，在中科院上海技术物理所获博士学位。当前主要研究方向为感知计算融合芯片、深低温电路设计和物理 AI 计算等，主持有国家自然科学基金等国家/省部级项目十余项，承担了国家重大项目的关键芯片研发任务，近三年以第一/通讯作者在 ISSCC、DAC、CICC、Nature 子刊、IEEE TCAS 等一流会议/期刊发表文章十余篇，独立研制几十款高性能传感专用集成电路芯片，在风云三号/四号气象卫星、天宫二号载人空间站、环境卫星、海洋卫星等我国多项航天遥感重大型号载荷中成功在轨应用。

TALK

A 128×96 Multimodal Flash LiDAR SPAD Imager with Object Segmentation Latency of 18μs Based on Compute-Near-Sensor Ising Annealing Machine

This paper presents a 128 × 96 multimodal flash LiDAR SPAD imager integrated with a compute-near-sensor Ising-model annealing processor for dynamic object segmentation, framed as a combinatorial optimization problem. The proposed system enables real-time updates of Hamiltonian coefficients using a high-bandwidth output-while-write scheme, and accelerates Ising spin iterations by exploiting multimodal SPAD information, achieving a remarkable segmentation latency of just 18 μs.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #16.1 / 15:45-16:10

詹陈长

南方科技大学

詹陈长，分别于 2004、2007、2011 年获复旦大学学士、硕士、香港科技大学博士学位。2006 至 2007 年在上海芯原微电子有限公司担任实习模拟 IC 设计工程师，2011 至 2012 年担任香港科技大学博士后，2012 至 2014 年在美国高通公司担任高级工程师，专注于为下一代移动设备研发高性能电源管理芯片。2014 年加入南方科技大学，现为微电子学院副教授。主要研究领域为电源管理和能量收集 IC 及系统的分析、设计，迄今为止发表了 1 本专著及 100 多篇学术论文，获授权 23 项中国专利、6 项美国专利。

TALK

A Light-Load Optimized Dual-Output Fly-Buck Converter With an Implicit Feedback of the Isolated Output

This paper presents a 100 V fly-buck converter with limited zero-current (ZC) time and implicit feedback of isolated output in discontinuous conduction mode (DCM). An anti-noise pre-regulator is developed to resist the noise and generate stable internal supplies during high-voltage switching. A ZC-time limitation scheme is designed to adjust the maximum ZC time in DCM, such that the lowest switching frequency in DCM is confined, and the charging frequency of the isolated outputs is guaranteed. The light-load efficiency can be improved with a lower switching frequency than working in the classical forced continuous conduction mode (FCCM). Yet, the isolated output voltage seriously drops with the load in ZC time-limited DCM, due to the loss of regulation. Therefore, an enhanced ontime generator (EOTG) is further introduced to generate adaptive on-time without requiring direct input or output voltage information, while realizing implicit feedback of the isolated output in DCM. The on-time is increased with the enlarged load of the isolated output, improving the regulation of the isolated output in ZC-time-limited DCM. The implemented fly-buck converter prototype was fabricated in a 100 V 0.18 μm BCD process. Up to 24% light-load efficiency improvement is achieved at VIN = 48 V with a 25 μs ZC time limitation. The measured peak efficiency is 94.4% with a 24 V input voltage.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #16.2 / 16:10-16:35

潘东方

中国科学技术大学

潘东方，中国科学技术大学教授，入选国家级青年人才项目。主要从事功率与射频集成电路设计研究，主持国家自然科学基金联合基金重点项目等。在国际会议和期刊上发表论文 50 余篇，其中以第一作者在集成电路设计领域顶会 ISSCC 和顶刊 JSSC 发表论文 7 篇，并以第一/通讯作者在 IEEE TMTT、TCAS-I、CICC 等期刊和会议发表论文 20 余篇。现为 IEEE 高级会员，担任 IEEE ICTA 技术委员会成员、分会场主席及《微电子学》青年编委等职务。

TALK

A 24V-to-20V Isolated DC-DC Converter using a Transformer-Based Supply-Generating Technique

This report presents a 24V-to-20V isolated DC-DC converter featuring a transformer-based supply-generating technique for efficient gate-driver power delivery. Unlike conventional high-voltage inverters that rely on auxiliary LDOs or buck converters, the proposed approach directly generates a 5 V supply from an auxiliary coil coupled to the primary winding, eliminating external power components and reducing system complexity. The transmitter (TX) and receiver (RX) are fabricated in a 0.18 μm BCD process and packaged in an LGA package. Measurement results demonstrate a peak efficiency of 73.2% and a power density of 36.5 mW/mm^3. Compared with prior integrated solutions, the proposed converter achieves a 13.2% efficiency improvement and meets the CISPR-32 Class B EMI standard on a two-layer PCB without stitching capacitors.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #16.3 / 16:35-17:00

陈映平

复旦大学

陈映平，博士生导师，2021 年入选国家海外高层次青年人才引进计划。2008 年于北京理工大学获得学士学位，2012 年于中科院微电子所获得硕士学位，2020 年于美国德克萨斯大学达拉斯分校(The University of Texas at Dallas) 电子工程专业获得博士学位，2020 年至 2021 年在比利时欧洲微电子中心 IMEC 进行博士后研究。2012 年至 2015 年先后在北京希格玛微电子和戴乐格半导体等公司担任模拟设计工程师。主要从事基于 CMOS/BCD、氮化镓(GaN) 等工艺的模拟/功率集成电路设计，包括 DC-DC converter，AC-DC converter, LDO 等。

TALK

A Closed-Loop EMI Regulated GaN Power Converter with 500MHz-Sampling-Bandwidth In-Situ EMI Sensing and 9kHz-Resolution Global Excess-Spectrum Modulation

As EMI standards evolve from the rules-based approach to the risk-based alternate, online EMI assessment and control become critical for lifetime risk management. Meeting such a trend, this article presents an online closed-loop EMI regulation for GaN power converter. Specifically, a wide-bandwidth in-situ EMI sensor is integrated to characterize the noise through autocovariance-based spectrum analysis. With a stepwise random space sampling, it significantly compresses the sensing time without sacrificing the accuracy for real-time EMI spectral characterization. Based on the online measured noise, a global excess-spectrum modulator is devised to adaptively track and hence continuously regulate the maximum excess noise. A prototype chip was fabricated in a 180nm BCD process, commanding two enhancement-mode GaN power switches at a nominal frequency of 2.8MHz. The measurement results show that the integrated in-situ EMI sensor can capture the EMI spectra with a 500MHz sampling bandwidth and 1mV sensing accuracy, while reducing the sensing time by over 25 times. Compared to the commercial spectrum analyzer, it demonstrates a maximum discrepancy of 3dB. The embedded global excess-spectrum modulator accomplishes a 9kHz-resolution EMI regulation, dynamically optimizing the EMI control.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #16.4 / 17:00-17:25

周泽坤

电子科技大学

周泽坤，作为项目责任人或主研人员完成多个国家自然科学基金、国家重点研发计划、国家重大专项、横向项目、中央高校基本业务费、省部级和总装预研项目等。项目涉及 DC/DC 变换器、AC/DC 变换器、LED 驱动、电池电量监测/充电管理、高品质音频放大器、光电集成、高速栅驱动及 PMU 等诸多热门领域，被广泛应用于汽车电子、医疗电子、平板电视/电脑、机顶盒、分布式供电系统、大尺寸 LED 屏幕、LCD 背光及低功耗通用 SoC、多模导航 SoC 等诸多产品中。

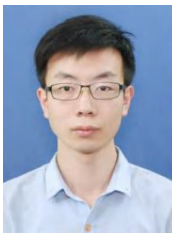
长期作为 IEEE 等领域内核心期刊及国家自然科学基金等评审，并在 IEEE Journal of Solid-State Circuits、IEEE Trans. Circuits Syst. I、IEEE Trans. Circuits Syst. II、IEEE Trans. Power Electron.、IEEE ISPSD、IEEE ISCAS 等国内外期刊及会议上发表论文 70 余篇；授权中国发明专利过百项、美国发明专利授权 6 项，合作编写专著 2 本。

TALK

A Condition-Insensitive Active SiC Gate Driver With On-Chip di/dt and dv/dt Sensing for Targeted Slew Rate Control

To address the longstanding challenges of segmented driving control in the control accuracy and load compatibility, this study introduces a condition-insensitive active silicon carbide (SiC) MOSFET gate driver, designed to achieve targeted control of di/dt and dv/dt slew rates. An innovative mixed-signal auto-timing (MSAT) technique employing the cascaded analog and digital delay lock loops (DLLs) is proposed for precise and flexible segment control. Furthermore, on-chip di/dt sensing with self-calibration, along with a low-power dv/dt sensing technique, enables the real-time slew rate monitoring during switching transients. The targeted slew rate control (TSRC) technique facilitates the adaptive closed-loop regulation of slew rates, ensuring compliance with predefined targets. Fabricated using a 0.18- μ m, 40-V bipolar-CMOS-DMOS (BCD) process, the proposed driver offers a tracking range for segment control of up to 156.7 ns, allowing independent control of di/dt (0.25, 0.35, and 0.45 A/ns) and dv/dt (5, 10, and 15 V/ns) targets across varied load conditions (400 V and 10 A, 600 V and 8 A, and 600 V and 12 A), achieving up to a 32% reduction in turn-on losses compared with conventional methods.

INVITED TALK 邀请报告



2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #16.5 / 17:25-17:50

张德生

华中科技大学

张德生，华中科技大学集成电路学院博士后，研究方向为宽禁带功率半导体器件驱动及其应用，主要聚焦于器件高速开关暂态的建模、调控、和多段式驱动芯片设计研究，致力解决开关损耗与 EMI 的折衷难题，围绕上述研究在 IEEE JSSC，IEEE CICC，IEEE TPEL，IEEE TCAS I 上发表多篇文章，申请国家发明专利多项。

TALK

An Adaptive Three-Stage GaN Gate Driver With Peak Miller Plateau Voltage Tracking and Voltage Tailing Suppression for 36.4% Switching Loss Reduction

Achieving low switching loss is critical for high-frequency gallium nitride (GaN)-based power converters due to the compact packaging and limited heat dissipation capacity of GaN devices. Focusing on minimizing the switching loss, this article proposes an adaptive three-stage gate driver (ATSGD) for GaN high electron mobility transistor (GaN HEMT). By providing a three-stage driving current within the Miller plateau (MP) stage, the proposed ATSGD can achieve a near-constant dV/dt, thus minimizing the switching loss under specific peak dV/dt constraints. Utilizing peak MP voltage tracking (PMPVT) and quick voltage tailing suppression (QVTS) techniques, the driver dynamically determines optimal switching timings for the three-stage driving currents in real time. Therefore, the extra losses caused by slow dV/dt start-up and voltage tailing effect are minimized under dynamic operation conditions. Fabricated in a 0.18 μ m bipolar-CMOS-double-diffused metal oxide semiconductor (BCD) process, the proposed driver reduces the total switching loss by 36.4% under 400 V/15 A with a peak dV/dt of 45 V/ns, benefiting from a 46.1% reduction in slow dV/dt start-up loss and an 88.7% reduction in voltage tailing loss compared with conventional gate drivers.

INVITED TALK 邀请报告

2026 年 3 月 26 日 · 第 2 天

宴会厅 3

TALK #16.6 / 17:50-18:15

杨佳成

澳门大学

杨佳成，博士，于 2021 年在电子科技大学获得学士学位，于 2025 年在澳门大学获得博士学位，目前在澳门大学模拟与混合信号集成电路全国重点实验室从事博士后工作，主要研究方向为高效率高功率密度电源管理芯片，混合型电源架构。杨佳成博士已在 ISSCC、JSSC、CICC 等期刊会议中发表多篇论文，并获得 IEEE 固态电路协会博士生成就奖。

TALK

A Multi-Phase Hybrid Converter with Q Samplers Enabling Simultaneous IL Auto-Balance and Arbitrary Phase Count

The paper presents a multiple-phase hybrid converter with Q samplers. Split-TON control enables VCF auto-balance and arbitrary phase counts under all-phase interleaving, while 0-V Q samplers support IL auto-balance with minimal reduction in power density. It achieves peak efficiencies of 90.5% and 91.5% at 1V and 1.8V VO. With 6-phase operation and ALL-ON control, the converter attains the lowest normalized undershoot. This method is extendable to other hybrid converters.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #17.1 / 08:30-08:55

王科平

天津大学

王科平，天津大学讲席教授，入选国家级高层次人才（WR）、国家级青年人才（QC）。主要研究方向为：射频/毫米波集成电路、硅基射频与微纳传感器异构集成电路、面向人工智能物联网的无线集成电路、面向脑机接口的神经调控集成电路与系统等。主持国家重点研发计划项目，国家自然科学基金联合重点项目，国家自然科学基金面上项目（2 项），科技委创新项目等国家级项目。曾获天津市科技进步一等奖、电子学会科技进步二等奖。发表 ISSCC 和 JSSC 论文 17 篇、IEEE 核心期刊（1/2 区）论文 45 篇；授权发明专利 20 余项。担任 IEEE AP/MTT/SS 天津联合分会副主席，中国电子学会青年科学家俱乐部理事，天津市集成电路行业协会专委会委员；担任 TCAS-II、MOTL、Microelectronics Journal、固体电子学研究与进展等期刊编委。

TALK

Reflectionless Blocker-Tolerant Mixer-First Receivers for 5G-Advanced/6G FR3 Communications

With the rapid evolution of next-generation wireless communication (e.g., 5G-Advanced, 6G), spectrum resources have become increasingly crowded. Compared to congested FR1 (sub-6GHz) allocations, The upper mid-band (FR3, ~6-to-24GHz) offers an order of magnitude more bandwidth, while avoiding the propagation penalties of mm-wave frequencies above 28 GHz. Recently, the reflection-based N-path mixer-first receivers designed for FR1 band have garnered widespread attention due to their capability to provide a tunable and frequency-selective bandpass response. However, the reflection-based out-of-band (OOB) rejection mechanism introduces two key implementation constraints. First, a trade-off exists between OOB rejection and switch size. Second, the OOB reflections can induce undesired standing waves, which degrade overall RF performance particularly in massive MIMO systems. To address these challenges, this talk focuses on reflectionless blocker-tolerant mixer-first receivers for next-generation wireless communications, covering frequency ranges of 6-to-26GHz and 10-to-30GHz.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #17.2 / 08:55-09:20

孟凡易

天津大学

孟凡易，天津大学微电子学院教授，万人计划青年拔尖人才，亚太工程组织联合会中国委员会委员。分别于 2011 年和 2016 年获得新加坡南洋理工大学本科和博士学位。主要研究方向为硅基 CMOS 射频/毫米波前端芯片和硅基-氮化镓异质集成芯片微系统，应用领域包含多波束通信、相控阵雷达、高密度电力电子等。发表学术论文 200 余篇，撰写英文专著 2 本，曾任 IEEE TCAS-II 副主编。2020 年获中国电子学会优秀科技工作者称号。

TALK

Design Practices of a 5G NR FR2 Low-noise Amplifier and a FR3 Power Amplifier

Recent wireless systems spanning 5G NR, 5G-Advanced, and emerging 6G are increasingly being architected to address both millimeter-wave (FR2) and mid-band FR3 spectra, imposing stringent—and often coupled — requirements on silicon RF front-ends. On the receiver side, ultra-wideband millimeter-wave LNAs are required to simultaneously support multiple 5G NR and NR-U bands with flat gain, low noise figure, and robust stability. On the transmitter side, FR3 PAs must deliver approaching watt-level output power and high efficiency while maintaining intrinsic harmonic containment and compact integration under tight silicon and thermal budgets.

Drawing from two recent JSSC works, this talk presents a set of circuit-level design and analysis practices for a 22.6 – 73.9 GHz ultra-wideband LNA and a compact FR3 CMOS SOI power amplifier. For millimeter-wave LNAs, synergistic equalization techniques combining shunt feedback, inductive peaking, and resonant feedback compensation are discussed, together with their analytical foundations for bandwidth extension, noise optimization, and stability control. For FR3 PAs, the focus is placed on transformer-based multi-way power combining, intrinsic harmonic termination shaping, and reliability-aware stacked transistor operation, highlighting how passive and active co-design can mitigate the efficiency–linearity–area trade-offs.

Beyond reporting measured performance, the presentation emphasizes practical design insights, including parameter sensitivities, layout–EM interactions, and reusable analysis frameworks that bridge circuit theory and silicon implementation. Collectively, these practices provide a unified perspective on wideband RF front-end design across FR2 and FR3, and offer concrete guidance for the development of future scalable, spectrum-aware 5G-Advanced and 6G transceiver architectures.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #17.3 / 09:20-09:45

王云

复旦大学

王云，复旦大学青年研究员，博士生导师，2019 年于东京工业大学取得博士学位，主要研究方向包括超宽带无线通信、毫米波相控阵、5G/6G/卫星通信集成电路。 任 IEEE ISSCC/AMPC/ICEPT/ICTA 会议 TPC 委员，IEICE ELEX 副编辑。

TALK

Ultra-Wideband Miniaturized RF Amplifier Integrated Circuit Design

To realize a smart society, fifth-generation (5G) wireless communication technology is one of the key technologies, 5G connects everything with high speed and low latency. In this report, RF amplifier integrated circuit designs for 5G Frequency Range 1 and 3 (FR1 and FR3) will be introduced. Multiple wideband design techniques are employed for a high-linearity, low-noise. The power amplifier (PA) and low-noise amplifier (LNA) both achieve a data-rate over 140 Gbps. This report provides a possible design direction of multi-band compliant 5G transceiver.

INVITED TALK 邀请报告

亓庚浈

中山大学

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #17.4 / 09:45-10:10

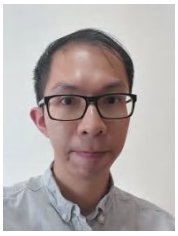
亓庚浈，2018 年在澳门大学获得电气与计算机工程博士学位。此后，在澳门大学模拟与混合信号超大规模集成电路全国重点实验室从事博士后研究。2020 年加入中山大学，现为微电子科学与技术学院副教授。2024 年成为 IEEE 高级会员。2016 年，在比利时鲁汶 imec 研究所开展了基于 CMOS SOI 工艺的射频可调谐前端模块设计研究。其主要研究方向为面向无线通信的 CMOS 射频集成电路，涵盖发射机、接收机、功率放大器及前端模块等领域。在固态电路期刊（JSSC）及国际固态电路会议（ISSCC）发表论文十余篇。

TALK

A Multi-Band RF Transmitter Employing a Transformer-Based N-Path Switched-Capacitor Modulator for CIM3 Suppression

A multi-band high-linearity radio frequency (RF) transmitter features a transformer-based N-Path switched-capacitor (SC) modulator to perform third-order harmonic (3x fLO) suppression, and tunable high-Q bandpass filtering to reduce the out-of-band (OB) noise emission. The intrinsic lowpass characteristic of the transformer also aids in suppressing the 3x fLO harmonic terms in the modulator, reducing the thirdorder cross-intermodulation product (CIM3) at the transmitter output. To enhance the transmitter efficiency and preserve the linearity, the power amplifier (PA) driver features a class-A/B transconductor (gm) parallelized with a gm linearizer biased in the triode region. Fabricated in 65-nm CMOS, the transmitter measures a power efficiency of 5.1% at a 2.3-dBm output, while showing CIM3 < −60 dBc and ACLR1 < −46 dBc. Over the 2-to-3 GHz RF bands, OB noise ≤ −157 dBc/Hz is consistently achieved, with power consumption between 30.8 and 34.3 mW. The active area is 0.21 mm2.

INVITED TALK 邀请报告



2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #18.1 / 08:30-08:55

阮家辉

澳门大学

阮家辉（Ka-Fai Un），分别于 2007 年在中国台湾台北的台湾大学获得电机工程学士学位，并于 2009 年及 2014 年在澳门大学（UM）取得电机与电子工程硕士及博士学位。

他曾于 2014 年在澳门大学担任博士后研究员，并于 2015 年担任讲师（UM Macao Fellow）。2017 至 2018 年期间，他以休假的方式赴爱尔兰都柏林大学学院（University College Dublin）电机与电子工程学院担任访问博士后研究员。自 2018 年起，他在澳门大学类比与混合讯号超大型积体电路国家重点实验室担任助理教授，现为副教授。

他的研究兴趣包括类比人工智慧（AI）电路、数位 A 加速器设计，以及类比与射频电路设计。2003 年，他代表得澳门参加国际数学奥林匹克（IMO）。他于 2008 获得 APCCAS 优秀学生论文奖证书。自 2024 年起，他担任 IEEE《Solid-State Circuits Letters》的副编辑。

TALK

CNN Accelerator Featuring a Memory Stationary Dataflow

The rapid growth of deep-neural-network (DNN) models has created an increasing gap between computation capability and memory efficiency in AI hardware. As memory movement now dominates both energy consumption and silicon area in modern accelerators, improving on-chip memory utilization has become essential for sustaining performance scaling. Residual-network architectures, such as ResNet, further intensify memory demands due to their large feature-buffering requirements, making memory-centric optimization a key design challenge.

In this talk, I will introduce a memory-utilization-aware CNN accelerator that addresses these challenges through a novel memory stationary (MS) dataflow. The MS dataflow unifies input and output feature processing within a single cyclic memory block, boosting memory utilization and reducing feature-memory access. To overcome buffering overhead in residual paths, we propose layer-wise clipped-asymmetric residual distillation (LCARD) quantization and memory-stationary gating (MSG), achieving higher OCMU and throughput gains over fixed-bit-width designs.

INVITED TALK 邀请报告

杨旭

中国科学院半导体研究所

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #18.2 / 08:55-09:20

杨旭，女，研究员，2020 年于中国科学院半导体研究所获得博士学位，同年入职中国科学院半导体研究所，2022 年入选北京市科学技术协会青年人才托举工程，主要研究方向包括仿生脉冲视觉芯片、脉冲型图像传感器、类脑脉冲神经网络算法和处理器，发表论文 20 余篇，申请国家发明专利 20 项。

TALK

A 10 000-Inference/s Bio-Inspired Spiking Vision Chip Based on an End-to-End SNN Embedding Image Signal Enhancement

Edge machine vision requires a vision chip to perform imaging and visual recognition with high speed, high accuracy, and compact size. Current vision chips adopt a two-stage workflow, which uses computer vision processing and a deep neural network to perform signal enhancement and recognition, respectively. However, the two stages involve different operations and are separately optimized, which causes degraded recognition accuracy, low inference rate, and huge hardware overhead. To address it, we propose a vision chip that integrates a single-photon avalanche diode image sensor and a reconfigurable spiking neural network (SNN) processor. Inspired by the human visual system that employs a full SNN for signal enhancement and recognition, the vision chip acquires spike-based images and performs an end-to-end SNN embedding image signal enhancement (ISE) for object recognition. The ISE and recognition are trained jointly in a unified deep learning framework to increase recognition accuracy and inference speed. The vision chip only integrates an SNN processor to perform ISE and recognition by being reconfigured into the low precision multiply-accumulation (MAC) mode or accumulation (ACC) mode, respectively, thereby avoiding a dedicated image signal processor. Based on a 55-nm CMOS technology, the fabricated vision chip integrates 128×128 pixels and can implement 4096 ACC/MAC components. The chip was measured to exhibit: 1) a 99.2% accuracy with 10 000 inferences/s at 10 lx and 95.3% at 1.43 mlx on the MNIST dataset and 2) a 94.32% accuracy with color mosaic images on the ETH-80 dataset.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #18.3 / 09:20-09:45

姚鹏

清华大学

姚鹏，清华大学集成电路学院副研究员，国家优青，爱思唯尔高被引学者。多年来一直从事基于忆阻器的新型存算一体智能硬件系统工作，研制国际首款多阵列存算一体系统，国际首颗忆阻器存算一体学习芯片。发表学术论文 80 余篇，授权国内外发明专利 10 余项，以第一/通讯作者发表在 Nature、Science 等顶级期刊，在 ISSCC、VLSI、IEDM 等半导体领域顶级会议报道，引用 8000 余次。主持国家“智能电网”2030 重大科技专项课题、自然基金委等多项国家项目，获得 2020 世界人工智能大会 SAIL 奖，2022 电子学会自然科学奖一等奖，2020、2023、2024 年度中国半导体十大研究进展，2025 教育部自然科学奖一等奖等。

TALK

HYDAR: A 390K QPS, 1574K QPS/W Hybrid Analog/Digital Compute-in-RRAM Accelerator for Efficient Recommendation System

We present the first 28nm hybrid compute-in-RRAM (CiR) accelerator for recommendation system (RecSys) based on the HYDAR framework: (1) DL ADCs enable early termination of non-topK calculations. (2) PPSP dataflow boosts throughput for irregular workloads. (3) A coarse-to-fine architecture preserves system recall accuracy. The 36M-RRAM CiR chip achieves 390K QPS with a SOTA 1574K QPS/W. The chips scale out to a 576M system for practical RecSys task, improving by 66x in QPS and 181x in QPS/W.

INVITED TALK 邀请报告

封晓宇

清华大学

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #18.4 / 09:45-10:10

封晓宇，现任清华大学助理研究员，于 2018 年和 2024 年分别于清华大学获取学士和博士学位，并获得清华大学 2024 年优秀博士论文。长期从事智能感知算法及硬件、低功耗电路与系统芯片等相关领域的研究工作，在 AI 模型优化算法、面向三维感知应用的高能效 AI 加速芯片等方面有丰富的成果积累。近年来在 JSSC，TNNLS，TCAD，TCAS 等期刊及 ISSCC，CICC，AAAI，ASP-DAC，A-SSCC，ISCAS 等国际会议发表论文 20 余篇，其中面向 3DGS 的加速芯片工作入选 ISSCC2025 亮点论文。

TALK

A 1286fps 0.39mJ/Frame Modeling/Rendering Unified 3D GS Processor with Locality-Optimized Computation and Reconfigurable Architecture

A modeling/rendering unified 3D GS processor is proposed with: 1) A locality-aware dynamic fine-grained rendering engine for reduced redundant computation. 2) A Locality-optimized unified rendering workflow to reduce EMA. 3) A unified reconfigurable architecture for neural modeling and gaussian rendering with minimal area overhead. It achieves 3.4× higher rendering throughput and 74.1% lower energy per frame than SOTA 3D GS accelerators, and orders-of-magnitude reduction in modeling latency.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #19.1 / 08:30-08:55

曹鹏

南京大学

曹鹏，博士，现为南京大学集成电路学院助理教授、特聘研究员。他于 2016 年获电子科技大学学士学位，2021 年获复旦大学博士学位，随后在复旦大学从事博士后研究。其主要研究方向为电源管理芯片与电机驱动芯片设计。

TALK

A Three-Mode Single-Inductor Four-Quadrant Converter Achieving 94.6% Peak Efficiency with Seamless Zero-Crossing

This paper presents a three-mode single-inductor four-quadrant converter with 94.6% peak efficiency for electrochromic smart windows. It supports a 5 to 12V input, a −5 to +5V output and a −3 to 3A load current, achieving full four-quadrant operation by employing buck/boost, inverting buck/boost and auxiliary transition modes. This integrated converter enables seamless zero-crossing and mode switching with a single inductor, thus resulting in a compact, low-cost, and low-complexity system.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #19.2 / 08:55-09:20

刘寻

香港中文大学（深圳）

刘寻，博士，现任香港中文大学（深圳）副研究员，博士生导师，校长青年学者，国家级青年人才。分别于 2011 年和 2017 年在浙江大学和香港科技大学获得本科和博士学位。在集成电路设计领域期刊和会议上共发表学术论文 38 篇，包括集成电路设计领域最高级别期刊 IEEE JSSC 论文 7 篇和被誉为“芯片奥林匹克”IEEE ISSCC 论文 5 篇。担任集成电路设计领域顶级会议 IEEE ISSCC 和 IEEE VLSI 的技术委员会成员；担任 TCAS II 副主编。2020 年，获美国高通公司专利奖；2017 年，于 ASP-DAC 获颁 University LSI Design Contest Special Feature Award（唯二篇）。

TALK

120V/230V Non-Isolated AC-DC Converter with High Power Density for IoT Devices

This report presents two non-isolated AC-DC converters for Internet of Things (IoT) applications. A 1.05-W universal input capacitive AC–DC Converter with idle power reduction will be presented first. This converter improves output power by increasing the AC–DC output voltage and stepping it down with an SC converter. Three operating modes are proposed to regulate the AC–DC output voltage and reduce its ripple. Thus, a smaller capacitor can be used to improve the power density of this system. Two capacitors in series with two LDMOS transistors are added to an AC-DC rectifier to increase loop impedance and reduce idle power, generating zero waves. The proposed power converter achieves 1.05-W output power, 577-mW/cm3 power density, and ~50% idle power reduction. Next, an offline power converter based on a full-duty-cycle input series dual-branch (ISDB) topology will be presented. The proposed ISDB converter elevates the overall output power of the AC–DC converter to 2.15-W and improves the power density to 1088-mW/cm^3.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #19.3 / 09:20-09:45

郭建平

中山大学

郭建平，博士，中山大学电子与信息工程学院（微电子学院）教授、IEEE 固态电路学会广州分会主席、ISSCC TPC Member，曾任 ICTA 电源管理 sub-committee TPC Chair。主要研究方向为电源管理及激光雷达芯片设计。在 IC 设计方向发表学术论文 100 余篇，含多篇 JSSC/ISSCC 论文。发表的 LDO 频率补偿技术广泛应用于国内头部芯片公司产品中，发表的全集成 FVF-LDO 论文单篇被引超过 400 次（谷歌学术），为近十年来被引最高的 LDO 论文之一。授权中国发明专利 40 余项，其中 20 余项已成功实施转让，电源管理芯片和激光雷达芯片实现了产业化应用。

TALK

Piezoelectric Energy Harvesting: From MPP to MPPT

A fully digital MPPT is proposed for bias-flip piezoelectric energy harvesting. Once the MPP is identified, its parameters are stored and locked. Even if the vibration amplitude/frequency changes or disappears entirely, it directly operates at the pre-recorded MPP, no need for repeated tracking and ensuring continuous maximum power output. By reusing the ZCD signal, no dedicated sampling operation is required for MPPT. The measured quiescent current of the MPPT circuit is 17 nA, and the peak MPPT efficiency is 99.8%.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #19.4 / 09:45-10:10

崔楷

清华大学

崔楷，分别于 2017 年和 2020 年在西北工业大学软件与微电子学院获得学士和硕士学位，并于 2024 年在西北工业大学计算机学院获得博士学位。现任清华大学电子工程系助理研究员，主要研究方向为无线能量传输与生物医学集成电路设计。

TALK

A Multi-Coil Scalable Energy-Shared Wireless Power Receiver Network for Distributed Time-Division-Multiplexing Somatosensory Cortex Stimulation

This work presents a system-level scalable wireless power receiver (RX) network for miniaturized distributed somatosensory cortex stimulation. By interconnecting the power outputs of all RX cells in the network, the stimulator in each cell can access the total received power of the whole network, with a time-division-multiplexing stimulation manner. Thus, each cell owns a multiple-input single-output wireless power RX network without additional RX coils, with improved efficiency and robustness.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #20.1 / 10:30-10:55

殷韵

复旦大学

殷韵，教授，博士生导师，主要从事收发机芯片设计、先进工艺高性能数字化射频电路设计和混合工艺射频芯粒异质集成等研究。获国家优青、上海市启明星项目等支持。近年来在包括 ISSCC、JSSC 等集成电路顶级会议期刊上发表学术论文 60 余篇。担任 ISSCC、ASSCC 国际会议 TPC 及期刊 TCAS-II 客座编辑。

TALK

Wideband Digital RF Transmitter Design

To fully benefit from advanced CMOS technologies, it is desirable to completely digitize the transmitter, which yields reduced die area, highly-efficient operation and direct interface to digital baseband. Driven by the increasing data rate demand with high-order modulation schemes, it poses great challenges on transmitter linearity and power efficiency to support wideband baseband signals. This talk will discuss on our recent works of wideband digital RF transmitter design.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #20.2 / 10:55-11:20

罗讯

深圳大学

罗讯，深圳大学特聘教授，国家级领军人才；IEEE 杰出青年工程师奖获得者；爱思唯尔-斯坦福大学全球前2%顶尖科学家（终身/年度），长期从事数字射频集成电路及其微系统集成相关研究。相关成果发表 ISSCC、JSSC 30 余篇，TMTT、IMS 近 60 篇。兼任/曾任 IEEE MWCL 责任主编，IWS 技术委员会主席，IMS 技术委员会分委会主席，ISSCC、CICC、RFIC 技术委员会委员等。

TALK

Digital-RF Transmitter for mm-Wave Application

Digital-RF transmitter with merits of integrated multi-function, high power efficiency, and compact circuit size is highly attractive for mordern wireless. This talk will focus on the proof-of-concept, design procedure of the digital-RF transmitter for mm-wave application.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #20.3 / 11:20-11:45

杨秉正

深圳大学

杨秉正，深圳大学电子与信息工程学院“百人计划“副教授，射频异质异构集成全国重点实验室成员。主要研究方向为射频、微波、毫米波、太赫兹功率放大器、发射机等集成电路设计。荣获 2021-2022 IEEE SSC-Society Predoctoral Achievement Award、2021 IEEE MTT-Society Graduate Fellowship Award 等奖项。

TALK

A 0.6-to-0.9GHz, 28.06dBm Pout, 43.73% SE, 6-Phase Switched-Capacitor Power Amplifier Using In-Cell Digital Waveform Synthesis for the 2nd-, 3rd-, and 4th-Harmonic Suppression

This work presents a 6-phase 0.6-to-0.9GHz switched-capacitor power amplifier with a peak output power of 28.06dBm and a peak system efficiency of 43.73%, using digital waveform synthesis for harmonic suppression. A reused differential-switch topology is utilized to generate multi-level stepped waveform with intrinsically canceled 2nd, 3rd, and 4th harmonics. Such an SCPA achieves 38.7/52.8/39.5dBc suppression level of the 2nd/3rd/4th harmonics at 850MHz and supports 40MHz 64-QAM and 20MHz 256-QAM signals.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #20.4 / 11:45-12:10

周杰

深圳大学

周杰，深圳大学射频异质异构集成全国重点实验室/电子信息工程学院助理教授。2016 年、2021 年先后在电子科技大学取得微电子专业学士学位、微电子学与固体电子学博士学位。2022 年至 2023 年，在澳门大学从事博士后研究工作。2025 年曾任电子科技大学讲师。主要研究方向为可重构无源器件、收发机与相控阵系统。

TALK

A 4.5-to-7.2GHz Beyond Rail-to-Rail Output SCPA with 27.9dBm Pout and 46.2% DE at 5.1GHz Using Periodic Voltage-Pacing Network

This work presents a switched-capacitor power amplifier (SCPA) using periodic voltagepacing network, capable of generating output voltage beyond conventional rail-to-rail limit, which enhances both the output power (Pout) and efficiency. Fabricated in a 40nm CMOS process, it shows a competitive 27.92dBm peak Pout and 46.2% peak drain efficiency covering a wide 1dB bandwidth from 4.5 to 7.2GHz. Furthermore, it supports 200MHz 64QAM and 80MHz 256QAM, confirming its suitability for 5G/6G and WiFi systems.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #21.1 / 10:30-10:55

林龙扬

南方科技大学

林龙扬，博士，2018 年获得新加坡国立大学博士学位，2021 年加入南方科技大学深港微电子学院任助理教授、副研究员、博士生导师；研究领域包括低功耗集成电路、存内计算、超低温集成电路、集成电路硬件安全等；曾获 2025 年 A-SSCC 最佳演示奖、2024 年 A-SSCC 最佳设计奖、2022 年 ISSCC 杰出远东论文奖、2022 年及 2020 年 ISSCC 最佳演示奖等奖项；担任 IEEE Trans. on VLSI Systems 的副编辑、IEEE ICTA 会议数字电路与存储分委会主席。

TALK

Collapsing the Vision Stack: Ultra-Efficient Analog Intelligence for Edge AI

This work presents a fully analog intelligent vision SoC that eliminates both sensor-processor and inter-layer A/D conversions for end-to-end vision. A continuous analog datapath from sensing to multi-layer inference is enabled by a PWM imager, an RRAM-based CIM, and a linearity-recovery analog memory. Fabricated in 55nm CMOS, the chip achieves 11pJ/(pixel·frame) sensing efficiency, 8,791 TOPS/W MAC efficiency, and 346 TOPS/W system-level efficiency across diverse vision tasks.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #21.2 / 10:55-11:20

李嘉敏

南方科技大学

李嘉敏，南方科技大学深港微电子学院副教授，博士生导师。主要从事集成电路设计领域研究，聚焦生物医疗芯片技术，研究方向包括体域无线供能与通信芯片、生物信号传感芯片、生物信号 AI 处理芯片、生物医疗集成系统设计。曾获国际固态电路会议（ISSCC）最佳演示奖、亚洲固态电路会议（ASSCC）SDC 最佳设计奖及杰出设计奖、IEEE 固态电路协会（SSCS）博士成就奖等奖项。担任 ISSCC SRP 委员会委员、ASSCC 技术委员会委员、ISEDA 技术委员会委员、ICTA 技术委员会委员等。

TALK

A Patient-Independent Prototype-Based Spatio-Temporal CNN Processor with Forward-Inference-Based Adaptation for Robust and Low-Latency Seizure Detection

This work presents a patient-independent, prototype-based spatio-temporal CNN processor for seizure detection, achieving high accuracy without patient-specific data, at the lowest energy (16.4 nJ/class) and latency (<120 ms). An optional forward-inference-based zero-shot adaptation improves robustness to variability and low-quality inputs. The 40-nm IC achieves 94.3%/94.9% sensitivity/specificity without patient data, improving to 95.4%/97.9% with adaptation, at 4.4× lower energy and 3× lower latency.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #21.3 / 11:20-11:45

朱建峰

清华大学

朱建峰，清华大学集成电路学院助理研究员，博士师从魏少军教授，主要研究方向包括可重构计算芯片、近存计算芯片和编译器优化技术等。入选国家级青年人才计划，主持国自然青年基金等多个项目，作为核心骨干参与多项国自然重大研究计划、专项项目、面上项目，获得省部级一等奖等多个奖励。

TALK

A 28-nm 239-bp/μJ Agile Pangenome Analysis Accelerator for Multi-Scheme Read Mapping

Recent advancements in deoxyribonucleic acid (DNA) sequencing have brought about a significant paradigm shift in genome analysis, moving from linear approaches to pangenome graphs. Pangenome analysis demands powerful computation capabilities to handle graph data structures, which are irregular and complex, as well as the flexibility to adapt to various algorithms and data types. This article presents the first silicon accelerator for pangenome read mapping. The 5.9-mm 2 822 -mW application-specific integrated circuit (ASIC) accelerator includes a dedicated graph mapping engine (GME) that leverages domain-specific characteristics to parallelize computations. It achieves a throughput of 151.8 Mbp/s and an energy efficiency of 239 bp/ μ J in pangenome read mapping. Moreover, its dynamic reconfigurability and pipeline bubble hiding technique allow it to efficiently adapt to multiple mapping schemes with improved hardware utilization. It is backward compatible with conventional short-read mapping and offers up to 2.24× area efficiency and 3.65× energy efficiency compared to state-of-the-art short-read mapping silicon accelerators while maintaining an accuracy comparable with standard software packages.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #21.4 / 11:45-12:10

刘嘉豪

电子科技大学

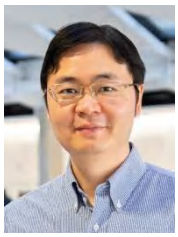
刘嘉豪，电子科技大学特聘副研究员，来自信息与通信工程学院物联网智能芯片与系统团队，团队负责人周军教授。主要研究方向为超低功耗机器学习/深度学习处理器设计，以第一作者/共同一作在 Nature Communications、ISSCC、JSSC、CICC、DAC、TbioCAS 等期刊/会议发表多篇论文，担任 TbioCAS、TVLSI、ISCAS 等期刊/会议审稿人。

TALK

A High-Accuracy and Ultra-Energy-Efficient Cardiac Arrhythmia Classification Processor for Wearable Intelligent ECG Monitoring

Wearable intelligent ECG sensors with integrated cardiac arrhythmia classification processors have been used to detect and classify arrhythmia, alerting users to potential cardiac diseases. While state-of-the-art arrhythmia classification processors employ neural networks (NN), the high computational complexity of NNs results in significant energy consumption, limiting the model size and classification performance of NNs. Additionally, inter-patient variation in ECG can lead to accuracy degradation when applying a trained NN to patients whose ECG features differ from those in the training dataset. In this work, we propose an ultra-energy-efficient cardiac arrhythmia classification processor incorporating three key technologies: 1) heartbeat difference-based classification to improve accuracy under inter-patient variation and reduce energy consumption; 2) event-driven NN computation with shared feature extraction to reduce energy consumption; and 3) an adaptive NN wake-up technique to reduce energy consumption while maintaining accuracy. The design was fabricated using 55 nm CMOS process technology and evaluated using the MIT-BIH arrhythmia dataset. For arrhythmia classification, it demonstrates an energy consumption of 0.09 μJ per classification with 98.7%/96.6% accuracy for intra-patient and inter-patient testing,respectively.

INVITED TALK 邀请报告



2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #22.1 / 10:30-10:55

孙楠

清华大学

孙楠，国家特聘专家，清华本科，哈佛博士，IEEE Fellow。他曾获美国德克萨斯大学奥斯丁分校终身教职，目前担任清华大学长聘教授、士模微电子公司创始人。他曾获美国自然科学基金 Career Award， IEEE 固态电路协会 New Frontier Award，北京市五四青年奖章。曾担任 IEEE 电路与系统协会和固态电路协会杰出讲师，JSSC 和 TCAS-I 编委，CICC 大会主席，以及 ISSCC 和 ASSCC 的技术委员会委员。他还担任过多家世界知名芯片设计公司的咨询顾问。他培养了 28 名博士生，其中 11 人在中美高校任教，包括 Gatech、ASU、清华、北大、成电、西电、西交等。他在芯片设计领域顶级期刊 JSSC 和会议 ISSCC 发表论文 70 余篇。

TALK

A Power-Efficient Jitter-Insensitive Wideband 1-bit CT ΔΣ ADC with Direct Charge Dump Feedback

Using a 1-bit quantizer in a wideband CT ΔΣ ADC is beneficial, but a 1-bit CT ΔΣ ADC imposes a stringent linearity requirement on OTA1, leading to high OTA1 power, and is sensitive to jitter when using a resistive/current-steering feedback. This work proposes to directly dump the feedback charge to the loop filter without the participation of OTA1, and OTA1 only processes the slow and small input signal and works for compensation, which does not require high accuracy, thus its power is significantly reduced. As the proposed feedback impulsively dumps the feedback charge, it is insensitive to jitter, alleviating the noise requirement on the clock circuit. To efficiently reduce the non-common-mode noise from the biasing current provider in an OTA, a switched capacitor supply is proposed. The prototype 1-bit, fourth order CT ΔΣ ADC with the proposed feedback and SC supply scheme is fabricated in a 28-nm CMOS process and achieves SNDRs of 76.3/73.2 dB in 25/40-MHz BW and Schreier FoM of 174.0/172.9 dB without DAC correction; furthermore, it can tolerate 2.4ps,rms jitter with only 1.2-dB SNDR degradation. The ADC core consumes 4.2mW, of which OTA1 only consumes 1.5mW. The prototype achieves one of the best power efficiencies among the 1-bit, jitter-insensitive, and DAC-correction-free state-of-the-art CT ΔΣ ADCs, validating the prominent advantage of the proposed techniques.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #22.2 / 10:55-11:20

陈铭易

上海交通大学

陈铭易，欧洲微电子研究中心(IMEC)博士后，现任上海交通大学集成电路学院（信息与电子工程学院）长聘副教授，博士生导师，IEEE 高级会员，TCAS-II 前任编委。长期从事面向未来产品的高性能模拟与混合信号集成电路设计研究，重点研究领域包括精密传感接口芯片、超高分辨率模数转换器芯片、微能量采集和电源管理芯片等，应用领域涵盖脑机接口、人形机器人、精密测量等工业、消费和医疗场景。近三年主持国家自然科学基金面上项目、十四五国家重点研发计划课题、中国电子学会专项，以及企业委托开发等项目十余项。在 IEEE JSSC、SSC-L、TIE、TPE、TIM、TBCAS、VLSI Symposium 等国际期刊和会议发表论文 50 余篇，申请发明专利 20 余项。研究成果获欧盟 “玛丽-居里”卓越奖、华人芯片设计技术研讨会(ICAC)最佳报告奖。承担研究生“双一流”优质课程《高等模拟模拟集成电路设计》获优秀结题。承担本科生《模拟集成电路设计》课程教学，获教学创新大赛二等奖、混合式教学创意设计奖。指导研究生获创“芯”大赛全国一等奖 3 项，企业杯赛一等奖 1 项，全国二等奖 5 项。指导多名研究生获国家奖学金、上海市优秀毕业生、上海交通大学优秀毕业生等奖项。在工业界一线从事芯片设计九年，研发多款用于消费电子和无线通信领域的数模混合信号量产芯片。

TALK

A 25.8% 3σ/μ-Accuracy, 0.12%/°C Temperature Drift Sigma-Delta Modulation Calibrated Pseudo-Resistor With GΩ to TΩ Tuning Range

This work presents an on-chip self-calibrated pseudo-resistor (PR) based on a sigma-delta modulation (SDM) loop. The proposed real-time calibration mechanism facilitates the implementation of an accurate low-drift ultra-high-value (UHV) PR with a wide tuning range at minimum hardware expenditure. Experimental results demonstrate that the resistance can be precisely tuned from 1.5 GΩ to 2.5 TΩ. The average temperature drift is 0.12%/◦C within the temperature range from−40 ◦C to 80 ◦C, which is comparable to the on chip high_x0002_resistance poly resistor. The relative accuracy (3σμ) is 25.8% under room temperature, representing an improvement of over one order of magnitude compared to an uncalibrated PR. To validate the proposed calibration loop, a capacitively-coupled instrumentation amplifier (CCIA) embedding the calibrated PR has been fabricated in a standard 180-nm CMOS process, occupying a core area of 0.187 mm^2. The CCIA achieves an accurately tunable high-pass corner frequency (fHP) from 0.13 to 217 Hz, a total harmonic distortion (THD) as low as 0.0093%, and a linear output swing up to 3.9 Vpp. The input-referred noise (IRN) is measured at 2.40 μVrms within a 0.5–200-Hz bandwidth. In conclusion, this work paves the way for implementing accurate tunable on-chip UHV resistors in mass production.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #22.3 / 11:20-11:45

王夏宇

西安电子科技大学

王夏宇，男，副教授，硕士生导师，2021 年获西安电子科技大学工学博士学位。长期从事光电探测模拟前端集成电路研究，包括：高精度时间数字转换器（TDC），高性能跨阻放大器（TIA）等。主持国家自然科学基金面上项目、青年项目，参与国家自然科学基金重点项目、科技创新 2030、科技部重点研发计划等重点项目。在 IEEE JSSC、IEEE CICC、IEEE TCAS I/II 等高水平会议和期刊发表论文 20 余篇，申请授权国家发明专利数十项，担任 IEEE TCAS I/ II 等国际期刊审稿人。

TALK

A Multi-Event, 7.9-ps Resolution Time Amplification-Based TDC With an Ultra-Low Static Phase Error DLL Using Interpolator Recycling Technique for dToF Applications

A multi-event time-to-digital converter (TDC) with a high conversion rate using an interpolator recycling technique is proposed in this work. The conversion dead time is greatly reduced by reusing the coarse interpolation channel (CIC) during the quantization of Start and Stop signals. A high resolution is achieved by a coarse–fine interpolation with a calibration-free high-linearity time amplifier (TA). A flash sub TDC using a novel fully symmetric quantization (FSQ) scheme is proposed to implement fine interpolation, which helps improve the linearity. An ultra-low static phase error (SPE) DLL with time amplification in the feedback loop is proposed, to improve the TDC's precision and linearity. The proposed TDC is fabricated in a 0.18-μm CMOS technology, achieving a 7.9-ps resolution over a 2033.5-ns dynamic range with a conversion rate of 80 MS/s. The worst case DNL and INL are +0.15/−0.09 LSB and +0.69/−0.43 LSB, respectively.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #22.4 / 11:45-12:10

祁亮

上海交通大学

祁亮，上海交通大学集成电路学院（信息与电子工程学院）副教授、博士生导师，从事模拟与混合信号集成电路设计与系统研究。2012 年在西安电子科技大学取得学士学位，2019 年在澳门大学取得博士学位，相关的研究成果在国际会议和期刊上发表超过 40 篇学术论文，包 ISSCC/VLSI/JSSC/TCAS-I 等。
入选国家级高层次青年人才计划、中国科协青年人才托举工程、上海市浦江人才计划等。现/曾主持国家重点研发计划“战略性科技创新合作”重点专项、国家自然科学基金面上项目、华为海思等多个企业联合研发项目。担任 IEEE TCAS-I、TCAS-II 和 ICAS 期刊编委，《微电子学》青年编委，IEEE ESSERC 等会议 TPC 成员。

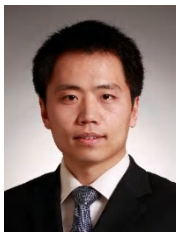
TALK

Time-Interleaved ΔΣ ADC for Broadband Wireless Applications

Time-interleaved (TI) structures have been widely used in Nyquist-rate ADC architectures such as Pipeline and SAR to enhance system sampling rates. Theoretically, this technique is also applicable to ΔΣ ADCs, effectively increasing their equivalent clock sampling rates. However, due to the recursive operational nature of ΔΣ modulators, different channels require internal interaction to achieve time interleaving, resulting in significantly higher architectural complexity compared to traditional Nyquist ADC time-interleaving schemes.

This talk presents a low-complexity solution based on extrapolation prediction: leveraging the recursive characteristics of ΔΣ modulators, the output of other channels is predicted using complete information from a single channel, thereby avoiding complex multi-channel collaborative design. Building on this approach and incorporating key circuit techniques such as hybrid-inputs adders and DAC linearity enhancement, a dual-channel TI ΔΣ ADC prototype was implemented using a 28nm CMOS process. Measurement results show that the ADC achieves 71.5 dB SNDR, 77.3dB DR, -160.3 dBFS/Hz NSD over a 200 MHz signal bandwidth, with a power consumption of 106 mW, delivering a state-of-the-art FoMS|SNDR of 164.3 dB.

INVITED TALK 邀请报告



2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #23.1 / 13:30-13:55

祁楠

中国科学院半导体研究所

祁楠，中国科学院半导体所研究员，中国科学院大学岗位教授，博士生导师。2013 年于清华大学获得博士学位，随后在美国俄勒冈州立大学、惠普公司从事研发工作，2017 年加入中国科学院半导体所工作至今。他持续针对高速通信集成电路、光电融合互连芯片研究，主持包括国家自然科学基金（面上、重点、重大研发计划）、国家重点研发计划等项目 10 余项，发表高水平论文 90 余篇，获亚洲固态电路会议“学生杰出设计奖”，成果两次入选“中国半导体十大研究进展”；学术兼职《半导体学报》编委、JSSC Guest Editor，IEEE ASSCC、ICTA、ICCS 等会议 TPC 成员，并担任 2025 年 ASSCC TPC 副主席。

TALK

Monolithically Integrated DWDM Si-Photonic Transceiver for Chiplet Optical I/O

With the explosive development of AI and ML, the ever-growing data movement is asking for high density interconnects with higher bandwidth, lower power and lower latency. However, the millimeter-sized MZM can hardly fit into xPU packages. Dense wavelength division multiplexing (DWDM) is also needed to shrink the fiber counts for higher shoreline density. The transistor-size Micro-Ring Resonator (MRR) enables high-density and high-efficiency integration with CMOS circuits. Its intrinsic resonance is employed for dense-WDM in the optical link. In this talk, a monolithically integrated DWDM Si-photonic transceiver is presented. All necessary electronic and photonic circuits are fully integrated on a single CMOS chip, including 4 channel drivers, transimpedance amplifiers (TIA), micro-ring modulators (MRM), micro-ring filters (MRF) and photodetectors (PD). Based on the high-Q micro-ring resonation, four 200-GHz spaced wavelengths transmitting and receiving at 50 Gb/s/λ each is demonstrated. Implemented in 45-nm SOI CMOS, experimental results show clear eyes at 4λ × 50 Gb/s with <10-12 Bit Error Rate (BER), achieving 176-Gb/s/mm2 BW-density and 3.5-pJ/bit power efficiency, which is boosted to 224-Gb/s/mm2 and 2.85-pJ/bit at 64-Gb/s/lane. Full link transceiver and multi-λ crosstalk experiments are demonstrated. At last, the recent advances in our group on the integrated optical I/O will be briefed.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #23.2 / 13:55-14:20

贾海昆

清华大学

贾海昆，博士，清华大学集成电路学院副教授、特别研究员和博士生导师。主要研究方向为硅基毫米波/太赫兹集成电路设计以及高速串行接口技术，包括：高性能硅基太赫兹信号源、毫米波高速无线通信收发机阵列、低功耗混合信号基带解调技术、毫米波 FMCW 雷达、大规模毫米波相控阵等等。作为负责人承担科技部重点研发计划、国家自然科学基金、北京市新一代信息技术等国家级和省部级科研项目。担任了亚洲固态电路会议（A-SSCC）、国际集成电路技术和应用学会（ICTA）的技术委员会成员。发表学术期刊和国际学术会议论文 100 多篇，包括集成电路设计领域顶级期刊 JSSC、IEEE Trans. MTT、IEEE TCAS-I、国际固态电路会议 ISSCC、欧洲固态电路会议 ESSCIRC 和亚洲固态电路会议 A-SSCC 等。

TALK

Exploring the Speed Limit of Planar CMOS Processes: A 240Gbps 0.7pJ/bit Analog Efficiency PAM4 Transmitter in 65n CMOS Process

Driven by artificial intelligence (AI), the data rate of high-speed SerDes is evolving rapidly from 200 Gbps per single channel to 400 Gbps. The performance of high-speed SerDes is strongly correlated with processes. Advanced FinFET processes boast advantages such as high transistor cut-off frequency (fT), fast switching speed, short interconnection routing length, and robust digital processing capability. FinFET processes from 14nm to 3nm are widely adopted by the industry at the 100G/200G generations. How to achieve a data rate comparable to that of advanced processes based on mature planar CMOS processes has become a valuable research topic. This report presents our exploration into the speed limit of planar CMOS processes and discusses the design techniques of a 240 Gbps PAM4 high-speed SerDes and a 256Gbps 5.4Vppd optical linear driver based on the 65 nm CMOS process. The relevant technologies can also be applied to advanced process nodes, which accelerates the evolution toward 400 Gbps per channel.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #23.3 / 14:20-14:45

郑旭强

中国科学院微电子研究所

郑旭强，中科院微电子研究所研究员，长期从事高速串行接口 SerDes 的研究，当前核心工作集中在：（1）10~32 Gb/s 传统 NRZ 调制高速串行接口与 DIE2DIE 单端高速并行接口的应用研究；（2）56~112 Gb/s PAM4 调制高速串行接口的样品研制；（3）200+Gbps 幅度/相干调制高速 DSP 关键技术研究。主持科技部重点研发计划、自然科学基金、中科院重点部署及横向研发等项目。近年来在 JSSC、TCAS-I、TCAS-II、CICC、ESSCIR 等国际知名期刊和会议发表论文 50 余篇，授权专利 11 项。担任 JSSC、TCAS-I、TVLSI 等期刊的评审工作。

TALK

A 112-Gb/s PAM-4 Retimer Transceiver

This report presents an ADC-DSP-based 112-Gb/s PAM-4 transceiver for long-reach retimer applications. It incorporates a compact low-jitter clocking scheme, an output-jitter-optimized TX, and a compensation-enhanced RX to lower the clock jitter and link BER while maintaining a high-energy efficiency. The clocking scheme utilizes a single jitter-filtering PI followed by an ILO to obtain synchronous low-jitter clocks with relaxed bandwidth and low-power consumption. The TX features an internal FFE cascaded with a forward-coupling pad driver to improve the output ISI jitter, and a timing-optimized 4:1 MUX to reduce the serialization jitter. The RX contains a flexible CTLE, an SNR-optimized ADC, and a high-resolution digital FFE/DFE to improve the compensation accuracy and further minimize the BER. These techniques are demonstrated by a prototype fabricated in a 28 nm CMOS process, achieving a raw BER of 1E-12 at 112 Gb/s over a 31.2-dB loss channel. The clock network delivers a rms recovered clock jitter of 252 fs and a power efficiency of 0.56 pJ/bit, which outperforms other state-of-the-art works. This work also verified the viability of forward-error correction-free PAM-4 transceivers beyond 100 Gb/s/lane for the high-speed retimer applications in the data center.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #23.4 / 14:45-15:10

江文宁

复旦大学

江文宁，博士。复旦大学集成电路与微纳电子创新学院青年副研究员。2020 年博士毕业于澳门大学，2020 年至 2021 年于澳门大学从事博士后研究工作，2022 年加入复旦大学。主要研究方向包括高性能数据转换器、高速接口、脑机接口等方向。

TALK

A 16Gb/s/pin 0.51pJ/bit Single-Ended NRZ Transceiver with Distributed Dual-Loop VDDQ Ripple Compensation and Dynamic Clock Duty-Cycle Calibration for Memory Interfaces

This work presents a 16 Gb/s/pin 0.51 pJ/bit single-ended NRZ transceiver with distributed dual-loop compensation (DDLC) for VDDQ ripple suppression and dynamic duty-cycle calibration (DDCC) for robust clocking. The DDLC locally regulates VDDQ ripple with a shared low-power LDO, reducing decoupling capacitor by 91.4% while improving horizontal/vertical eye margins by 1.61×/1.36×. Demonstrated on five channels, it scales naturally to larger DQ counts for high-density memory.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #23.5 / 15:10-15:35

赵潇腾

西安电子科技大学

赵潇腾，西安电子科技大学教授/博士生导师，国家级青年人才，专注于高速数据接口与芯粒互连集成电路设计。主持国家自然科学基金重大研究计划重点项目 1 项、面上项目 1 项，陕西省重点研发计划项目 1 项。在 IEEE ISSCC/JSSC/CICC/TMTT/TCAS-I 等旗舰会议及期刊上发表论文四十余篇，拥有 25 项专利。相关工作入选 2022 年“中国半导体十大研究进展候选”。以第一完成人获得科技研发与最佳论文奖 3 项。担任 IEEE ICTA TPC 并入选《微电子学》首届青年编委。参与 IEEE 标准制订 2 项。

TALK

Compatibility and Testability Techniques for High-Speed and High-Density Interfaces

With the development of wireline communication and the Chiplet ecosystem, numerous standards and protocols have emerged for high-speed, high-density interfaces. Concurrently, the testing challenges associated with these interfaces have become increasingly prominent. This report aims to explore compatibility technologies across multiple standard protocols, primarily focusing on clock and data synchronization techniques, transmitter linearization techniques, wideband clock generation and distribution circuits, as well as on-chip built-in-self-testing (BIST) technologies in both the time and frequency domains.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #24.1 / 13:30-13:55

唐中

西安电子科技大学

唐中，本科和博士毕业于浙江大学，曾任荷兰代尔夫特理工大学博士后研究员，多年集成电路产业界工作经历，现为西安电子科技大学教授，研究方向高性能传感器接口集成电路设计。研究成果发表于 IEEE JSSC、IEEE ISSCC、IEEE TCAS-I 等国际知名学术期刊和会议论文 50 余篇，包含第一/通讯作者的 IEEE ISSCC、IEEE JSSC 10 余篇，部分成果获得浙江省科技进步二等奖。

TALK

Capacitively-Biased Diode Technique and Its Applications

BJTs/Diodes biased with static current sources can generate PTAT and CTAT signals, which are widely used to build bandgap references, temperature sensors, and other analog circuits in CMOS processes. Despite their high accuracy and reliability, they typically require an over-1V supply voltage, which may limit their applications in advanced CMOS processes, where a sub-1V supply is preferred. Furthermore, their over-1V supply and static power also limit the energy efficiency in IoT applications. To further reduce the supply while keeping high accuracy, the capacitively-biased diode (CBD) technique was proposed recently. Instead of using static current sources, BJTs/diodes can also be biased by pre-charged capacitors, which require a lower voltage headroom and consume only dynamic power. In this talk, the speaker will introduce the recent research on the CBD technique and explore its applications in various analog designs, such as temperature sensors, bandgap references, and current sources.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #24.2 / 13:55-14:20

吕良剑

华东师范大学

吕良剑，博士，现任华东师范大学副教授、博士生导师。主要研究方向聚焦高通量无线脑机接口、智能感知等应用场景中的高可靠模拟、混合信号集成电路设计。近 5 年主持国自然基金青年项目、国家重点研发计划课题、上海市市级重大专项课题、上海市基础研究计划项目等 7 项。以一作、通信在 JSSC、TCAS-I/II、TBioCAS、ISSCC、CICC、ESSERC、A-SSCC 等 IEEE 期刊及国际会议发表文章 30 余篇。科研成果多次获得国际学术奖项，包括：以第一作者获得了 2019 年 ISCAS 生物医疗方向最佳论文奖和 2020 年 ISCAS 学生最佳论文奖；以通讯作者入选 2024 年 CICC 学生最佳论文候选与 2025 年 TCAS-I 月度亮点论文。2020 年入选上海脑科学与类脑研究中心首批“求索杰出青年”——“求索”青年研究员。

TALK

A 1ppm/°C and ±0.066% 3σ Accuracy Bandgap Reference with Temperature-Adaptive PTAT Scaling

This paper presents a process-independent, curvature-compensated bandgap reference. By introducing a temperature-adaptive duty-cycled resistor to scale the PTAT voltage, the design effectively compensates for CTAT nonlinearity without introducing offset errors. Fabricated in 0.18μm CMOS, the prototype chip occupies 0.068mm2 and consumes 15μA. After two-point trimming, it achieves an average temperature coefficient of 1 ppm/°C and a 3σ output accuracy within ±0.066%.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #24.3 / 14:20-14:45

刘彦

上海交通大学

刘彦，博士，上海交通大学集成电路学院副教授。研究方向为模拟集成电路设计技术、植入式脑机接口和片上实验室系统，致力于利用混合信号集成芯片实现高通量的生物传感。主持或参与多项脑机接口、信号传感国家纵向和企业横向课题，在集成电路设计、脑机接口等方向发表行业权威期刊/会议论文 40 余篇，申请国内外专利发明专利 10 余项，已授权 4 项。

TALK

PWM-Based Impedance Boosting Technique With Autonomous Background Calibration for VCO-Based Neural Front Ends

Adaptive impedance boosting for bio-signal acquisition front-ends is crucial for wearable and implantable devices where sensors exhibit high and widely varying source impedance. This talk presents a pulse-width modulation (PWM)-based, capacitively coupled chopped voltage-controlled oscillator (VCO) continuous-time delta-sigma modulator (CTDSM) for bio-potential monitoring. A PWM-based positive feedback loop is introduced to cancel on-chip coupling and decoupling effects, thereby boosting input impedance with a simplified calibration digital-to-analog converter (DAC). A frequency-domain loop stability detection scheme continuously monitors VCO outputs through a fully digital implementation, enabling a background auto-calibration mechanism that achieves sub-second convergence time. Fabricated in a 180-nm CMOS process, the proposed VCO-based neural front-end achieves an IRN of 3.09 μVrms, an SNDR of 81.0 dB, and a DR of 85.7 dB, at a 10-kHz chopping frequency, it exhibits. Additionally, an input impedance of 8.73 GΩ is achieved at 2 Hz.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #24.4 / 14:45-15:10

石丹

广东工业大学

石丹，博士，广东工业大学“青年百人计划”特聘副教授。本(2016)、硕(2019)毕业于四川大学微电子系，于 2025 年在澳门大学模拟与混合信号集成电路全国重点实验室获得博士学位，研究兴趣包括应用于物联网超低压、低功耗、紧凑型智能温度传感芯片；高集成度 SoC 下高性能温度传感及补偿系统设计等。已发表高水平论文 10 余篇，包括第一作者身份发表 2*JSSC /1* ISSCC /等。在 ISSCC-2025 会议获 STGA 旅行资助奖。2019-2020 年曾就职产业界并参与公司商业芯片项目。兼任 IEEE JSSC、TCAS-I、TCAS-II、Sensors Journal 等多个期刊审稿人。

TALK

A Wire-Metal-Based Temperature Sensor With a Fractional-Discharge FLL and V2T Converter Achieving 45-fJ •K2 R-FoM in 28-nm CMOS

This report presents a compact wire-metal-based temperature sensor for thermal detection in advanced technologies. The key innovations include: 1) a fractional-discharge scheme originated by extracting the fractional pulse from the 5-phase voltage-controlled ring oscillator (VCRO) to shrink the discharge window in the front-end (FD) to 10% of a complete clock cycle, preserving the power budget while eliminating the need for bulky metal resistors; 2) a voltage-to-time (V2T) converter with chopping implemented as amplifying stage inside the frequency-locked loop (FLL), eliminating the undesired dc offset and 1/f-noise to safeguard the sensing accuracy and resolution. Prototyped in 28-nm CMOS process, this sensor occupies a footprint of 4,100 μm2 and consumes 10.5 μW under 0.8 V VDD at room temperature. It demonstrates outstanding 3σ inaccuracies of □1.5 °C/□0.2 °C after 1-/2-point trimmings across −40 to 125 °C, respectively. The resolution figure-of-merit (R-FoM) achieves 45 fJ·K2, illustrating the best-in-class performance compared to the resistor-based temperature sensors in the sub-65-nm process.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #24.5 / 15:10-15:35

李海华

澳门大学

李海华，博士，2017 年于武汉大学微电子学学士学位，2020 年于中国科学院微电子研究所取得硕士学位。2020 - 2021 年，他在慧智微电子（广州）公司出任射频电路设计工程师。2025 年，他在澳门大学获得电机及电脑工程博士学位。自 2025 年 8 月起，他在澳门大学模拟与混合信号超大规模集成电路全国重点实验室担任博士后研究员。其研究方向涵盖模拟/混合信号集成电路、低功耗低噪声时钟以及温度补偿电路系统。在博士期间，他以第一作者身份发表了多篇 ISSCC 以及 JSSC 论文。

TALK

A 0.6V 9.4µW 1,892µm2 Current-Pulse-Injection Crystal Oscillator Featuring Capacitively Biased Amplifier with 242.2dBc/Hz PN FoM @1kHz Offset

This paper reports a current-pulse injection-based Crystal Oscillator (XO). A capacitively biased amplifier, powered by the stacked capacitor power supply (SCPS), delivered a short boosted current pulse into the crystal to limit the amplifier's shoot-through current while upholding the XO's phase noise. Fabricated in 65nm CMOS, the XO core occupies 1,892µm^2. The 16MHz XO consumed 9.4µW at 0.6V VDD, associated with a phase noise of −137.9dBc/Hz @1kHz offset, corresponding to a superior FoM of 242.2dBc/Hz.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #25.1 / 13:30-13:55

程林

中国科学技术大学

程林，现任中国科学技术大学集成电路学院（微电子学院）教授。主要研究方向为功率及模拟集成电路设计，包括高压/高速直流-直流转换器、隔离电源芯片、无线充电芯片、模拟前端芯片等。在国际会议和期刊上发表论文 100 余篇，其中以第一或通讯作者发表集成 ISSCC 和 JSSC 论文 30 余篇。曾获 2026 年 IEEE SSCS New Frontier Award，2020 年 IEEE ASP-DAC 最佳设计奖、2018 年香港科学会青年科学家（提名奖）和 2015 年 IEEE 固态电路协会 Pre-Doctoral Achievement Award。现任 ISSCC 技术委员会 Power Management 分委会成员。

TALK

A 100A LLC Resonant Converter with an Embedded Primary-Current-Extracted Regulator

LLC resonant converters are widely used for 48V-to-~1V xPU power delivery due to their inherent ZVS/ZCS operation, which enables high efficiency and compact magnetics. To support hundred-ampere load currents, multiple paralleled discrete GaN/Si power devices are typically employed, whose gate drivers require a dedicated low-voltage supply (e.g., 5V). In conventional implementations, this supply is generated by a separate auxiliary buck converter or transformer winding, increasing BOM, board area, and efficiency loss.

To address these challenges, this report presents a 100A LLC resonant converter with embedded primary-current-extracted regulator. The proposed regulator supplies the gate drivers of the LLC converter, thereby eliminating the need for an external auxiliary buck converter or additional auxiliary windings. Fabricated in a 0.18μm BCD process, the proposed regulator occupies a die are of 8.3mm2. Operating at a switching frequency of 1MHz, the LLC resonant converter achieves a 60V/2V voltage conversion with a peak efficiency of 93.4%.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #25.2 / 13:55-14:20

孟淼

同济大学

孟淼，同济大学特聘研究员，博士生导师、电子科学与技术系副主任，高能效集成电路与系统实验室 PI。近年来，围绕低功耗、高能效模拟/射频集成电路设计方向，设计研发多款芯片，包括超低功耗无线通信芯片、全植入式脑机接口芯片、人体信道通信芯片、环境能量采集芯片等，研究成果以第一/通讯作者多次发表在 ISSCC/JSSC。现担任 CICC 技术委员会委员。

TALK

PVT-Robust Wide-Band Backscatter Modulator for Ultra-Low Power IoTs

Conventional backscatter modulators are limited to low-order modulation at low data rates, whereas existing high-order approaches exhibit PVT sensitivity and require frequent calibration. This talk will introduce an energy-efficient backscatter modulator supporting wide-band, high-throughput, and calibration-free operation.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #25.3 / 14:20-14:45

王远飞

澳门大学

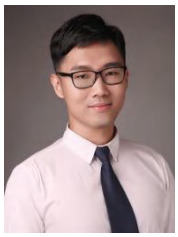
王远飞 ，澳门大学模拟与混合信号超大规模集成电路国家重点实验室博士后。本科与博士毕业于电子科技大学，博士后期间先后在中国科学技术大学与珠海澳大科技研究联合工作站、澳门大学、香港科技大学从事研究工作。个人在集成电路领域累计发表 17 篇高水平论文，包括 3 篇 IEEE ISSCC 会议论文，2 篇 IEEE JSSC 期刊论文，并荣获 2025 IEEE CICC 最佳常规论文奖。研究方向为高性能电源管理集成电路、能量采集系统等。

TALK

A Battery Charger Based On Mesh-Connection 2×CF Continuously-Scalable-Conversion-Ratio Converter Achieving 3.2W/mm3 Power Density

This work presents a compact battery charger for smartwatches based on a mesh-connected continuously scalable-conversion ratio converter (CSC) that uses only two CFs. The proposed design reduces the number of invalid phases, switch and routing resistance, achieving 89.2% efficiency at 16.8 W output power and a power density of 1.6 W/mm^2 and 3.2 W/mm^3. A shared- EA scheme ensures a smooth transition between constant-current and constant-voltage (CC-CV) modes. With a peak power PCE of 92%, this compact and efficient design is particularly well-suited for smartwatch applications.

INVITED TALK 邀请报告



2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #25.4 / 14:45-15:10

胡琛

南方科技大学

胡琛，南方科技大学电子与电气工程系研究助理教授（副研究员）。研究应用于服务器电源、高压驱动电源等领域的集成电源芯片，包括电路拓扑、控制和模拟设计自动化等，并在 ISSCC, JSSC, TPE, TCAS-I 和 TCAS-II 发表多篇论文。担任 TPE,TCAS-I 审稿人，IEEE 国际集成电路与系统会议(ISICAS2025)分会主席。共申请发明专利 13 项，其中 3 项已获得授权。

TALK

A 2.5-5V Input 100V Output 86.2% Peak Efficiency Fibonacci-Dickson Hybrid Converter for Acoustic Surface Audio Driver

This talk introduces a hybrid boost converter designed for the acoustic surface audio driver, operating within an input voltage range of 2.5–5 V and boosting it to a high voltage (HV) of 100 V. The design adopts a cascaded approach by integrating the Fibonacci and Dickson switched-capacitor (SC) topologies. This combination enables the converter to achieve a high-voltage conversion ratio (VCR). It offers the advantages of a reduced number of flying capacitors and reduced voltage stress for power switches. To improve the overall efficiency, we only use laterally diffused N-type metal-oxide-semiconductor (LDNMOS) power switches, which offer low ON-resistance, fast switching, and reduced fabrication mask requirements. In addition, a stacked active bootstrap replaces the conventional bootstrap diode with an actively controlled transistor that has lower ON-resistance, overcoming the diode forward voltage drop issue and improving efficiency. The converter delivers a maximum output power of 2 W at 100-V output voltage with a peak efficiency of 86.2% and a power density of 7.43 W/cm3.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #25.5 / 15:10-15:35

路延

清华大学

路延，清华大学长聘教授、兴华讲席教授、国家级高层次人才、国自然优青（港澳）。2013 年博士毕业于香港科技大学电子与计算机工程系。2014 至 2024 年就职于澳门大学微电子国家重点实验室；2024 年 7 月 1 日加入清华大学电子工程系。主要研究方向包括功率转换器设计、电源管理芯片设计、无线能量传输电路与系统等。发表学术论文 200 余篇，学术专著三本，其中 IC 设计领域顶尖论文 ISSCC+JSSC 共 70 余篇。曾获 IEEE 电路与系统协会 2017 杰出青年作者奖、ISSCC 2017 菅野卓雄远东最佳论文奖、IEEE 固态电路协会博士生成果奖 2013-14 届（本人）及 2024-25 届（指导学生）。曾任 JSSC、TCAS-I 和 TCAS-II 客座编辑；ISSCC 技术委员会成员、CICC 电源分会主席、IEEE SSCS 杰出讲师。现任 IEEE CASS 杰出讲师、IEEE TCAS-II 资深领域编辑、IEEE JEDS 副编辑和《半导体学报》副主编。

TALK

An Inductor-at-Middle Hybrid Buck Converter with Shared Power-Signal Path for Distributed Vertical Power Delivery

This talk presents an inductor-at-middle hybrid buck DC-DC converter for high-current density vertical power delivery, reusing the power inductors as signal feedback paths. The proposed switching bus multiplexing control reuses the power path to carry a feedback signal, mitigating the challenges in sophisticated signal and power network co-design for pin-intensive distributed applications. The prototype achieves a vertical current density of 1.65A/mm^2.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #26.1 / 15:45-16:10

许灏

复旦大学

许灏，复旦大学青年研究员，博士生导师，IEEE 高级会员，2010 年复旦大学微电子学本科学位， 2018 年加州大学洛杉矶分校（UCLA）电子与计算机工程博士学位，长期从事射频、模拟以及混合信号集成电路设计研究。2017 至 2019 年在 Broadcom 全职工作参与研发基于 DSP 的相干光通信收发芯片，2019 年至 2021 年于 Apple 全职工作参与研发高性能无线通信芯片，自 2021 年回国后于复旦大学微电子学院全职工作，发表 IEEE JSSC、IEEE ISSCC 等国际高水平期刊和会议论文 40 多篇。

TALK

Design of 25–31GHz Power Amplifier and True Power Detection in 40nm CMOS

We present a compact mixer-based true power detector integrated within a Ka-band power amplifier (PA). By performing capacitive voltage sensing and inductive current sensing at the primary coil, the compact power detector eliminates the need for additional area-consuming passive components while still allowing the power amplifier to maintain a single-ended antenna output. The control of magnetic coupling with the secondary coil is achieved by exploiting magnetic flux cancellation rather than increasing the physical distance between coils. The active mixer multiplying the voltage and current employs current bleeding technique that simultaneously suppresses the flicker noise and enhances linearity, leading to a state-of-art dynamic range. Without phase shifters or resistor termination, the overall power detector achieves intrinsic phase compensation by matching the delays between the voltage and current sensing paths. Fabricated in a 40nm CMOS process, the power detector occupies covers a detectable power range from -18dBm to +15dBm across 25-31GHz with 12.1mW power consumption.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #26.2 / 16:10-16:35

文进才

杭州电子科技大学

文进才，杭州电子科技大学电子信息学院教授，博士生导师，研究方向为射频/毫米波集成电路设计、毫米波多频段可重构电路及系统芯片设计等。

TALK

A Compact 26/38GHz-Reconfigurable Dual-Band LNA Using Transformer-Based Pole-Zero-Inversion Image-Rejection Technique Achieving >39/41dB IRR for 5G Multi-Band Applications

The fifth-generation (5G) communication technology utilizes millimeter-wave (mm-wave) spectrum to meet high-speed data transmission requirements. These 5G Frequency Range 2 (FR2) bands typically include the n257/n258/n261 and n259/n260 bands, which can be classified as a mm-wave low-frequency (LF) band (24.25 to 29.5GHz) and high-frequency (HF) band (37 to 43.5GHz). A large-scale multi-channel transceiver technology is the key to expanding mm-wave transmission distance and communication capacity. However, the number of transceiver channels is limited by the operating frequency bands and antenna size. Therefore, multi-band mm-wave circuits that can significantly reduce chip size and power consumption are both highly practical and technically challenges. In this talk, we will report a compact 26/38GHz dual-band high-IR LNA for narrow-LO dual-side mixing reception. This work simultaneously reduces the requirements for LO source bandwidth and IQ architecture reception, provideing an alternative solution for simplified and compact mm-wave multi-band transceiver circuits.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #26.3 / 16:35-17:00

顾鹏

东南大学

顾鹏，博士，2017 年获东南大学信息工程专业学士学位，2022 年获东南大学信息与通信工程专业博士学位。2022 年加入东南大学信息科学与工程学院移动通信全国重点实验室，任助理研究员。主要研究面向 B5G/6G 通信、卫星通信、雷达等系统的相控阵波束成型芯片、变频芯片及通感一体芯片等。

顾鹏博士曾入选国家“博新计划”和江苏省“卓越博士后计划”。主持了江苏省科技重大专项联合攻关项目、国家自然科学基金青年基金、江苏省自然科学青年基金、博士后科学基金面上项目等研究项目，参与了国家重点研发计划、国家自然科学基金等项目。作为核心成员参与的“CMOS 毫米波大规模集成平板相控阵技术及产业化”项目，获评 2023 年国家技术发明二等奖。研发多款全集成高性能相控阵芯片、变频芯片、雷达收发芯片，应用于卫星互联网、新一代移动通信等关键领域；在 JSSC、TMTT、TCAS-I、RFIC、A-SSCC 等权威期刊和会议发表论文 28 篇；获中国发明专利授权 3 项，实用新型专利授权 1 项。

TALK

K-/Ka-Band Down/Up Frequency Converter Chipsets for Phased Array SATCOM Ground Terminals

Large-scale integrated phased arrays are enabling the millimeter-wave (mm-Wave) satellite communications (SATCOMs). Dedicated to the SATCOM planar phased array systems, the design of the K-/Ka-band down/up frequency converter (FC) chipsets is presented. The quadrature Gilbert FCs benefit from the proposed differentiated IF and LO high-order in-phase and quadrature (IQ) balancing techniques, supporting fully on-chip high-image/sideband rejection ratio (IRR/SRR). The wideband IF signal processing chains, simultaneously enabling gain control, reconfigurable filtering, Hilbert transformation, voltage/power amplifying, as well as single-ended/differential signal conversions, are proposed for the heterodyne up and down FCs. The FC chipsets fully support the 2-D operation in the RF band of 17.7–21.2 GHz [downlink receiver (RX)]/27.5–31.0 GHz [uplink transmitter (TX)] and the wide-IF band of 0.8–4 GHz, offering the peak conversion gain of 35.7/33 dB for the RX/TX, with over 40-dBc IRR/SRR and 58-dBc calibrated LO suppression.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 1

TALK #26.4 / 17:00-17:25

唐大伟

东南大学

唐大伟，男，2025 年博士毕业于东南大学电磁场与微波技术专业，2020 年本科毕业于西南交通大学电子科学与技术专业。主要研究方向为宽带毫米波太赫兹芯片与系统，以第一作者在 ISSCC、JSSC、CICC、ASSCC 等固态电路领域会议与刊物发表 10 篇论文，合作发表 37 篇论文。曾获 SSCS Predoctoral Achievement Award、中国电子学会优博论坛十佳墙报奖、第七届/第六届 ICAC 华人芯片研讨会最佳海报奖、全国宝钢特等奖学金等荣誉。

TALK

Ultra-Broadband Self-Compensated Vector-Modulation Phase Shifter With Over 100-GHz Bandwidth

With the rapid development of communication, radar, radio astronomy and security inspection imaging, next-generation RF systems are evolving toward universal and ultra-broadband (UBB) operation. However, the lack of wideband and low-cost phase shifter (PS) has been a bottleneck in these systems, limiting the operating bandwidth, phase resolution, size, and ease of array expansion. In this work, we introduce a self-compensated vector modulation (SCVM) PS architecture with significant reduction in amplitude and phase errors, and dramatically enhanced bandwidth. It also effectively suppresses performance degradation caused by non-ideal factors such as variable gain amplifier (VGA) nonlinearity and coupler imbalance. An overcompensation technique that eliminates amplitude and phase errors is proposed, and the operating bandwidth of a silicon-based PS has been increased to more than 100 GHz for the first time. To reduce the chip area, an active-coupling technique is introduced, reducing the large chip size requirement for passive devices. The prototype PS is designed in a 130-nm SiGe BiCMOS process, achieving a state-of-the-art operation frequency range from 6 GHz to 110 GHz, with a maximum $\Delta\theta$RMS of 3°, a maximum ΔGRMS of 0.5 dB, and a phase shifting resolution of 2.5°.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #27.1 / 15:45-16:10

陈迟晓

复旦大学

陈迟晓，复旦大学集成电路与微纳电子创新学院副研究员/博导，集成芯片与系统全国重点实验室副主任/创新中心主任，国家自然科学基金委优青，上海市青年科技启明星。研究方向包括 AI 芯片架构、存算一体和三维集成，在 12nm-65nm 主流节点完成 20 余次流片。在芯片设计顶会 ISSCC/顶刊 JSSC 等上发表论文 11 篇，任 A-SSCC 技术委员会委员，ICAC 大会共主席、集成芯片与芯粒大会论坛组织主席等，获上海市技术进步一等奖、IEEE A-SSCC 杰出设计奖、复旦大学五四青年奖章等。

TALK

Scalable Compute-in/near-Memory Systems with 2.5D/3D/3.5D Integration

The rapid expansion of large AI models, such as ChatGPT, has placed significant challenges on traditional computing architectures. To overcome the memory wall memory-centric architectures such as Computing in/near Memory (CIM/PNM) have emerged, integrating computation and memory to reduce both latency and energy consumption. This talk explores the scalability of CIM/PNM systems through 2.5D/3D/3.5D heterogeneous integration enabled by advanced packaging techniques. In 2.5D integration, a layer-wise pipeline parallelism mapping is discussed, where inter-chiplet communication is minimized to improve efficiency. In 3D integration, the stacking interface promises enhanced bandwidth, reduced interconnect delays, and scalable performance for AI workloads. An active interposer-based 3D CIM system is developed to enable flexible 3D communication. The talk will also address the architectural and circuit-level challenges associated with designing active interposer-based systems. In 3.5D integration, an architecture-algorithm co-design approach is developed for decoder-only large language model (LLM) systems. The recent 3.5D PNM technology effectively addresses the extremely large memory access and tens of gigabytes of weight data required by these systems. These 2.5D/3D/3.5D approaches offer a viable path for sustaining advancements in scaling laws in the post-transistor-scaling era, with significant implications for AI infrastructure, edge computing, and high-performance systems.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #27.2 / 16:10-16:35

刘波

东南大学

刘波，东南大学集成电路学院副教授、博导，EDA 国创中心人才培训部部长。长期从事智能计算电路与芯片设计研究，主持国家自然科学基金、国家重大科技专项课题、国家重点研发计划课题等。在 ISSCC、IEDM、MICRO、DAC、TCAS-I/II、TCAD 等电路设计权威期刊和学术会议中发表论文 50 余篇。在 28nm、22nm 等工艺节点成功流片 10 余款原型芯片，部分技术已在国内行业领军企业产品中完成验证部署。

TALK

A 51.6μJ/Token Subspace-Rotation-Based Dual-Quantized Large-Language-Model Accelerator with Fused Scale-Activation INT Datapath and Rearranged Bit-Slice LUT Computation

A 51.6μJ/token accelerator for rotation-based dual-quantized LLMs is presented. A subspace-rotation method with parallel Hadamard transposer reduces on-chip rotation power by 62.3% and area by 59.7%. A fused scale-activation unit lowers energy by 61.5% vs. the naive FP design. Rearranged bit-slice LUT computation achieves 2.28 × better energy efficiency compared to a direct bit-parallel MAC implementation, while supporting flexible bit-width. The chip reduces per-token energy by 32.6% over SOTA under an equal accuracy constraint.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #27.3 / 16:35-17:00

李潇然

北京理工大学

李潇然，北京理工大学集成电路与电子学院预聘助理教授/特别副研究员，长期从事集成电路设计与存算一体技术相关研究。在 Nature Electronics、IEEE Journal of Solid-State Circuit、IEEE International Solid-State Circuits Conferences、IEEE Transactions on Electron device 等国际国内权威期刊和会议发表论文 60 余篇，其中以第一作者或通讯作者发表 SCI 检索论文 20 篇；授权国家发明专利 13 项；以第一作者出版“十四五”国家重点出版物一部。作为项目负责人主持国家自然科学基金、北京市自然科学基金、国家重点研发计划子课题、中国博士后科学基金以及多项横向课题，设计完成多款具有自主知识产权的芯片并通过实际测试验证，相关研究成果积极推动我国芯片的研发和产业化，指导学生获得挑战杯、全国大学生集成电路创新创业大赛等国家级和省部级奖项 20 项。

TALK

A Multicore Programmable Variable-Precision Near-Memory Accelerator for CNN and Transformer Models

Convolutional neural network (CNN) and Transformer are the most popular neural network models in computer vision (CV) and natural language processing (NLP). It is quite common to use both these two models in multimodal scenarios, such as text-to-image generation. However, these two models have very different memory mappings, dataflows and mathematical operators, making it difficult to accelerate both types of models simultaneously. To address the forementioned challenges, we propose a multi-core programmable near-memory-accelerator and introduce an arbitration-free multi-port SRAM array to improve storage utilization while maintaining flexibility. To achieve performance comparable to compute-in-memory (CIM) designs, we use near-memory variable-precision multiplier-accumulators (NVMAC) to perform multiply-accumulate (MAC) operations tightly close to the memory to maximize the memory access throughput and support the mixed-precision neural network inference. We use a fine-grained instruction set architecture to support software sparsity and reduce overhead caused by coarse-grained non-MAC operations with low utilization. A chip is fabricated in a 28 nm process and achieves 6.3-to-101.4TOPS/W energy efficiency for Transformer model and 7.3-to-194.6 TOPS/W for CNN model, 1.2x to 4.2x compared with other state-of-the-art designs, while efficiently supporting both CNN and Transformer overloads.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 2

TALK #27.4 / 17:00-17:25

王扬

清华大学

王扬，博士，清华大学副研究员，入选中国电子学会青年人才托举、获得清华大学“未来芯片学者”，从事可重构智能计算芯片架构、存内计算芯片架构与三维集成智能计算芯片架构研究，作为负责人主持科技部重大项目课题/国家自然基金委青年基金等项目 7 项，近三年来，以第一/通讯作者发表 ISSCC/JSSC/VLSI 等论文 36 篇(6 ISSCC/5 JSSC/4 VLSI)，共发表学术论文 50 余篇，研究成果入选“中国芯片科学十大进展”，3 次获得“中国半导体学报十大进展提名奖”，获得 CCF CHIP Best Paper Award，ISSCC Highlight Paper；担任集成电路顶级期刊 JSSC/TCAS-I/TCAS-II 等审稿人。

TALK

A 28nm Speculative-Decoding LLM Processor Achieving 105-to-685μs/Token Latency for Billion-Parameter Models

LLMs face decoding bottlenecks. Speculative Decoding (SD) reduces latency via a small draft model for serial decoding and a large target model to verify in parallel. Despite this advantage, it still suffers from exponent redundancy, inefficient weights/KV, and hardware underutilization. We propose an SD LLM processor with three innovations: an exponent dual-reuse MAC, draft back-propagation target mixed-precision dataflow, and draft early start parallel compute, achieving 10.29× speed increase.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #28.1 / 15:45-16:10

冼世荣

澳门大学

冼世荣，现为澳门大学微电子研究院副院长(学术)，模拟与混合信号超大规模集成电路国家重点实验室副主任,以及电机及电脑工程系教授。他于欧洲施普林格出版了 1 本专著、持有 12 项专利及超过 170 篇高性能模拟集成电路领域的学术期刊和会议论文。

冼博士为以下高端国际会议的技术委员会会员，包括 IEEE CICC 会议数据转换器子委会主席，VLSI 会议技术委员会会员，A-SSCC 亚洲固态电路会议学生设计比赛评委副主席、ICTA 会议技术委员会副主席、IEEE 电路和系统期刊 II (TCAS-II) 的副主编。他是 2024-2025 年度国际 IEEE 固态电路协会(SSCS)的杰出讲师。他是 2011 年国家科学与技术进步二等奖共同得奖者之一(该奖为全澳门首次获得)。

TALK

Continuous-Time Pipelined Delta-Sigma ADC With DAC Image Prefiltering

This presentation reports a continuous-time (CT) pipelined delta-sigma (ΔΣ) ADC featuring a proposed pre-filtering scheme to tackle the DAC image issue. We introduce a fast-shunting route for high-speed DAC image current with a passive RC low-pass filter (LPF) on the quantization (QTZ) path. Together with another LPF on the signal path to align the delay, the CT front-end stage provides a residue signal with a small amplitude and smooth edges, relaxing the linearity requirements on the residue amplifier (RA) and the back-end stage. Specifically, the RC delay in the two LPFs are tracked over process variation, relaxing the signal leakage to the back-end. For the back-end stage, we utilize an all-pass filter (APF) analog delay in a 2nd-order CT cascade of integrators with feedforward (CIFF) ΔΣ modulator (DSM) with an input feedforward path. Such an APF can restore the unity signal transfer function (STF) under the influence of excess loop delay (ELD), thus simplifying the matching requirement between analog and digital domains' transfer functions.

Prototyped in 28-nm CMOS process, the proposed ADC operates with a clock of 3.2GHz, occupying an active area of 0.104 mm2. It exhibits a 72-dB dynamic range (DR) and a 68.5-dB peak signal-to-noise-and-distortion ratio (SNDR) over a 160-MHz bandwidth (BW). The modulator consumes 36.2 mW, yielding 165-dB Schreier figure-of-merit (FOMS) based on the SNDR.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #28.2 / 16:10-16:35

仲易

清华大学

仲易，现任清华大学电子工程系助理研究员，分别于 2013 年和 2020 年在北京理工大学获得学士和博士学位，2015 至 2018 年作为国家公派联合培养博士生在美国德州大学奥斯汀分校进行合作学术访问。2020 年至 2022 年在清华大学电子工程系从事博士后研究工作，在 2023 年入职清华大学电子工程系担任助理研究员。仲易主要的研究方向包括高速高能效模数转换器（ADC）、高性能时间域模数转换器、高性能自动化设计 ADC 等，近五年共发表国际高水平论文 30 余篇，其中顶级会议 ISSCC、顶级期刊 JSSC 等学术论文 10 余篇，是 JSSC、TCASI 等期刊审稿人，国内期刊《微电子学》青年主编。仲易博士在 2023 年曾获华为海思“最佳合作伙伴奖”。

TALK

A CMOS Hybrid Common-Gate Current-Integrating Sampler with >37dB SNDR Across 51GHz BW in a 128GS/s Front-End

This work proposes a CMOS hybrid common-gate current integrating sampler to address linearity, BW, and jitter limitations in prior wideband ADC front-ends. The front-end employs a hybrid common-gate V-I converter, transformer-coupled inductive peaking, and an automatic power-gating hold buffer, enabling 48.1dB SFDR and 38.6dB SNDR near its 52GHz BW-3dB. This work demonstrates superior SNDRBW (measured near BW3dB), outperforming prior samplers/ADCs reported in ISSCC/JSSC/VLSI with BW>30GHz.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #28.3 / 16:35-17:00

罗豪

深圳市中兴微电子技术有限公司

罗豪，2007 年本科毕业于华中科技大学，2012 年博士毕业于浙江大学，2019 年入职中兴微电子，负责高速高性能 ADDA 芯片和超高速 ADDA 芯片的研发和量产交付，发表 SCI 和 EI 收录论文 10 余篇，授权专利 25 项。

TALK

A 14b 20GS/s RF-Sampling DAC Achieving 70.4dBc IMD3 up to 8.9GHz

This work presents a 14b 20GS/s RF-Sampling DAC. By introducing a switch driver with process-and-temperature-adaptive (PT-adaptive) level shifting and enhanced low-crosspoint control, the DAC demonstrates an IMD3 of 83.5dBc at 7.2GHz and a maximum output power of 7dBm without negative supply. And an algorithm, named ISI-Minimizing Dynamic Element Matching (ISIM-DEM), is proposed to mitigate output distortion induced by inter-symbol interference (ISI) effect at 8.9GHz and 20GS/s.

INVITED TALK 邀请报告

2026 年 3 月 27 日 · 第 3 天

宴会厅 3

TALK #28.4 / 17:00-17:25

唐希源

北京大学

唐希源，北京大学助理教授、博士生导师。他分别于 2012 年和 2019 年在上海交通大学和德克萨斯大学奥斯汀分校（UT Austin）获得学士和博士学位。2015 至 2017 年期间，他于 Silicon Labs 担任芯片设计工程师。2019 至 2021 年期间，他在 UT Austin 从事博士后科研工作。他担任 ISSCC/A-SSCC 技术委员会成员和 IEEE Solid-State Circuits Letters 副主编。

TALK

High-Performance Time-Domain Capacitance-to-Digital Converters

Capacitive sensors are widely used in IoT applications and smart edge devices to detect a broad range of physical quantities, including pressure, humidity, acceleration, and proximity. These applications call for capacitance-to-digital converters (CDCs) that deliver high resolution, low latency, and outstanding energy efficiency.

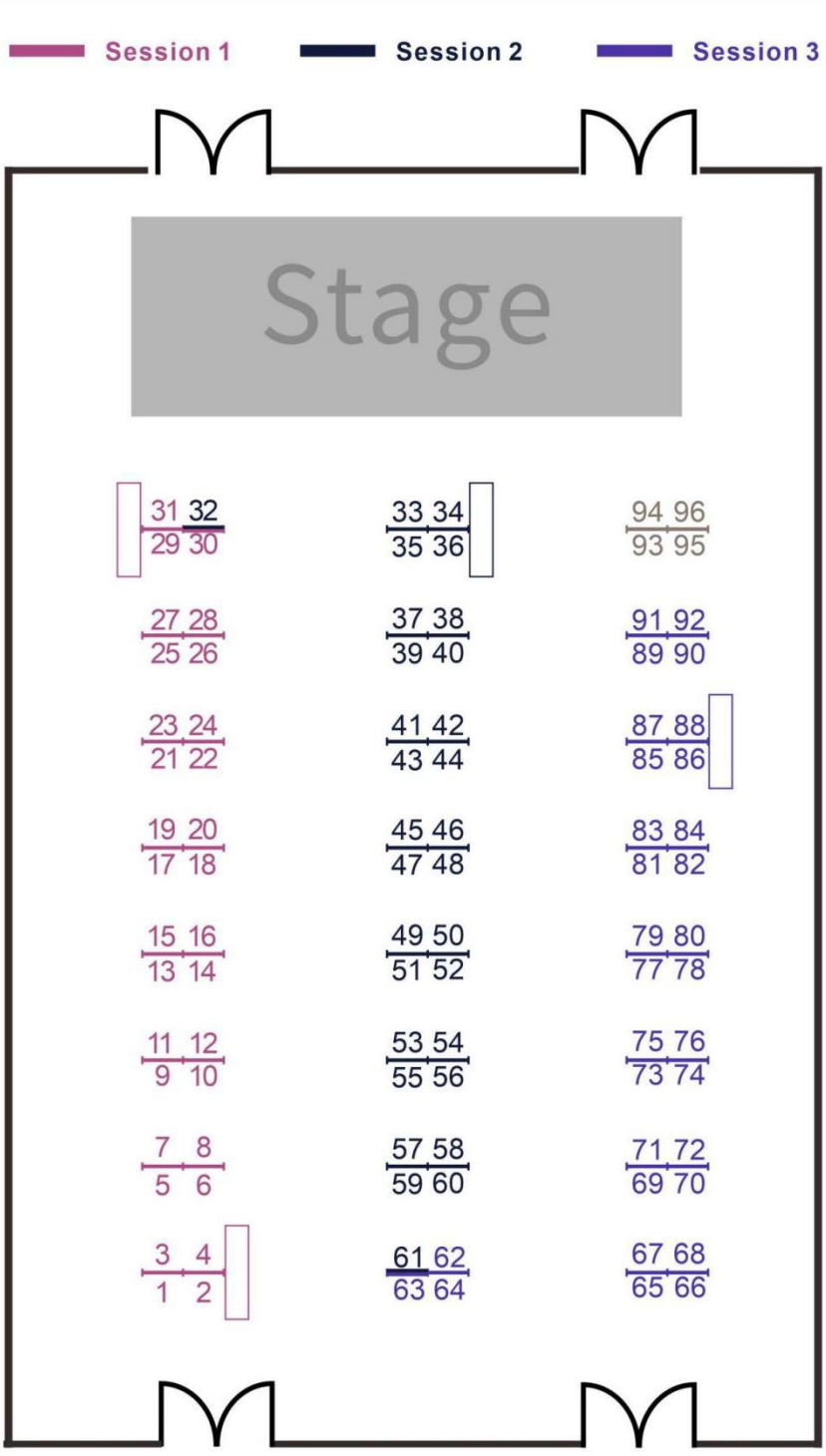
This talk will begin with an overview of the fundamental principles and key design trade-offs of capacitive sensor readout circuits, followed by recent research advances such as emerging converter architectures and time-domain quantization techniques. Several design examples will be presented, including double PFD quantizers and time-domain feedforward compensation. The talk will conclude with a discussion of future directions and opportunities in CDC design.

POSTER SESSION 学生海报展示

2026 年 3 月 25 日 19:00-21:00

宴会厅 3

Session 1: Connectivity and Clocking	P01-P31	玫红色区域
Session 2: Computing and Power Management	P32- P61	深蓝色区域
Session 3: Analog, Sensors and Data Converters	P62-P92	蓝紫色区域



Session 1: Connectivity and Clocking

P01 海报题目：A 10-72GHz SDR Receiver with Compact and Low-Phase-Noise LO Frequency Quintupler

报告人：白浩宇，北京大学
指导老师：廖怀林

摘要： Demands for 5G NR, 6G, autopilot radar, satellite communication and other emerging applications promote the development of compact receivers for easier phased-array integration and some communication protocols such as 5G n263 require receivers with over 70GHz bands [1-3]. Therefore, a multi-standard-supported SDR receiver with a small die area, a high RF bandwidth and high reconfigurability shows excellent adaptation for the potential demands [4,5]. In a multi-standard receiver, the orthogonal local oscillator (LO) accuracy directly affects the demodulation quality. However, the existing wideband orthogonal LO generators including XFMR-based IQ network, QVCO, and hybrid-path band selection show limitations such as high core area, high power consumption, or high spur interference [6,7]. Besides, the down-mixing scheme of RF signals over 40GHz like harmonic mixing shows relatively low conversion gain [8]. This work introduces a 10-72GHz receiver with only one inductor-less LO generator for multi-protocol applications. Phase interpolator and edge-combining switched-capacitor (SC) based frequency quintuple techniques are proposed to output 10GHz to 40GHz LOs while operating within 2-8GHz. For the 40-72GHz band, the RF signals are down-mixed two times with the same frequency to reduce the LO operating frequency to fRF/2. The first down-mixing process is performed with the image band at DC, achieving over 100dB image rejection ratio (IRR) through the transformer for input matching and then relieving the noise deterioration and image interference. This work describes a 10-72GHz, 26-48dB gain, and 19.7-23.7dBm OIP3 SDR receiver with a 0.068mm2 LO generator.

P02 海报题目：A 1.6-to-3.8GHz Reconfigurable FMCW Radar SoC with 81.5% Relative-Bandwidth PLL for Real-Time Life Detection in Disaster Response

报告人：蔡凡勋，北京航空航天大学
指导老师：张慧

摘要： A 1.6-to-3.8GHz FMCW radar SoC for real-time non-line-of-sight life detection is implemented in 40nm CMOS. An 81.5% BW ring-VCO PLL with DTC achieves 29.6kHz frequency error and 0.78-to-400MHz/μs chirp slopes. The TX integrates a 13.43dBm PA, while the RXRF features 8.1dB NF, baseband chain with 100dB-rejection SC-HPF at 1kHz and CT Δ-Σ ADC. A RISC-V core with FPU/VPU enables DSP, detecting people behind 6 walls and vital signs behind 2, occupying 7.65mm2 and consuming 0.395W.

P03 海报题目：A Charge-Domain Fractional-N ADPLL Based on Charge-Steering Sampling

报告人：陈炜一，中国科学技术大学
指导老师：胡诣哲

摘要： We propose a charge-domain fractional-N all-digital phase-locked loop (ADPLL) that employs charge-steering sampling (CSS) of a sinusoidal reference waveform. The well-known issue of quantization error in fractional-N operation is compensated by a capacitive digital-to-analog converter (CDAC), which

serves the conventional role of a digital-to-time converter (DTC). This CDAC is further merged with the inherent CDAC of a successive approximation register (SAR) analog-to-digital converter (ADC), which is exclusively used for digitizing the time-error mainly induced by the phase noise (PN). Initially, the combined CDACs are preset to VDD, and then discharged during a short digitally controlled oscillator (DCO)-divider-triggered pulse via a pseudo-differential MOS pair directly driven by the input reference sinusoidal waveform. Owing to the gentle slope of the reference waveform, the charge-domain fractional-N operation achieves a wide and linear time-error detection (TD) range. Furthermore, by reinterpreting the SAR ADC output using multi-bit midrise encoding, the effective time-to-digital conversion (TDC) gain is boosted by bang–bang (BB) effects while maintaining fast and robust locking. To accurately model the CSS current, we introduce a damped-sine waveform model incorporating harmonics, providing comprehensive insight into the CSS-TD gain, even with short-channel devices. Fabricated in 22 nm CMOS, the prototype achieves an rms jitter of 96 fs at 24 GHz with a reference spur of −60 dBc in integer-N mode, while 167.8 fs at approximately 24.5 GHz with a worst in-band spur of −47.8 dBc in fractional-N mode. The occupied area is only 0.08 mm^2.

P04 海报题目：A 25.48-29.25 GHz Rotary Traveling-Wave Oscillator Achieving -191dBc/Hz FoM at 10 MHz Offset Using RingInterleaved N/P Cross-Coupled Pairs in 22-nm CMOS

报告人：邓俊程，中国科学技术大学

指导老师：胡诣哲

摘要： This paper presents a 25.48–29.25 GHz rotary traveling-wave oscillator (RTWO) employing ring-interleaved nMOS/pMOS cross-coupled pairs along a Möbius ring to achieve low phase noise and high efficiency. By generating 16 phases with fewer active cells, the design reduces noise sources and power consumption while maintaining a simple switched-capacitor array. Reusing part of the Möbius ring as common-mode inductance enhances the return-path impedance, suppresses device noise, and improves the effective Q. Placing the switched capacitors between the nMOS and pMOS pairs introduces a partial inductive path for harmonic currents, mitigating flicker phase noise. Fabricated in 22-nm CMOS, the RTWO consumes 8.8 mW and occupies 0.03 mm^2, achieving a peak FoM of −191 dB at 10 MHz offset across a 13.7% tuning range, breaking the −190 dB barrier for RTWOs and approaching state-of-the-art LC oscillator performance.

P05 海报题目：A 0.068mm2 8.5-to-12.7GHz Complementary Dual-Core VCO with Auto-2nd-Harmonic-Tracking Technique Achieving 202.7dBc/Hz Peak FoMT and 0.9dB-FoM Variation at a 1MHz Offset in a 39.6% Tuning Range

报告人：杜欣橙，澳门大学微电子研究院

指导老师：殷俊

摘要： A complementary dual-core VCO with auto f2nd tracking is proposed to achieve consistently low PN and a high FoM over a wide tuning range (TR). Prototyped in 65nm CMOS, the proposed VCO achieves a peak FoM@1/10MHz of 190.7/193.5dBc/Hz with only 0.9/1.6dB variation across the TR from 8.5 to 12.7GHz (39.6%). The VCO occupies a compact area of 0.068mm2 including a small decoupling capacitor of 18pF.

P06 海报题目：A 25-31GHz Compact True Power Detector with >33dB Dynamic Range in 40nm Bulk CMOS

报告人：顾俊杰，复旦大学
指导老师：闫娜

摘要：This paper presents a compact mixer-based true power detector (PD) integrated within a Ka-band power amplifier (PA). The proposed compact PD avoids on-chip balun by sensing the voltage and current from the primary coil. Flicker noise suppression by current bleeding and linearity enhancement in the mixer expand the overall dynamic range of power detection. Intrinsic phase compensation in the detection paths removes the need of additional phase shifters, which further saves area cost. Fabricated in a 40nm CMOS process, the PD occupies a core area of 3520μm2 and maintains a dynamic range of >33dB across 25-31GHz with 12.1mW power consumption.

P07 海报题目：A Wideband Replicas-Rejection Digital Transmitter Using Joint-Digital-Analog Interpolation and Filtering in 28nm CMOS

报告人：胡春晓，复旦大学
指导老师：徐鸿涛

摘要：This article proposes a wideband replicas-rejection quadrature digital transmitter (Q-DTX) with joint-digital-analog interpolation and filtering techniques for high signal bandwidth applications. The digital polyphase architecture, swapping the order of interpolation and filtering, is employed to increase the sampling rate with low power consumption. The analog interpolation is integrated in the digital power amplifier (DPA), along with the digital-domain filtering, to further suppress sampling replicas. A wideband analog interpolation DPA with IQ-sharing and Doherty techniques is realized to enhance the efficiency at power back-offs (PBOs) while supporting wide frequency coverage. Implemented in 28-nm CMOS, this Q-DTX occupies only 0.88-mm2 core area. Powered by only one 1.1-V supply, this Q-DTX achieves 27.3-dBm peak output power with 30.5% system efficiency (SE) at 3.6 GHz. The 3-dB RF bandwidth range is 2.1–5.1 GHz. For Wi-Fi 40-MHz 64QAM signal with peak-to-average power ratio (PAPR) of 7.2 dB, this Q-DTX achieves 21.1-dBm average output power (Pavg) and 21.6% average SE with error vector magnitude (EVM) of －26.0 dB at 2.56 GHz. For Wi-Fi 80-MHz 256QAM signal with PAPR of 8.7 dB, it obtains Pavg of 17.5 dBm and average SE of 10.3% with EVM of －29.5 dB at 3.84 GHz. This Q-DTX achieves over 42-dBc sampling replicas rejection.

P08 海报题目：A Ka-band Multi-Beam Phased-Array Transmitter with Time-Modulation for PAPR Reduction and Physical Layer Security

报告人：蒋睿阳，清华大学
指导老师：贾海昆

摘要：This article presents a fully connected, timemodulated, multi-beam phased-array transmitter (TX), with reduced multi-beam peak-to-average power ratio (PAPR) and physical layer security. In the proposed time-modulated architecture, phase-shifted beam signals are sequentially fed into dedicated power amplifiers (PAs) at different time slots, contrasting with the conventional voltage-domain beam combination. Thus, the linearity and efficiency problems in conventional architecture are avoided, while

maintaining comparable effective isotropic radiated power (EIRP) performance. On the other hand, as each beam is transmitted in turn through different PAs, the phase compensation provided by phase shifters (PSs) deteriorates outside the main lobe region, providing the desired physical layer security. The proposed TX is fabricated in a 65-nm CMOS process, where a canceling-based time modulator and a synchronous clock distribution network are implemented to support the time modulation. A measured 20.9-dBm saturation output power (Psat) and 9.37% power-added efficiency (PAE) at 6-dB power back off (PBO) from Psat are achieved. A twobeam, four-element TX system is implemented for over-the-air (OTA) measurements. The dual-beam measurement reveals the expected PAPR reduction, with an output power improvement of 1.1 dBm in 16-QAM for the 5% EVM and a 1.5-dBm improvement for 256-QAM at 4% EVM. Furthermore, the time-domain combination also suppresses the inter-beam power contention, resulting in constant performance regardless of the power of the other beam. When PA is saturated by beam 1 signal, the EVM of beam 2 is improved by 5.2%. The desired physical layer security is proved in single beam measurement, where the EVM of the eavesdropper increases from 4.8% to 18% at a 30◦ angle.

P09 海报题目：A 26/28/37/39GHz Reconfigurable Fully Connected MIMO Receiver Front-End with On-Chip Diplexer Achieving 52-to-70dB Blocker Rejection

报告人：蒋徐颢，东南大学

指导老师：尤肖虎/李连鸣

摘要：A 24.25-to-29.5 / 37-to-40GHz fully connected MIMO receiver (RX) front-end for 5G FR2 that enables 52-to-70dB calibration-free inter-band blocker rejection and up to -5dBm blocker tolerance is introduced. A compact on-chip diplexer and band-selective network are integrated in the RF chain to reject undesired signals before the mixer. The RX can support concurrent dual-band or multi-stream single-band operation, and achieve 4.8Gb/s 64-QAM non-contiguous inter-band carrier aggregation operation.

P10 海报题目：A D-Band 5-bit SiGe Active Bidirectional Phase Shifter Achieving 0.09-dB RMS Gain Error and 0.86° RMS Phase Error

报告人：孔令峥，东南大学

指导老师：陈继新

摘要：This brief presents a D-band active bidirectional vector-modulation phase shifter (PS) based on a phase inverter embedded variable gain amplifier (PI-VGA). A Lange coupler and self-shielded Marchand baluns are utilized for IQ signal generation and combination, achieving bidirectional lowloss impedance matching. The switchless bidirectional PI-VGA incorporates compensation networks for parasitic reduction and intrinsic gain enhancement, enabling amplitude modulation and quadrant selection. The PS supports 5-bit 360◦ bidirectional phase shifting over 112-145 GHz. The measured minimum insertion losses are 7.5 dB and 9.5 dB for forward and reverse operations, with RMS gain errors of 0.09 dB. The measured minimum RMS phase errors for both directions are 0.91◦ and 0.86◦. The measured input 1-dB compression point amounts to 8 dBm and the core area of the PS is only 0.256 mm2, with an average power consumption of 81 mW under 3.3 V power supply. To the best of the authors' knowledge, this is

the first reported D-band active bidirectional PS, and the PS is suitable for terahertz time-division duplexing (TDD) phased arrays, offering a compact size and reduced insertion loss.

P11 海报题目：TIP: Turbo Implicit Pursuit Channel Estimator for mmWave MIMO Systems

报告人：李昌瀚，东南大学

指导老师：张川

摘要：Compressed-sensing (CS)-based channel estimation is a promising technology for future millimeter wave (mmWave) multiple-input–multiple-output (MIMO) systems, enabling significant pilot reduction and improved estimation accuracy. Channel estimators based on matching pursuit (MP) variants offer lower complexity compared with other CS algorithms, but suffer from high latency due to their iterative nature, hindering efficient hardware implementation. To mitigate this issue, this article introduces a turbo pursuit (TP) strategy that relaxes sequential dependencies in MP variants, enabling parallel processing and pipelined implementation. To demonstrate the effectiveness of TP, this article further introduces turbo implicit pursuit (TIP), a hardware-friendly instance of TP that leverages a prioritized gradient descent (GD) strategy for low-complexity least squares (LS) solving. A hardware auto-generator for TIP is then proposed using a formula representation approach, which constructs a parameterized hardware-algorithm design space and enables hardware-algorithm co-optimization. Our optimized 32 × 4 TIP MIMO channel estimator ASIC in 65-nm CMOS achieves 0.53-μs latency under 18.75% measurements. Compared with prior implementations of MP variants, this work achieves higher or comparable estimation accuracy with over 18% latency reduction and over 5× higher throughput to area ratio (TAR) for ASICs, and over 90% latency reduction with over 3× higher hardware efficiency for FPGAs.

P12 海报题目：Reflectionless Blocker-Canceling Mixer-First Receivers for Next-Generation Communication and Sensing Systems

报告人：李凯，天津大学

指导老师：王科平

摘要：1. This paper proposes a 6-18 GHz reflectionless blocker-canceling mixer-first receiver for satellite communication systems. By introducing a novel phase-compensation feedforward path, out-of-band blockers are effectively canceled and a reflectionless design is implemented to minimize the LO power consumption. The 65nm CMOS prototype achieves maximum out-of-band rejection of 55.6 dB, voltage gain of 8.9 to 11.6 dB, and NF of 11.2 to 17.6 dB while consuming 53 to 81 mW.

2. This paper presents two reflectionless blocker-canceling mixer-first receivers. By employing a reflectionless blocker-canceling technique with phase compensation, the trade-off between out-of-band (OOB) rejection and switch size is decoupled. Thus, switches with small-size can be used without sacrificing OOB rejection, and the power consumption of the local oscillator (LO) buffers is also reduced. Further, the phase compensation technique can accurately allocate the transmission zero, thereby enhancing the rejection of high-side TX leakage. Two receiver variants (Design-1 and Design-2), mainly differing in LO and baseband (BB) circuits, are fabricated in 65 nm and 40 nm CMOS technologies, with chip area of 0.99 mm2 and 0.7 mm2, respectively. Design-1 operates from 6-18 GHz, with a RF-to-BB conversion gain of 8.9-11.6 dB and a maximum high-side OOB rejection of 55.6 dB. Design-2 covers a

wider range of 6-26 GHz, achieving a RF-to-BB conversion gain of 7.2-9.9 dB in wide mode and 7.0-9.5 dB in narrow mode, with a maximum high-side OOB rejection of 50.8 dB in both modes. Design-1 has a BB BW-3dB of 225 MHz, while Design-2 achieves 320 MHz in wide mode and 210 MHz in narrow mode, along with a steeper transition-band roll-off and flatter passband. The power consumption of Design-1 and Design-2 are 53-81 mW and 61-76 mW, respectively.

3. This paper presents two RF-to-Millimeter-Wave blocker-tolerant mixer-first receivers. A feedforward path with phase compensation is designed parallel to the main path to cancel the out-of-band (OOB) blocker. It can break the trade-off between mixer switch size and OOB rejection, thereby simultaneously achieving high transition-band roll-off and excellent LO-to-RF isolation. In addition, a balanced input network is employed to achieve broadband input matching. LC tanks are introduced into the second design to further improve the OOB rejection. Fabricated in a 130 nm SOI CMOS process, the proposed receivers achieve a transition-band roll-off of 40 dB/decade and OOB rejection of 25-55 dB in the frequency range of 10-30 GHz. It also achieves a maximum LO-to-RF isolation of 61.7 dB at 11 GHz.

P13 海报题目：A 180-to-240Gb/s Analog-Intensive PAM-4 Transmitter with 0.70pJ/b Analog Power Efficiency in 65nm CMOS

报告人：林子逸，清华大学

指导老师：贾海昆

摘要：This paper presents a 180-240Gb/s analog-intensive PAM-4 transmitter in 65nm CMOS process. A three-stage cascaded 2-to-1 analog MUX (AMUX) is employed to reduce the complexity and therefore the parasitic capacitance of both output and internal high-speed nodes. Reconfigurable 4-tap FFE, current injection, and dual T-coil techniques are proposed to enhance the output swing and the bandwidth. The transmitter achieves 0.70pJ/b analog energy efficiency at a 240Gb/s data rate.

P14 海报题目：A 47.0Tb/s/mm 112Gb/s/pin PAM4 Single-Ended Transceiver Featuring 4-Aggressor Crosstalk Cancellation and Supply-Noise Tolerance for Short-Reach Memory Interfaces

报告人：刘谦，南京大学

指导老师：杜源

摘要：This paper presents a five-lane 112Gb/s/pin PAM4 single-ended transceiver in 28nm CMOS for high-density short-reach memory interfaces. Low-power triple-equalization, 4-aggressor shape-fitting crosstalk cancellation and supply-noise-tolerant clock distribution networks are involved to improve the signal integrity. The design demonstrates robust performance against severe crosstalk and supply noise, achieving an energy efficiency of 0.52pJ/b and an edge density of 47.0Tb/s/mm.

P15 海报题目：A 21.6fsrms-Jitter, − 260.7dB-FoM Fractional-N PLL Enabled by an Intrinsically Linear Variable-Slope SPD for Quantization Error Cancellation

报告人：刘彦超，复旦大学

指导老师：倪熔华

摘要：This work presents a fractional-N PLL with an intrinsically linear variable-slope sampling phase detector for quantization error cancellation. Linearity, noise, and power efficiency are improved by

eliminating the edge-restoration buffer. Combined with the proposed charge-injection based nonlinearity compensation, the 14GHz prototype PLL achieves 21.6fs rms jitter, -260.7dB FoM and -67.4dBc worst-case spur in fractional-N mode with 18.1mW power consumption in 28-nm CMOS process.

P16 海报题目：A 14GHz Chopper-Refolding Sampling PLL Achieving 33.8fsrms and 80.8dBc Reference Spur with a kT/C-Noise-Cancellation SPD

报告人：刘翌晨，清华大学

指导老师：王燕

摘要：A 14 GHz chopper-refolding sampling PLL is implemented in 28 nm CMOS, integrating a kT/C noise cancellation sampling phase detector (SPD) and a self-injection VCO with harmonic-impedance expansion. The SPD decouples jitter and phase detection gain, while the chopper-refolding scheme filters flicker noise. The VCO enables high FoM without manual tuning, achieving 33.8 fsrms jitter, -80.8 dBc spur, 16.8 mW power, and competitive jitter performance among integer-N PLLs.

P17 海报题目：A 16Gb/s/pin 0.51pJ/bit Single-Ended NRZ Transceiver with Distributed Dual-Loop VDDQ Ripple Compensation and Dynamic Clock Duty Cycle Calibration for Memory Interfaces

报告人：罗昀斌，复旦大学

指导老师：刘琦/江文宁

摘要：A 16Gb/s/pin 0.51pJ/b single-ended NRZ transceiver with distributed dual-loop compensation (DDLC) for VDDQ-ripple suppression and dynamic duty-cycle calibration (DDCC) for robust clocking is presented. The DDLC locally regulates VDDQ with a shared lowpower LDO, reducing the required decoupling capacitor by 91.4%, while improving horizontal and vertical eye margins by 61% and 36%. Demonstrated on five channels, the proposed DDLC scales naturally to larger DQ counts for high-density memories.

P18 海报题目：20.10 A 214-to-242GHz Miniaturized Co-Packaged PA-Antenna Array with 29dBm Lens-less EIRP in a 0.13μm SiGe Process

报告人：孟千起，东南大学

指导老师：洪伟

摘要：This work presents a miniaturized, high-power, and wideband THz PA-antenna array,realizing 29dBm lens-less peak EIRP from 214 to 242GHz. To improve the BW and Psat of the PA, a folded 10th-order power-splitting/combining and staggered-matching method is proposed, achieving 17.4dB peak gain and 16.5dBm peak Psat from 160 to 248GHz. To address the efficiency and BW limitation of the AoC, a co-packaged ULP slot-patch antenna is integrated, extending the radiation efficiency to 66.7% and BW to 36GHz.

P19 海报题目：A 0.06mm2 14.7-to-20.2GHz Quad-Core VCO Enabled by the Folded Circular Transformer Achieving 201.1dBc/Hz FoMT and 203.4dBc/Hz FoMA

报告人：欧天政，澳门大学/复旦大学

指导老师：罗文基

摘要：This paper proposes a quad-core oscillator utilizing a folded circular transformer that utilizes both

magnetic and electric coupling for core synchronization, greatly reducing the area and phase noise penalty of quad-core VCOs. Moreover, the proposed transformer simultaneously enhances common-mode and differential-mode quality factors. Fabricated in 28nm CMOS, the proposed VCO covers 14.7-to-20.2GHz (31.5%) within an area of 0.06mm2 while consuming 5.3mW power. It achieves FoMA and FoMT@10MHz offset frequency of 203.4 and 201.1dBc/Hz at 15.8GHz.

P20 海报题目：A 128mW 2x4 Radar-on-Chip with Forward-ΔΣ DPLL-Locked Multi-Injection RTWO in 22nm CMOS Enabling ADCFree Digitization and PS-Free Beamforming Demonstrated in In-Cabin Vital-Sign Monitoring

报告人：彭集，中国科学技术大学
指导老师：楼立恒

摘要：A 2×4 phased-array SIL radar-on-chip in 22nm CMOS is demonstrated for in-cabin vitalsign monitoring. Built on a forward-**ΔΣ** DPLL-locked multi-injection RTWO at 20GHz, it concurrently serves as (de)modulator, beamformer, and data converter. The chip delivers 0dBm CW/PMCW for respiration cancellation, boosting SFDR by 9dB for cardiac extraction. RTWO-based beamforming covers ±48° FoV in ~15° AoA step. The 1.42mm2 chip consumes 128mW and achieves RR/HR errors <±6bpm with 1.2mW DSP on-chip.

P21 海报题目：A 40-nm CMOS Phase-Tunable Four-Phase Injection-Locked Ring VCO Utilizing Unbalanced Feedforward Topology Achieving − 211.1- to − 207.3-dBc/Hz FoMA Over Differential/Orthogonal Phase Range of − 90.0° to 80.9°/− 69.6 °to 76.5°

报告人：汤鹊志，上海交通大学
指导老师：金晶

摘要：This article proposes a phase-tunable four-phase injection-locked ring voltage-controlled oscillator (RVCO) voltage-controlled oscillator (VCO), where the functions of muti-phase generation and clock phase tuning are merged in the VCO, and no additional phase-tuning block is needed in the clock system. The ring oscillator (RO) utilizes a novel unbalanced feedforward topology with high power and area efficiency. By tuning the ratio of the feedforward current to the input current at each stage of the oscillator, the phase of the four-phase output clock can be precisely and flexibly controlled. The proposed VCO achieves an inherent phase-tunable/calibration feature for desired phase outputs, without the need for additional back-end calibration circuits, avoiding the deterioration of noise performance and the increase in power consumption in the clock path. The injection locking technique is applied in the proposed VCO to maintain good noise performance over a wide frequency and phase-tuning range. The VCO prototype in a 40-nm CMOS can cover the frequency range of 3.27.5 GHz and achieves a wide differential/orthogonal phase-tuning range of 90.0° to 80.9°/69.6° to 76.5° and a small phase-tuning step of 0.14°/mV on average. Over the full phase range, the VCO achieves an FoMA of 211.1 to 207.3 dBc/Hz, which is the best FoMA among the state of the arts.

P22 海报题目：A 220-GHz Low-Noise CMOS Receiver Utilizing Noise Cancellation and Gain Enhancement

报告人：王丽娟，东南大学

指导老师：胡三明

摘要： This paper presents a 220 GHz low noise receiver (RX) implemented in 40 nm bulk CMOS process with fT/fmax = 300/270 GHz. The RX comprises a 2-stage low noise amplifier (LNA), a single-balanced active mixer, and an intermediate frequency amplifier. To enhance gain and suppress noise of LNA, a tri-coil gm-boosting network and an inductors-assisted differential noise-cancellation network are proposed. The core of LNA is designed using a lossy-Gmax-core to simultaneously achieve noise and gain matching. The proposed active mixer integrates a noise-self-cancellation network embedded between gate and source of the switch-stage and utilizes the lossy-Gmax-core as the gm-stage, improving both conversion gain (CG) and noise performance. The RX achieves a CG of 17.8 dB, a minimum noise figure of 11.8 dB, an input 1-dB compression point (IP1dB) of -24.7 dBm, while consuming 35.5 mW. The design occupies a total area of only 0.2 mm^2, with a core area of 0.078 mm^2. To the best of the authors' knowledge, this work demonstrates the lowest reported noise figure among CMOS receivers operating above 200 GHz.

P23 海报题目：A Low Phase Noise and High-Efficiency Biharmonic Class-F− 1 VCO With Improved Waveform Shaping

报告人：吴悦，澳门大学

指导老师：彭亚涛

摘要： This article presents an inverse class-F (class-F−1) voltage-controlled oscillator (VCO) architecture that achieves a higher figure of merit (FoM) compared with the reported RF harmonic VCOs. The design conditions for FoM improvement in biharmonic VCOs (with sole 2nd harmonic) are analyzed. To meet the conditions revealed, a distributed dual-mode resonator (DMR) without magnetic flux cancellation, featuring simultane ously high 1st and 2nd harmonic impedances, is introduced to realize the proposed class-F−1 VCO, enabling improved phase noise (PN) with reduced power consumption. The proposed structure is able to boost the 2nd harmonic voltage components while suppressing the detrimental misaligned 3rd harmonic voltage in the output waveforms by introducing significant 2nd harmonic voltage (VG2) at the gates. Consequently, the waveform exhibits an extended flat region of the waveform where the impulse sensitivity function (ISF) approaches zero, leading to reduced noise-to-PN conversion, even without excessive D-to-G voltage gain. Meantime, the introduced VG2 enlarges the zero-current (ZC) zone in the output current waveform, thus improving the power efficiency. Two prototypes of VCO targeting room-temperature (RT) and cryogenic applications are designed and measured to verify the proposed architecture. The RT VCO achieves a frequency tuning range (FTR) from 9.37 to 10.86 GHz, delivering state-of-the-art PN of −143 dBc/Hz at a 10-MHz offset, and attaining a peak FoM of 198.9 dBc/Hz. The cryogenic VCO measured an average FoM of 210.2 dBc/Hz under sub-1 mW at 4.2 K.

P24 海报题目：A CMOS Low-Noise Fast-Settling BM-TIA with CM-Post-Amplifier Chip Connectivity for 50G-PON

报告人：夏翼飞，西安交通大学

指导老师：李丹

摘要： In this paper, we address the noise and settling time challenges in CMOS BM-TIA for low cost, which

also highlights the unique capability to drive a continuous-mode (CM) post amplifier chip in the BM environment.

P25 海报题目：A 6GHz Quadrature Digital Transmitter Supporting 1GHz Signal Bandwidth with <-40dB EVM Floor and >55dB Dynamic Range in 28nm CMOS

报告人：谢锋，复旦大学
指导老师：殷韵/徐鸿涛

摘要：A 6GHz quadrature DTX supporting a 1GHz signal bandwidth is presented in 28nm CMOS, where static and dynamic nonlinearities are carefully optimized. Occupying a core area of 0.67mm2 and packaged in a fanout SiP, the DTX delivers 23.1dBm peak output power with a 30.3% peak PAE at 6.0GHz, and the 1dB RF bandwidth is from 5.7 to 6.5GHz. For 1GHz 64-QAM signals, it achieves 18.0dBm Pavg and 16.2% PAEavg with -25.5dB EVM. The dynamic power range is >55dB, and its EVM floor is -40.8dB.

P26 海报题目：A 2.68-pJ/b 135-GHz OOK Transmitter With Class-F VCO in 28-nm CMOS for High-Speed Link

报告人：严铮，东南大学
指导老师：陈继新

摘要：This work presents a 135-GHz high-speed ON–OFF keying (OOK) transmitter (TX) chip fabricated in 28-nm CMOS technology. A simplified 45-GHz Class-F voltage-controlled oscillator (VCO), with low-power consumption and implicit tripling characteristic, is proposed to generate a 135-GHz local oscillator (LO) signal. A Gilbert-cell modulator is utilized to support highspeed modulation and provide a high ON/OFF ratio. Cascaded inverters are utilized to reshape the baseband signal distorted by external metal interconnects. Moreover, amplifiers based on neutralized gm core are used to boost the third harmonic signal at 135 GHz and amplify the D-band modulated signal. The TX was used to establish a wireless link via on-board Vivaldi antennas. Data rates of 29 and 30 Gb/s were achieved with an energy efficiency of 4.4 and 4.25 pJ/bit, respectively, over a 2-cm over-theair (OTA) distance. In a low-loss channel such as bonding-wire connections, a data rate of 32 Gb/s with an energy efficiency of 2.68 pJ/b was achieved. PRBS31 was used to verify that the TX chip is suitable for applications requiring long pseudorandom binary sequence (PRBS) data streams. To the best of authors' knowledge, this work achieves the highest error-free OTA data transmission rate among D-band OOK TX chips, providing a feasible CMOS solution for sub-terahertz (sub-THz) high-speed point-to-point wireless or wireline communication.

P27 海报题目：A 140GHz Full-Duplex CMOS Transceiver with Metasurface-Integrated Self-Interference-Cancelling Antenna Supporting 16Gb/s 16QAM Dual-Mode Bidirectional Communication

报告人：杨佳伟，紫金山实验室
指导老师：胡三明

摘要：This paper presents a 140GHz CMOS transceiver for both full-duplex and frequency-division duplex communication. By proposing self-interference (SI)-cancelling antenna and dual-polarized metasurface, the design achieves measured EIRP of 26.8dBm and SI suppression of >49dB, therefore providing enough

SINR for transceivers. A 16Gb/s 16QAM simultaneous bidirectional communication over 1m is demonstrated, achieving the highest data rate reported for full-duplex dual-mode transceivers in the comparison table.

P28 海报题目：A 0.184mm2 WW-Band Single-RTWO-Based Subharmonic RX Achieving 3.72 dB-NF and I/Q Mismatch < 0.8° in 22 nm CMOS

报告人：杨绍琦，中国科学技术大学

指导老师：胡诣哲

摘要：We present a W-band sub-harmonic IQ receiver (RX) featuring a single rotary traveling-wave oscillator (RTWO) integrated with an ADPLL. It addresses key challenges in conventional mmwave direct-conversion RXs: LO generation and distribution with poor phase noise (PN), IQ mismatch, high power consumption, large area, and high dc offset. RTWO multimodes are suppressed via asymmetric capacitance in the crossover of the Möbius ring. Fabricated in 22 nm CMOS, the RX demonstrates a 3.72 dB noise figure (NF), IQ mismatch <0.8◦using a bundle-based calibration. It occupies a tiny area of 0.184mm2 and has a total power consumption of 56.7 mW, including the ADPLL.

P29 海报题目：A PLL Technique: Charge-Steering Sampling

报告人：杨宇豪，中国科学技术大学

指导老师：胡诣哲

摘要：This article introduces a charge-steering sampling (CSS) technique for time-error detection (TD), an equivalent of phase detection (PD), in phase-locked loops (PLLs). The CSS mechanism presets the input capacitors of a successive approximation register (SAR) analog-to-digital converter (ADC) to VDD and subsequently discharges them during a reference-triggered pulse through a pseudo-differential MOS pair directly driven by the oscillator. The resulting differential-mode (DM) charge residue, proportional to the time error, is digitized by the ADC to support all-digital PLL (ADPLL) operation. The proposed technique simultaneously achieves high-TD gain for low jitter, the excellent oscillator isolation for reduced reference spur, and multi-bit digital TD output for fast locking, fully leveraging the capabilities of advanced CMOS technology. A digital loop filter (DLF) featuring a dead zone (DZ) in the integral path is introduced to mitigate potential conflicts with the proportional path. To accommodate the short-oscillator period Tosc at millimeter-wave (mm-wave) frequencies, we propose extending the CSS pulsewidth to 1.5Tosc . In addition, a damped-sine waveform model for the CSS current is developed, providing deeper insights into the high-TD gain characteristics. The comprehensive noise analysis of the CSS is conducted using a multirate timestamp model, identifying contributions to the output phase noise (PN). Fabricated in 22-nm CMOS, the 18.8–23.3-GHz CSS-ADPLL prototype achieves 63-fs rms jitter, −52.4-dBc reference spur, and a figure of merit (FoM) of −254 dB, while consuming 9.95-mW total power, with only 1.3 mW allocated to the loop. For an initial frequency error of 200 MHz, the system achieves a locking time of 0.61 μs, benefiting from the combined effects of a counter-based frequency-locked loop (FLL) (0.27 μs) and the multi-bit digital output of the CSS-ADPLL (0.34 μs).

P30 海报题目：A 24-to-27.5GHz Self-Adaptive Load-Modulated Balanced Amplifier for Integrated Communication, Sensing, and Power Transfer Scenarios

报告人：于路琦，东南大学
指导老师：余超

摘要：A 24-to-27.5GHz self-adaptive load-modulated balanced amplifier (SALMBA) is proposed for 6G integrated communication, sensing, and power-transfer scenarios. Based on the proposed self-adaptive power divider, the power divide ratio can dynamically change according to the input power levels, and the back-off PAE and saturated performance of the SALMBA can be significantly improved. The SALMBA achieves the saturated PAE of 28.5 to 33%, and 10dB OPBO PAE of 15.3 to 22.1% over 24 to 27.5GHz.

P31 海报题目：BayesBB: A 9.6-Gb/s 1.61-ms Configurable All-Message-Passing Baseband Accelerator for B5G/6G Cell-Free Massive-MIMO Systems

报告人：张艺，东南大学
指导老师：张川

摘要：Cell-free massive multi-input multi-output (CF-mMIMO) has emerged as a promising alternative for the forthcoming beyond 5G and 6G (B5G/6G) systems. As an imperative part of supporting B5G/6G applications, baseband(BB) chips encounter more challenging key performance indicator (KPI) requirements. To achieve the B5G/6G goal of higher than 8-Gb/s/user throughput, less than 2-ms latency, and configurable hardware, a Bayesian inference-based all-message passing baseband-accelerator (BayesBB) is presented in this article. Benefiting from the pipelined and fully unfolded all message-passing architecture, BayesBB delivers three unexplored merits: high throughput (9.6-Gb/s), low latency (1.61-ms), and good configurability. Specifically, a ten-gigabit ethernet (XGE) interface with 10.3125-Gb/s SerDes is used, resulting in 9.6-Gb/s throughput. A fully unfolded MIMO-BP detector achieves a detection latency of 1.44-ms, contributing to chip latency of 1.61-ms. A configurable architecture is designed, supporting various B5G/6G applications, for example, the decoding of both 3GPP low-density parity-check (LDPC) codes and polar codes. As a system-level implementation, tests have verified that 16 arrays of BayesBB can handle the BB processing of a 128 × 128 CF-mMIMO system with commercial setups, delivering 9.6-Gb/s throughput and >100-b/s/Hz spectrum efficiency (SE).

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P32 海报题目：A 28 nm 68.6TOPS/W Folded-Differential SwitchedCapacitor FIA-Based SRAM CIM Macro With Scalable MAC Sizes for Tiny-ML Inference,

报告人：陈仲豪，清华大学

指导老师：杨华中

摘要： This paper presents a switched-capacitor SRAM CIM macro optimized for TinyML inference. Key features include: 1) an area-efficient folded-differential multiply-andaccumulate (FD-MAC) scheme to double the signal margin; 2) a closed-loop floating-inverter amplifier (FIA)-based charge accumulation technique for SNR enhancement and MAC voltage integration; and 3) a sparsity-aware multi-step MAC method to reduce A/D conversions and improve utilization. Fabricated in a 28nm process, the 32kb prototype achieves 68.7 TOPS/W energy efficiency and 1.74 TOPS/mm2 area efficiency in 8-bit mode.

P33 海报题目：A Cryogenic HBT-CMOS Temperature Sensor Operating From 4 to 70 K

报告人：邓宸，澳门大学

指导老师：彭亚涛

摘要： In current cryogenic temperature sensor (cryo-TS) systems, the sensing front-end and readout circuits typically operate in cryogenic and room-temperature environments, respectively. This paper proposes a scheme to integrate both the front-end devices and readout circuits of cryo-TS within the cryogenic environment to achieve lower noise, digital fan-out of temperature information, and cost reduction. We employed the silicon-germanium (SiGe) heterojunction bipolar transistors (HBT), which demonstrated excellent linearity and current gain even at cryogenic temperatures, as the sensing front end of the cryo-TS and a Zoom-ADC as its readout circuits. A redundancy bit is introduced in the cryogenic readout ADC to avoid temperature misjudgment. The design methodology and key considerations for implementing cryogenic readout analog circuits are presented. Implemented in a 65 nm CMOS process, the cryo-TS achieved a 1-point-trimmed (at 40 K) inaccuracy of ±0.54 K (3σ) from 4 K to 70 K under a supply current of 22.13 μA.

P34 海报题目：An Area-Efficient High-Precision Analog Front End for Battery Management System

报告人：邓宽，同济大学

指导老师：吴江枫

摘要： An analog front end (AFE) for monitoring the voltages of a stack of sixteen Li-ion batteries is presented. Each cell has a conversion voltage range of 0 to 5 V, allowing for a stack maximum input voltage of up to 80 V. The gate voltage bootstrap switch in high-voltage applications accurately measures battery voltage, reducing nonlinear sampling errors and significantly shrinking circuit size by omitting LDMOS devices. Furthermore, the high voltage switch charge injection cancellation is adopted to counteract the error introduced by the asymmetric sampling switches. All sixteen channels were sampled and amplified within 16 μs. The AFE is fabricated using a 0.18 μm high-voltage BCD process, and the total circuit area is 0.32 mm2. The measurement error for the 16-channel battery voltage is within 1 mV.

P35 海报题目：Algorithm-level Approximate Computing-in-Memory (AACIM) Chip and Compiler

报告人：刁海康，北京大学
指导老师：唐希源

摘要： With the rapid advancement of edge AI, the complexity of tasks on edge devices is continually increasing, demanding better efficiency and precision from AI accelerators. Pre-aligned floating-point computing-in-memory (FP CIM) has been proposed to achieve high-precision neural network (NN) computations based on floating-point (FP) data precision. However, the complex digital circuitry required for integer (INT) mantissa multiply-accumulate (MAC) computation and exponent alignment severely limits the efficiency and throughput of FP CIM. This work proposes an energy- and area-efficient computing-in-memory (CIM) engine for one-shot FP NN inference and on-device fine-tuning. To improve the throughput of FP CIM, a one-shot compute scheme is proposed to perform FP operation within one cycle. It adopts the multiply-less NN instead of the multiply-based NN to simplify the integer mantissa MAC to minimum selection. A customized 8-bit parallel minimum selector is also designed to further reduce the parallel computation cost. To simplify the FP/INT conversion process, an input-weight co-alignment workflow is proposed to eliminate maximum exponent selection and simplify mantissa shifting logic. To minimize the inference accuracy loss caused by environmental changes, a lightweight on-device fine-tuning core (ODFC) is designed to support online weight updates. The 28-nm fabricated chip achieves an energy efficiency of 128 TFLOPS/W and a computational density of 7.02 TFLOPS/mm2 at BF16, representing a 4.1× and 3.4× improvement over previous state-of-the-art works, respectively.

P36 海报题目：A 14.08-to-135.69Token/s ReRAM-on-Logic Stacked Outlier-Free Large-Language-Model Accelerator_x000b_with Block-Clustered Weight-Compression and Adaptive Parallel-Speculative-Decoding

报告人：董平成，香港科技大学
指导老师：郑光廷

摘要： This work presents a 55nm speculative decoding-based LLM accelerator with bumping-based face-to-face ReRAM-on-logic stacking technology. It features a local rotation unit for outlier-free low-bit quantization, a stacking-aware PNM architecture co-designed with blockwise vector quantization to reduce weight EMA overheads, and an adaptive parallel speculative decoding scheme with out-of-order scheduler for high resource and bandwidth utilization. Our chip achieves 14.08-135.69token/s and 4.46-to-7.17× speedup over vanilla speculative decoding.

P37 海报题目：A Piezoelectric Energy Harvesting Interface With Type Detection and Variable-Duty-Cycle-Based MPPT for Periodic and Shock Vibrations

报告人：冯一鸣，复旦大学
指导老师：曾晓洋

摘要： This paper presents a novel multi-mode energy harvesting interface system designed to optimize energy harvesting in dynamic mechanical environments, such as periodic and shock vibrations. The system proposes the integration of vibration type detection (VTD) mechanism, a variable duty cycle-based maximum power point tracking (MPPT) algorithm, and an energy extraction cease-time determination (EECTD) module, enabling adaptive energy harvesting strategies based on varying vibration conditions.

The VTD mechanism classifies vibrations into periodic and shock types, facilitating tailored energy harvesting strategies. The variable duty-cycle-based MPPT algorithm dynamically adjusts the rectifier's duty cycle based on the input conditions, ensuring efficient energy conversion under both periodic and shock vibrations. In the case of shock vibrations, the EECTD module halts energy extraction during negative power regions to minimize control power losses. Experimental results demonstrate that, compared to conventional full-bridge rectifiers (FBR), the proposed system enhances energy harvesting by 6.03 times under shock vibrations and by 7.69 times under periodic vibrations. By incorporating mode switching and optimized energy harvesting tailored to different vibration types, the proposed system offers a more efficient and adaptable solution.

P38 海报题目：SpikeRAM: A 48.1pW/synapse/b Event-driven Spiking Compute-Near/In Memory Processor with Neuromorphic Sensor Enabling Life-Long On-Chip Learning

报告人：付皓天，香港科技大学（广州）
指导老师：程伯骏

摘要：Edge perceptual SoCs increasingly demand high energy efficiency, strong privacy protection, and adaptability for real-world tasks involving power-hungry applications, sensitive data, and diverse users and environments. To address these requirements, we propose SpikeRAM, a neuromorphic sense–memory–compute system with on-chip learning, tightly integrated with an event vision sensor. SpikeRAM features three key characteristics: (1) Near-sensor computing with event-driven convolution operations. (2) One time-window triggered e-OTBP learning algorithm. (3) Gray-code encoded weights with ternary gradients for efficient on-chip learning. Benefiting from these designs, SpikeRAM achieves highly energy-efficient real-time inference with a power density of 48.1pW/synapse/bit. Meanwhile, it maintains over 90% learning accuracy while reducing learning memory and computational cost by more than 24 times, and decreasing the average memory programming times by 86.3%. The effectiveness of SpikeRAM is demonstrated on practical applications such as event-based signature verification.

P39 海报题目：A 24-W 91.5% Peak Efficiency All-in-One Dual-Loop Controlled Quasi-Resonant Isolated DC–DC Converter With Adaptive Peak Current and Valley-Hysteresis-Locking Techniques

报告人：郭子宾，西北工业大学
指导老师：马彦昭

摘要：This brief presents an all-in-one isolated DC-DC converter combines a primary flyback controller, secondary synchronous rectifier and digital isolator on a single chip. The converter adopts quasi-resonant (QR) peak current mode control with valley-hysteresis-locking (VHL) method. The adaptive peak current and VHL techniques could prevent sudden frequency hopping at some load point. Additionally, a down-hill detection method in the valley detector ensures accurate valley switching operation. With these proposed techniques, the converter could realize quasi-resonant under different load conditions. The chip has been fabricated with a 0.18 μm BCD process, and the primary and secondary control chips occupy the area of 1.04 mm2 and 0.62 mm2, respectively. The converter delivers 12 V output with a maximum current of 2 A, achieving a peak efficiency of 91.5%.

P40 海报题目：A 22-nm 109.3-to-249.5-TFLOPS/W Outlier-Aware Floating-Point SRAM Compute-in-Memory Macro for Large Language Models

报告人：何斯琪，复旦大学
指导老师：朱浩哲

摘要： Large language models (LLMs) have demonstrated exceptional performance in complex artificial intelligence (AI) tasks. However, their rapidly increasing parameter sizes lead to significant communication and computational overhead, posing challenges to the energy efficiency (EEF) and memory footprint of AI processors. Compute-in-memory (CIM) architecture has emerged as a promising solution to alleviate bandwidth constraints and improve EEF. Nonetheless, both integer (INT) and floating-point (FP) CIM implementations struggle with the trade-off between accuracy and memory requirement when applied to LLMs. Outlier-aware quantization (OAQ), which employs low-precision formats for normal values and retains FP formats for high-magnitude outliers, has proven effective in matching the accuracy of full-FP baselines and has become a mainstream approach for efficient LLM deployment. Therefore, this work presents OA-CIM, an SRAM-based digital CIM macro that facilitates element-wise hybrid processing of BF16 outliers and INT4 normal values. The major contributions are: 1) an LUT-based multiply-and-accumulate (MAC) circuit design, which supports efficient FP/INT-compatible (FIC) MAC operations; 2) an xor-sharing non-maximum exponent gating scheme that reduces latency and area by bypassing unnecessary exponent comparisons in FP dataflow; and 3) a sparsity-aware readout circuit with distribution-offset weight encoding (DOWE) to mitigate the power-intensive charging/discharging process on the bitline. A 22-nm 512-kB 8T SRAM OA-CIM prototype is fabricated, which achieves an EEF of 346.6 TOPS/W in INT4 mode and 249.5 TFLOPS/W in outlier mode, representing a 2.7× to 3.1× improvement over state-of-the-art mixed-precision CIMs.

P41 海报题目：HR-DCIM: High-Reliability Floating-Point Digital CIM Architecture with Unified Low-Cost Iterative Error Correction

报告人：何祯，清华大学
指导老师：尹首一

摘要： Digital computing-in-memory (CIM) is a promising computing paradigm for neural networks (NN) acceleration. However, during the actual deployment process of digital CIM chips, we find that existing digital CIM designs face the severe computing reliability issue, which is crucial for real product development but remains underexplored. Thus, this work pioneers a systematical computing reliability analysis for digital CIM across off-memory and in-memory levels. We find that both the off-memory floating-point (FP) exponent alignment and the in-memory random cell bit-flip errors impair digital CIM's computing reliability, causing significant truncation and bit-flip accuracy loss. Critically, existing reliability solutions are incompatible with the unique multi-row accumulation structure of digital CIM, which either severely damage digital CIM's performance or result in prohibitive overhead.

To address above challenges, we propose HR-DCIM: a high-reliability FP digital CIM architecture featuring unified low-cost iterative error correction. Specifically, for the off-memory reliability, we propose an exponent-mantissa joint-alignment mechanism to repurpose inherent invalid bits of aligned mantissas as

compensation bits to reduce alignment truncation loss, without damaging digital CIM's performance. Then, for the in-memory reliability, we propose a remainder aliasing-based unified multiply-accumulation (MAC) error correction mechanism to correct possible MAC errors caused by various cell error cases with low-cost iteration. Experimental results show that the proposed techniques enable digital CIM to maintain high performance and efficiency across various operating voltage conditions without significant accuracy loss.

P42 海报题目：A 40nm 4Mb High-Reliability STT-MRAM Achieving 18ns Write-Time and 94.9% Wafer-Level-Die-Yield across -55°C-to-125°C

报告人：侯耀儒，香港科技大学
指导老师：邵启明

摘要： This work presents a 40nm 4Mb mass-production-ready, wide-temperature (-55°C to 125°C) STT-MRAM fabricated on a 300mm Si wafer, achieving 18ns write time, 1e8 endurance and 94.9% wafer-level yield. Key innovations include on-chip LDO-based power supply for wide-temperature requirements, asymmetrical write path to mitigate low-temperature breakdown risk, 2T-2M bit-cell structure for reliable high-temperature read operations, and byte-wise ECC to enhance yield and adapt with various MCU interface.

P43 海报题目：A Globally Optimized 3-D MPPT System for Dual-Band RF Energy Harvesting with Collaborative Source Reconfiguration

报告人：李霞光，复旦大学
指导老师：曾晓洋/陈之原

摘要： This paper presents a globally optimized RF energy harvesting system leveraging the novel concepts of 3-D maximum power point tracking (MPPT) and collaborative source reconfiguration, achieving high MPPT accuracy and wide input power range. The 3-D MPPT is realized by coordinating energy source, optimizing the rectifier output and regulating the rectifier stages. By integrating a multi-level regulating DC-DC converter with a reconfigurable rectifier, the system enables synchronized and collaborative energy harvesting from dual-band RF sources. The fabricated chip demonstrates a peak end-to-end efficiency of 71%, a sensitivity of -24.1 dBm, and the wide high-PCE input power ranges of 15.5 dB and 20.5 dB at 433 MHz and 900 MHz, respectively.

P44 海报题目：A 2.15W 120V/230Vac to 5-to-12Vdc Offline Power Converter with Full-Duty-Cycle Input-Series Dual-Branch Converter Achieving 1088mW/cm3 and 87.2% Peak Efficiency

报告人：刘刚，香港中文大学（深圳）
指导老师：刘寻

摘要： This paper presents a 120V/230Vac to 5-to-12Vdc offline power converter consisting of a capacitor-drop AC-DC rectifier and a full-duty-cycle input-series dual-branch DC-DC converter for IoT devices. The proposed converter operates at full-duty-cycle with VCR of D/2 and reduces both the CREC volume and the voltage stress on components, while achieving high efficiency across a broad input and output voltage range. 87.2% peak efficiency, 2.15W output power, and 1088mW/cm3 power density are

achieved.

P45 海报题目：A Galvanic Isolator Achieving 117-Mb/s Forward Data Transfer in the Presence of 181-kV/μs Common-Mode Transient Interference

报告人：陆杰，南京大学
指导老师：邱浩

摘要： Targeting a high data rate (DR) in the presence of common-mode transient (CMT) interference in the isolated gate driver application scenario, we presented an inductively galvanic isolator (GI) consisting of transmitter (TX) and receiver (RX) dies. To eliminate the destructive effects of CMT interference, an adaptive transconductance enhancement (ATE) technique was proposed on the TX side, which enables real-time detection of CMT events and contributes to an enhanced gm to stabilize the oscillator's operation. For the data transfer, we observed the problem of unequal data symbol durations using the conventional frequency-shift keying (FSK) demodulator, which can lead to shoot-through current or large reverse conduction loss. This problem was solved by the proposed compensated FSK demodulator. Both TX and RX dies in the proposed GI were fabricated in a 0.18 μm BCD process. Experimental results verified that the proposed GI demonstrates static CMT immunity (CMTI) up to 299 kV/μs. Furthermore, even in the presence of a severe CMT interference of 181 kV/μs, the GI supports a high DR of 117 Mb/s, corresponding to a data rate ratio (DRC) of 67 %, with a low bit error rate (BER) of 10-8. This extends the state-of-art by 3.72× in DRC and 1.24× in dynamic CMTI.

P46 海报题目：Fully Analog In-Memory Annealing Ising Machine with Unified Deterministic and Probabilistic Computing Array Using CMOS-integrated VCMA-MTJ

报告人：陆韵阳，香港科技大学
指导老师：邵启明

摘要： This work presents a fully analog in-memory annealing Ising machine based on CMOS-integrated voltage-controlled magnetic anisotropy magnetic tunnel junction (VCMA-MTJ), developed through a device-circuit-system co-design approach to address bottlenecks in traditional digital CMOS and mixed-signal CMOS+X Ising machines. By unifying classical bit (C-bit) and probabilistic bit (P-bit) functionalities into the VCMA-MTJ device, the proposed chip, fabricated using 28-nm CMOS+VCMA-MTJ technology, enables simultaneous deterministic Hamiltonian calculations and probabilistic spin updates, thus achieving a fully analog in-memory Ising machine. System-level demonstrations validate the prototype's performance, incorporating calibration techniques to TMR variations in the C-bit array and switching variations in the P-bit array. Without relying on additional ADCs, DACs, or RNG circuits, this work demonstrates a spin density enhancement of 8.9× to 73.7×, while achieving an annealing power per spin of just 28 μW (power reduction of 2.46× to 147×) compared to prior CMOS and CMOS+X-based all-to-all Ising machines.

P47 海报题目：PAPRICA: A Pre-Synthesis Area Predictor for Baseband Circuit Auto-Generators

报告人：毛昀尉，东南大学
指导老师：张川

摘要： Auto-generation and auto-optimization for baseband circuits have significantly enhanced design

productivity. Nevertheless, existing auto-optimizers primarily focus on optimizing RTL code for algorithm performance, neglecting critical hardware constraints. To overcome this limitation, this paper proposes Paprica, a pre-synthesis area predictor for baseband circuit auto-generators. Paprica bridges the gap between hardware parameters and area, providing auto-optimizers with accurate area predictions in milliseconds. To validate Paprica, we estimate the area of three baseband circuits (polar encoder, MIMO detector, and polar decoder). Experimental results demonstrate remarkable accuracy and efficiency in area prediction, achieving a mean absolute percentage error (MAPE) of 0.21%, 1.49%, and 1.20% with average end-to-end runtimes of 0.9 ms, 8.0 ms, and 6.6 ms, respectively. Paprica outperforms the state-of-the-art approach in area prediction, reducing MAPE by 98.0%, 91.8%, 78.4%, respectively, and decreasing average end-to-end runtime by over 99% across the three circuits.

P48 海报题目：A 12nm 4Mb 104.56-to-137.75TFLOPS/W Charge-Trap Transistor-Based Computing-in-Memory Macro Using Analog-Predict-Digital-Compute for AI Edge Devices

报告人：沈浚哲，中国科学院微电子研究所

指导老师：窦春萌

摘 要： Previous non-volatile CIM (nvCIM) macros suffer from low storage density, unnecessary multiply-and-accumulate (MAC) operations, and large hardware cost for floating point computations. A 4Mb CTT nvCIM macro, fabricated in 12nm CMOS, supports INT/FP4 MAC operations with the analog-predict-digital-compute scheme for power saving, achieving an energy-efficiency of 137.75TFLOPS/W and > 40 times improved density FoM (storage density×computing density).

P49 海报题目：A 6V-to-1V ReSC-Hybrid Two-Stage Merged Buck Converter with an Ultra-Small Inductor for VPD

报告人：宋志邦，清华大学/澳门大学

指导老师：路延

摘要： This work presents a compact 6-to-1 V resonant switched-capacitor (ReSC) hybrid two-stage merged buck converter targeting point-of-load vertical power delivery (VPD) in XPU systems. The proposed topology merges a low-frequency ReSC stage and a low-voltage high-frequency inductor-first buck stage, enabling efficient regulation with simple duty-cycle control and greatly reduced volume of the passive components. The two stages (chips) are fabricated in a 180-nm BCD and a 65-nm CMOS process, respectively. Compared with conventional ReSC, The ReSC-Hybrid converter maintains high efficiency across most of the regulation range. With a compact 33nH inductor, it achieves 92.4% peak efficiency at 0.2 VCR and delivers 1.3 W/mm^3 power density and 2.35 A/mm^2 vertical current density.

P50 海报题目：GenPolar: Generative AI-Aided Complexity Reduction for Polar SCL Decoding

报告人：孙玉泰，东南大学

指导老师：张川

摘要： The CRC-aided successive cancellation list (CA-SCL) decoding algorithm for polar codes has gained widespread adoption thanks to its outstanding performance. However, with the evolution of 6G technologies, the high complexity of CA-SCL decoding poses a challenge in meeting growing performance requirements. Consequently, it is crucial to devise strategies that reduce this complexity

without compromising error rates. Current efforts to mitigate the complexity mainly depend on harnessing special nodes associated with the code construction sequences, such as Fast-SCL decoding. However, these strategies suffer from redundant complexity due to ill-suited construction sequences and unnecessary sorting operations within special nodes. Addressing this issue, this paper proposes a hardware-friendly and GenAI-aided complexity reduction approach for Fast-SCL decoding, named GenPolar. This approach involves two-step optimization techniques: 1) Transformer encoder models for generating polar construction sequences, and 2) a sorting entropy based method for sorting reduction. These two-step techniques result in reduced complexity with negligible performance loss. For polar codes of length-1024 with code rates of 0.25, 0.50, and 0.75, GenPolar achieves latency reductions of 20.6%, 29.8%, and 40.6%, respectively. Even benchmarking against the reduced-complexity version of Fast-SCL decoding, the relative gains are 14.0%, 17.8%, and 22.3%, respectively. It should be noted that the immediate application is not limited to Fast-SCL decoding but also extends to other node-based SCL decoding algorithms like SSCL-SPC and SR-SCL.

P51 海报题目：A 16Mb 166.8TOPS/W Near-Memory Phase-Domain-Computing Ferroelectric NAND Flash for Approximate Nearest Neighbor Search on Edge Devices

报告人：王柏翰，中国科学院微电子研究所
指导老师：窦春萌

摘要： Previous near-memory computing (NMC) or in-memory-computing (IMC) NANDs suffers from limited IO width, large energy-delay-product, and can not support diverse vector types. This work presents the fabricated 16Mb near-memory phase-domain-computing (NM-PDC) FeNAND chip can compute the 512 similarity distances between 256-dimensional, 4-bit vectors in a single search operation, with an energy efficiency of 166.8 TOPS/W and 12.8 times reduced overall search latency.

P52 海报题目：A 28nm 127.54TFLOPS/W MXFP6 and 117.42TFLOPS/W MXFP8 Compute-in-Memory Macro with Adaptive-Preserved-Bit-Width and Serial-Dual-Bit-Sliding Schemes

报告人：王幸，东南大学
指导老师：司鑫

摘要： Conventional FP-CIMs suffer from fixed preserved bit-width (PBW), limiting their adaptability and efficiency. This work proposes the first MXFP-CIM macro enabling wide-range adaptive PBW, featuring: (1) A serial dual-bit-sliding scheme; (2) A harmless data mapping scheme with a hierarchical hidden-bit decoder; (3) An adjustable-PBW MXFP-MAC circuit via twin-stage allocation. The 28nm MXFP-CIM macro achieves a peak energy efficiency of 127.54TFLOPS/W in the MXFP6/6 mode.

P53 海报题目：ACEMARL: Adaptive Clustering Enhanced Multi-Agent Reinforcement Learning for Analog Circuit Sizing

报告人：吴翰，南方科技大学
指导老师：路延/姜俊敏

摘要： Analog circuit sizing remains a critical bottleneck in integrated circuit design, requiring extensive manual effort and computational resources. While multi-agent reinforcement learning (MARL) accelerates

optimization through parallel agent training, existing approaches rely on manual circuit block clustering that fails to capture functional relationships between parameters. This paper presents ACEMARL, an adaptive clustering framework that automatically discovers functionally similar parameter clusters. ACEMARL integrates Bi-population Covariance Matrix Adaptation Evolution Strategy (BIPOP-CMA-ES), a high-performance evolutionary algorithm, for multi-modal exploration with data-driven clustering, aiming for automatic agent assignment. Experimental validation on amplifier and low-dropout regulators with up to 179 parameters demonstrated 3.3-5.0$\times$ faster convergence and 5.7-38.5\% Figure-of-Merit (FoM) improvement compared to state-of-the-art (SOTA) block-based methods. The framework reduced confidence interval width by 31.6-60.7\% along mean reward trajectories, enabling fully automated analog circuit sizing with improved stability and performance.

P54 海报题目：A 28-nm Mode-Reconfigurable CAM-CIM Hybrid Complete 3-SAT Solver Supporting Conflict-Driven Clause Learning with 100% Solvability

报告人：吴子涵，北京大学
指导老师：王源

摘要：The K-SAT problem is NP-complete and costly on von Neumann machines. Several ASIC solvers have been proposed to mitigate this, but they rely on inefficient crossbar mapping, overlook community structures and lack adaptability to formula size. This work presents an ASIC complete solver with conflict-driven clause learning (CDCL), employing a mode-reconfigurable CAM–CIM hybrid architecture. Fabricated in 28nm CMOS, it achieves 4.3-to-5.1 times speedup and 1.4 times energy reduction over a state-of-the-art ASIC complete solver.

P55 海报题目：A Flexible Digital Compute-in-memory Chip for Edge Intelligence

报告人：闫岸之，清华大学
指导老师：任天令

摘要：Flexible electronics, coupled with artificial intelligence, hold the potential to revolutionize robotics, wearable and healthcare devices, human–machine interfaces, and other emerging applications,. However, the development of flexible computing hardware that can efficiently execute neural-network-inference tasks using parallel computing remains a substantial challenge. Here we present FLEXI, a thin, lightweight and robust flexible digital artificial intelligence integrated circuit to address this challenge. Our approach uses process-circuit-algorithm co-optimization and a digital dynamically reconfigurable compute-in-memory architecture. Key features include clock frequency operation of up to 12.5 MHz and power consumption as low as 2.52 mW, all while achieving subdollar-per-unit cost and an operational circuit yield of between approximately 70% and 92%. Our circuits can perform 1010 fixed and random multiplications without error, withstand over 40,000 bending cycles and maintain stable performance for a period exceeding 6 months. A one-shot on-chip neural network deployment eliminates the power consumption and latency associated with sequential weight writing, achieving up to 99.2% accuracy in temporal arrhythmia detection tasks on a single 1-kb chip. In addition, FLEXI demonstrates over 97.4% accuracy in human daily activity monitoring using multimodal physiological signals.

P56 海报题目：A 10MHz All-1.2V-NMOS Battery-Input Single-Mode Hybrid Buck-Boost Converter

in 65nm CMOS with Fast Transient Response

报告人：杨文杰，清华大学

指导老师：路延

摘要：Buck-boost DC-DC converters are widely used in Li-ion battery-powered portable devices. For the conventional buck-boost converter, high voltage stress of switches, right-half-plane (RHP) zero and large inductor current ripple are major three drawbacks. This paper presents an inductor-first ladder-based hybrid single-mode buck-boost converter implemented in 65nm CMOS. All switches and capacitors only experience a voltage stress of 1/3 output voltage (VOUT). The converter works in single mode operation and exhibits small inductor current ripples. This work achieves the highest chip density of 1.62A/mm2 and off-chip power density of 6.55W/mm3.

P57 海报题目：Fully Digital Hybrid Compute-in-ROM/SRAM Architecture for On-Chip Deployment of Large-Scale Deep Neural Networks

报告人：于天熠，清华大学

指导老师：李学清

摘要：Compute-in-memory (CiM) is a promising approach to alleviating the von Neumann memory wall bottleneck in data-intensive tasks. As a candidate to build CiM, static-random-access memory (SRAM) has become popular in accelerating deep neural networks (DNNs) because of its mature fabrication support and high flexibility. However, SRAM-based CiM suffers from low memory density, resulting in frequent weight reloading and increased power consumption during end-to-end inference tasks. Recently, read-only-memory (ROM)-based analog CiM (ACiM) has demonstrated the potential to deploy all DNN weights on-chip by leveraging high-density ROM. It may also achieve encouraging flexibility by exploiting the synergy between a small SRAM and a big ROM. Nevertheless, it faces challenges in achieving high computing density due to limitations in analog-to-digital converter (ADC) performance.

Meanwhile, digital CiM (DCiM) improves computing density but incurs significant energy and area overhead due to the adder tree. To address these challenges, we proposes the first fully digital and flexible compute-in-read-only-memory (DCiROM) design approach. On the one hand, DCiROM introduces a novel ROM-logic fusion CiM that reduces the CiM area by 51% while maintaining high memory density and computing performance. On the other hand, DCiROM achieves high flexibility with minimal area overhead by proposing two innovative multiply-and-accumulate (MAC) resource-reusing techniques. This work has implemented a DCiROM chip with 3024Kb ResNet-56 parameters using a 65nm CMOS technology. This macro achieves 6.9-29.5x higher normalized FoM (memory density x computing density) than the state-of-the-art CiM works. Additionally, it reduces energy consumption per image inference by 2.9-9.9x compared to SRAM-based CiM works when off-chip access is considered.

Additionally, this paper presents a fully digital compute-in-ROM/SRAM macro for edge AI acceleration, fabricated in a 28nm CMOS technology. The proposed architecture integrates 18Mb of compressed ROM with 8Kb of trainable SRAM, achieving a record-high memory density of 26.9 Mb/mm^2. This work introduces a novel sparsity-aware ROM mapping mechanism, reducing area by 91% and 88% for sparse and dense weights compared to SRAM implementation. The proposed ROM macro employs a

value-aware balanced adder tree that enhances computing throughput by 28% via critical path optimization. Furthermore, this chip utilizes a scalable ROM/SRAM hybrid architecture that maintains <0.5% accuracy loss in transfer learning scenarios, while supporting model expansion through time-division multiplexing (TDM). Measurement results demonstrate a 7.9-40.3x improvement in density FoM over prior CiM designs, achieving 1159.4 TOPS/W x Mb/mm^2 in SWaP (Space-Wattage-and-Performance-Density) metric. For complete inference tasks, the proposed design exhibits 43.8x higher energy efficiency than volatile SRAM/eDRAM CiM works.

P58 海报题目：A Compact Dual-Capacitor Relay SPT Supply Modulator with Overshoot-Free Adaptive On-Time Control for 5G FR2 CMOS PA

报告人：喻哲文，清华大学/澳门大学

指导老师：路延

摘要：5G new-radio frequency-range-2 CMOS PAs with high peak-to-average-power ratios suffer from low efficiency, calling for compact and fast symbol-power-tracking (SPT) supply modulators (SMs). Inductor-based SPT shows limited tracking speed, while multilevel switched-capacitor approaches need redundant capacitors and switches. The proposed prototype dual-capacitor relay SPT SM with overshoot-free adaptive constant on-time control achieves <290ns tracking using a 0402 inductor, suitable for compact PA arrays.

P59 海报题目：A CRYO-CMOS RF-DAC Based Super-Heterodyne Transmitter for Superconducting Qubit Control

报告人：袁凤恩，澳门大学

指导老师：彭亚涛

摘要：Multiple Qubits should be manipulated to perform practical quantum computing, which requires a broad frequency range for the qubit control chip. We present a 4 K cryo-CMOS quantum control chip featuring a Mixing (MIX)/ Non-return-to-zero (NRZ) mode radio frequency digital to analog converter (RF-DAC) and an up-conversion mixer. By opting for Mixing Mode RF-DAC and a mixer for two-stage frequency up-conversion instead of direct-conversion or other methods, our controller can achieve a wider modulated frequency range and lower power consumption.

P60 海报题目：An Inductor-at-Middle Hybrid Buck Converter with Shared Power-Signal Path for Distributed Vertical Power Delivery

报告人：朱仲耀，清华大学/澳门大学

指导老师：路延

摘要：This work presents an inductor-at-middle hybrid buck converter for high-current density vertical power delivery, reusing the power inductors as signal feedback paths. The proposed switching bus multiplexing control reuses the power path to carry a feedback signal, mitigating the challenges in sophisticated signal and power network co-design for pin-intensive distributed power delivery network. The prototype achieves a vertical current density of 3.17A/mm2.

P61 海报题目：A 6.78-MHz Wireless Power and Data Transfer System Achieving Simultaneous 48.6% End-to-End Efficiency and 4.0-Mb/s Forward Data Delivery With Interference-Free

Rectifier

报告人：庄泉荣，南京大学
指导老师：邱浩

摘要：Targeting implantable medical devices (IMDs), we presented a simultaneous wireless power and data transfer(WPDT) system, using the fundamental and harmonic components of the bridge inverter on the transmitter (TX) side to, respectively, deliver power and forward data. On the receiver (RX) side, we discovered the data-flipping problem using the conventional full-bridge rectifier (FBR), which is ascribed to the interference from its distorted input voltage (VAC). This problem is solved by the proposed interference-free rectifier (IFR) featuring its low-distortion staircase Vac. To further alleviate the crosstalk between power and data transfer, a tapped coil three-capacitor (TL3C) topology on the TX side together with a resonant topology on the RX side was proposed. The IFR IC was fabricated by a 0.18-μm CMOS process, with which a 6.78-MHz WPDT system was implemented. Experimental results showed that compared with the conventional FBR, the interference voltage ratio (IVR) in the proposed IFR was reduced from −17 to −45.2 dB. At a distance of 6 mm, our system supported simultaneous 54.4-mW load power (PLoad) and 4.0-Mb/s forward data rate (DR) with 48.6% end-to-end efficiency (ηE2E). Both figure of merits (FoMs) for power and data transfer are the highest compared with previous results.

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P62 海报题目：An LTPS-TFT-Based Large-Area PPG Readout Circuits With Improved Linearity and Robustness for Flexible Healthcare Ring

报告人：伯扬，上海交通大学
指导老师：赵健

摘要： Thin-film transistor (TFT) can be fabricated on flexible substrates, offering potential for seamless, long-term wearable health monitoring. However, the limited performance, process variation, and motion artifacts hinder the widespread adoption of flexible wearable devices. This article presents a TFT-based photoplethysmography (PPG) acquisition circuit for flexible healthcare rings, integrating a voltage-controlled oscillator (VCO) based analog front-end (AFE) to overcome the performance limitations caused by the low mobility of TFT devices. Meanwhile, a dead-zone free (DZ-Free) phase-frequency detector (PFD) was proposed and integrated into the VCO transimpedance amplifier (TIA) to enhance the linearity. Additionally, a 0-1 MASH VCO-analog-to-digital conversion (ADC) structure was adopted to improve the quantization dynamic range (DR). The system is implemented using 3- μ m low-temperature poly-silicon (LTPS) TFT (LTPS-TFT) process of TIANMA Microelectronics. The measurement results show that DZ-Free PFD improves the linearity and the proposed VCO-TIA achieves a 61.5-dB DR. The proposed ADC demonstrates a 72-dB spurious-free dynamic range (SFDR), a 65.8-dB SNDR and an 80-dB DR. Under temperature sweeping from −40℃ to 80℃ and supply voltage variations of 10 ± 2 V, the ADC maintains performance variations within 3%, while the TIA stably sustains a gain of 110 dB Ω . Finally, PPG and blood oxygen saturation (SpO2) measurements were demonstrated, including ambient light compensation. This work provides a feasibility demonstration for TFT-based fully integrated flexible electronics in bio-signal monitoring applications.

P63 海报题目：An Energy Efficient Amplifier with a Closed-Loop Gm-Boosting Stage and Current Mirror Based SR Enhancement for Driving Large Capacitive Loads

报告人：曹思遥，浙江大学
指导老师：宋爽

摘要： This paper proposes a low-power two-stage amplifier for large capacitive load driving. A closed-loop gm-boosting (CLGB) stage with complementary driving devices is exploited to reduce the output resistance and thus makes the output pole non-dominant with minimum power overhead. Therefore, the amplifier has the dominant pole internally with a small capacitor, achieving a high gain-bandwidth (GBW). Meanwhile, a current-mirror based slew rate (SR) enhancement circuit is implemented to increase the current driving capability. This circuit leverages the gain of a cross-coupled pair to generate an SR enhancing current with a fixed ratio to its bias, featuring high PVT robustness compared with voltage-based enhancement. The proposed amplifier is implemented in a standard 55nm CMOS technology, with an active area of 0.009mm2. It achieves a GBW of 1.6MHz with a 12nF CL, achieving an IFoMS of 984,615 that advances the state-of-the-art by 1.4X. It provides an SR of 0.19 V/μs with a 12nF load, with an IFoML of 116,923, exceeding the state-of-the-art by 2X. The excellent GBW and SR with a quiescent current of only 19.5μA make this amplifier suitable for large capacitance driving applications.

P64 海报题目：A 28nm 8-Bit 32-GS/s DAC Achieving > 55dBc/> 40dBc SFDR up to

5.2GHz/13.6GHz Using 4-Channel NRZ Time-Interleaving with Background Calibration for Direct Digital Signal Synthesis

报告人：陈思皓，清华大学

指导老师：杨华中

摘要：This work presents an 8-bit 32-GS/s 4-channel non-return-to-zero (NRZ) time-interleaving (TI) digital-to-analog converter (DAC) fabricated in a 28 nm CMOS process. This DAC is the first to achieve a sampling rate of over 16 GS/s using an NRZ TI structure. The proposed DAC employs background calibration to ensure the clock timing alignment of the four channels, which significantly improves the DAC dynamic performance. The measurement results demonstrate a 55 dBc spurious-free dynamic range (SFDR) at 5.2 GHz and a 40 dBc SFDR at 13.6 GHz. The total power consumption is 692 mW when the DAC operates at 32-GS/s sampling rate (FS) under a mixed 1.8V/1.2V/1.0V supply. The proposed DAC provides superior bandwidth and precision for direct digital signal synthesis (DDS), especially at high frequencies.

P65 海报题目：An Energy-Efficient Pipelined-SAR ADC With Cascode Capacitively Degenerated Dynamic Amplifier and MSB Pre-Conversion Technique

报告人：陈卓毅，北京大学

指导老师：沈林晓

摘要：This article presents an energy-efficient fully dynamic pipelined successive approximation register (SAR) analog-to-digital converter (ADC), which utilizes a cascode capacitively degenerated dynamic amplifier (CD-DA) as the residue amplifier. The proposed amplifier achieves inherent linearity together with a boosted gain, while an output swing enhancement technique further extends its swing range. To guarantee stable linearity across wide temperature variations, a PTAT bias current is employed. In addition, the most significant bit (MSB) pre-conversion technique is introduced, which elegantly integrates the output swing enhancement method with the second-stage SAR ADC, enabling simultaneous swing extension and faster residue conversion without additional hardware. The prototype ADC is fabricated in a 22-nm CMOS process and achieves 73.9-dB signal-to-noise-and-distortion ratio (SNDR) and 89.4-dB spurious free dynamic range (SFDR) at Nyquist input while consuming only 0.36 mW. This corresponds to a Walden figure of merit (FoM) of 1.78 fJ/conversion-step and Schreier FoM of 182.3 dB. The measurement shows that the SNDR variation is below 2 dB at −40~80 ◦C and over ±10% supply variation.

P66 海报题目：A CMOS Hybrid Common-Gate Current-Integrating Sampler with >37dB SNDR Across 51GHz BW in a 128GS/s Front-End

报告人：戴军，清华大学

指导老师：孙楠

摘要：This work proposes a CMOS hybrid common-gate current integrating sampler to address linearity, BW, and jitter limitations in prior wideband ADC front-ends. The front-end employs a hybrid common-gate V-I converter, transformer-coupled inductive peaking, and an automatic power-gating hold buffer, enabling 48.1dB SFDR and 38.6dB SNDR near its 52GHz BW. This work demonstrates superior SNDR (measured near BW), outperforming prior samplers/ADCs reported in ISSCC/JSSC/VLSI with BW>30GHz.

P67 海报题目：An Energy-Efficient, High-Resolution kT/C-Noise- Canceled Pipelined-SAR Capacitance-to-Digital Converter With Incomplete-Settling-Based Correlated Level Shifting in 22-nm CMOS

报告人：高继航，北京大学

指导老师：沈林晓

摘要：This article presents a high-resolution and energy-efficient pipelined-successive-approximation -register (SAR) capacitance-to-digital converter (CDC). The converter uses a two-stage SAR analog-t o-digital converter (ADC) and a Residue amplifier (RA) to effectively convert the input signal. To mitigate the impact of kT/C noise during the sampling process, an enhanced kT/C noise cancellati on technique is used within a pipelined-SAR architecture. In addition, an innovative incomplete-set tling-based correlated-level-shifting (ISCLS) technique is proposed to achieve an equivalent open-lo op gain of over 80 dB, thereby enhancing power efficiency and amplification accuracy. Furthermor e, a background calibration loop is proposed to track PVT changes and ensure high-precision am plification under PVT variations to ensure PVT stability. The proposed CDC is implemented in a 22 -nm CMOS process. The prototype achieves a resolution of 37.12 aF under 384-fF input capacitan ce with 4.71 μW, resulting in a Walden figure-of-merit (FoMw) of 7.9 fJ/conv.-step, which represen ts more than a twofold improvement compared with previous sub-fF resolution CDCs.

P68 海报题目：A 0.93ps-ToF-Resolution 14.6mW NIRS IC with Signal-Aware Optical Frontend and Rotational Modulation Data Converter for Psychiatric Disorders Diagnostics

报告人：郭志鹏，上海交通大学

指导老师：赵健

摘要：This work proposed a near-infrared spectroscopy (NIRS) IC achieves a 0.93 ps time-of-flight (ToF) resolution within a 10 Hz bandwidth while consuming 14.6 mW power. The chip is configurable to operate across frequencies ranging from 10.24 to 40.96 MHz, enabling compact optical system designs and adaptability to diverse diagnostic methods for psychiatric disorders. The maximum measurement error of the absorption coefficient and the reduced scatter coefficient are less than 3%, surpassing the state-of-the-art. Comprehensive in-vitro and in-vivo demonstrations showcase its capability for both verbal task and niacin flush based mental health diagnosis.

P69 海报题目：A 13b 500MS/s 94dB-SFDR Resistive-Input Pipelined-SAR ADC_x000b_with Linear and Efficient Current-Buffer-Based Integrating Sampler

报告人：何西榆，清华大学

指导老师：孙楠/揭路

摘要：This work proposes a pipelined-SAR ADC featuring a current-buffer-based integrating sampler that presents a resistive input with good linearity. A floating charge transferrer (FCT) with multi-bit pre-conversion (MB-PC) enables linear residue amplification and accelerates the second-stage conversion. The prototype ADC achieves an SNDR of 67.5 dB and an SFDR of 94.5 dB under a Nyquist input at 250 MHz. This SFDR is the highest reported for discrete-time ADCs operating above 200 MS/s.

P70 海报题目：A 2.16 μW Chopper Amplifier with a Feedforward SAR ADC Assisted Mixed-Signal DC-Servo Loop Achieving ±1V DC Offset Cancellation in 2.1s and 1Vpp CM Interference Tolerance for Neural Signal Acquisition

报告人：黄博，西安交通大学
指导老师：张鸿

摘要： Emerging brain-computer-interface technologies necessitate precise acquisition of weak neural signals under strong interferences (Fig. 1) [1–5]. Apart from common-mode interferences (CMI) at 50/60 Hz, the electrode DC offset (EDO) can be up to 1 V and varies remarkably when connection status changes, especially in wearable sceneries. In applications where a frontend amplifier is shared by multi-channel electrodes, large EDO steps may occur at the amplifier's input when the channel switches [2]. Therefore, cancellation of large EDO within a short recovery time is very important for these cases. In these areas, capacitively-coupled instrumentation amplifiers (CCIA) are popular because of their low power and fully integration advantages, in which chopper-stabilization (CS) is often incorporated to suppress the CCIA's large 1/f noise [3]. However, with chopping, the EDO could propagate through the input capacitor and saturates the CCIA. In addition, the decreased input impedance (Zin) due to chopping not only attenuates the neural signal but also deteriorates the CMI's effect caused by electrode mismatch. Many structures have emerged to solve above problems, such as DC-servo loops (DSL) [3] for EDO cancellation, CMI cancellation (CMC) loops [3], positive feedback loops (PFL) for Zin boosting [4]. Among them, the existing DSL techniques still face tough tradeoffs between the maximum EDO can be cancelled (VEdo,max), recovery time, power consumption, and noise injection. This paper presents a CS-CCIA with a feedforward SAR ADC assisted mixed-signal DSL (MS-DSL) in 180nm CMOS, which achieves the best overall performance in terms of Vedo,max, recovery time, power consumption and noise among recent related works. In addition, a feedback CMC (FB-CMC) loop and a hybrid PFL are also proposed, achieving 1－VppCMI tolerance and 2GΩDC Zin, respectivel...

P71 海报题目：A 2.84-mW 8-MHz Bandwidth 76.7-dB SNDR N-Path-Filter-Based Pure Bandpass DSM

报告人：李润坤，香港中文大学
指导老师：潘江鹏

摘要： This article presents a power-efficient high-performance bandpass Delta-Sigma modulator (BPDSM) based on passive N-path filters (NPF) for direct digitization of intermediate-frequency (IF) signals in wireless receivers. NPF-based BPDSMs have recently been introduced, offering excellent power efficiency and flexible IF frequencies. However, the reported ones recorded a relatively narrow bandwidth, had a redundant passband around DC, and were demonstrated only with a single-bit quantizer. In this work, we report the first NPF-based BPDSM that removes the redundant DC passband using a special NPF for extended bandwidth and improved power and area efficiency. For this reason, it is called a pure BPDSM. Furthermore, we demonstrate that the NPF-based BPDSM works well with a multi-bit quantization approach for improved performance. A fourth-order BPDSM prototype was designed and fabricated in a 65-nm CMOS process, occupying an active area of 0.086 mm2. It features an IF tuning range from 100 to 500 MHz with a signal-to-noise-plus-distortion ratio (SNDR) greater than 60 dB over a fixed 8-MHz bandwidth. Clocked at 700 MHz (IF = 175 MHz), the BPDSM achieves a peak SNDR of 76.7 dB over the 8-MHz bandwidth while dissipating 2.84 mW from a 1.2-V supply, leading to a Schreier's figure-of-merit of 171.2 dB, the highest among reported BPDSMs of any type.

P72 海报题目：High-Performance Flexible Carbon Nanotube CMOS Integrated Circuits for

Sensor Front-End

报告人：李汪昌，北京大学

指导老师：胡又凡

摘 要： Flexible sensor front-end ICs that process signals in-situ are vital for next-generation human-interfacing flexible electronics. Carbon nanotubes (CNTs) offer a promising opportunity to construct high-performance CMOS transistors and ICs in a mechanically flexible form, thanks to the CNTs'excellent electrical and mechanical properties. We report wafer-scale, high-performance flexible CNT CMOS transistor technology and its applications in both analog and digital ICs. For analog circuits, CNT CMOS transistors distinguish themselves from Si counterparts by showing inherent negative differential resistance (NDR) effects in subthreshold region, which produce intrinsic gain singularities (gmro $\rightarrow\infty$) that can be utilized in circuits for ultrahigh and exponentially variable gain. A flexible CNT CMOS op-amp with a tunable single-stage gain of 35-60 dB is demonstrated. For digital circuits, flexible CNT transistor shows advantages in speed due to the high mobility (comparable with rigid Si CMOS), superior to other flexible transistor technologies. We report a five-stage ring-oscillator showing oscillation frequency of 356 MHz, corresponding to stage delays of 281 ps, under a supply voltage of 2.6 V, representing the first flexible high-speed ICs with sub-nanosecond stage delays. We also build a flexible flash memory array based on CNTs. Leveraging the platforms of flexible CNT transistors, flexible sensor front-end electronics can be built, as we demonstrated in proof-of-concept flexible electrocardiogram/electromyogram patches.

P73 海报题目：A 103.9dB-SFDR 83.8dB-SNDR 3MHz-BW Multi-Bit Quadratic-Exponential Noise-Coupled IDSM with High Tolerance to DAC Non-Linearity

报告人：李振升，澳门大学

指导老师：冼世荣

摘要： This paper presents a quadratic-exponential noise-coupled (NC) IDSM to achieve a quantization noise shaping effect greater than 4th order with OSR 22, while having high tolerance to DAC non-linearity and a small noise penalty factor. The DAC2 and adder in NC are reused for a larger effective OSR and improve energy efficiency. Implemented in 28nm CMOS, the IDSM achieves an SNDR/SFDR of 83.8dB/103.9dB, with a 3MHz bandwidth, and 794μW, resulting in Schreier FoMSNDR/FoMDR of 179.6dB/181.4dB.

P74 海报题目：A 0.0022 mm2, 2 GS/s Resettable VCO-Based ADC With-out Quantization Noise Shaping

报告人：鲁涛，中国科学技术大学

指导老师：胡诣哲

摘要： With the rapid advancement of sensing and communications, there is an increasing demand for medium-resolution (6–8 b), high-speed (> 1 GS/s) ADCs. Flash and time-interleaved ADCs typically obtain high sampling rates, albeit at the cost of large power [1], [2], [3]. Taking advantage of the significant advances in digital performance in CMOS, time-domain based converters enable ever faster conversion speeds [4], [5], [6], [7]. Highly digital low-power VCO-based ADCs have particularly benefited from this trend. Although VCO-based ADCs features inherently first-order noise shaping of quantization noise, they are widely used in low-speed, high-precision applications thanks to oversampling [14], [8], [9], [10], [11],

[12], [13]. However, with the continual increase in VCO frequency in newer process nodes, Nyquist VCO-based ADCs can achieve progressively better accuracy at high sample rates, thus making them attractive for high-speed applications [16], [17]. Additionally, since a Nyquist VCO-based ADC can achieve an extra bit of resolution by halving the sample rate [15], this feature enables easy adaption to various communication standards and frequency bands, thus enhancing versatility. In this paper, we propose a Nyquist VCO-based ADC with a single channel of 2 GS/s. The key innovations include: 1) a resettable ring VCO (R-RVCO), 2) switched buffers (sw-buf), and 3) a compact fine-quantizer with phase folding, all aimed at substantially improve SNDR and FOM.

P75 海报题目：Energy-Efficient Sensor Readout Frontend for Emerging Edge Applications

报告人：罗昊洋，北京大学
指导老师：唐希源

摘要：Emerging edge applications demand low-noise, low-power, wide-dynamic-range sensor readout frontends. This work proposes a tracking-zoom readout design with a fast tracking technique that tracks input signals continuously based on fine quantizer outputs. It also comprises a floating-Gm-CCO loop filter to support current reuse with a low CCO operating voltage. The design achieves 90.2dB SNDR over 10kHz-BW with 4.91μVrms input-referred noise and 4.82μW power consumption, leading to a SNDR Schreier FoM of 183.4dB.

P76 海报题目：A 0.5-ppm/°C Voltage Reference With Sub-Ranging On-Chip Self-Heating and Second-Order Compensation in 65-nm CMOS

报告人：吕文召，湖南大学
指导老师：陈卓俊

摘要：This article presents a voltage reference with ultralow temperature coefficient (TC), which is suitable for high-precision industrial applications. Using a shunt resistor in the current-mode bandgap reference (BGR) achieves a complementary-nonlinear PTAT current for second-order temperature compensation ranging from 10 °C to 85 °C. Additionally, a temperature-locked loop (TLL) is implemented to regulate on-chip self-heating, maintaining a stable die temperature at 10 °C across the ambient range from −40 °C to 10 °C, thereby significantly improving the overall TC. The proposed voltage references have been designed and fabricated using a standard 65-nm CMOS technology. The proposed on-chip self-heating BGR with second-order compensation achieves an average TC of 0.50 ppm/◦C with a standard deviation of 0.12 ppm/°C after one-point trimming from −40 ◦ C to 85 ◦ C. It consumes 23.3 μA at 27 °C and occupies 0.12 mm2.

P77 海报题目：A 140-dB Single-Exposure Wide-Dynamic-Range CMOS Image Sensor Combining LOFIC and Selective Overflow Technology

报告人：马彪，天津大学
指导老师：徐江涛

摘要：This article presents a wide dynamic range (WDR) CMOS image sensor (CIS) integrating lateral overflow integration capacitor (LOFIC) technology and selective overflow architecture, achieving a 140 dB dynamic range (DR) in a single exposure. The proposed pixel architecture modulates the barriers of overflow paths to enable saturated charges overflow through two distinct pathways: effective overflow (captured by LOFIC) and ineffective overflow (discharged via VDD). This unique selective overflow

mechanism equivalently enhances the charge storage capacity of the LOFIC capacitor, strengthening high light detection capabilities and thereby extending the DR. In addition, we propose a count-range-selectable single-slope (SS) analog-to-digital converter (ADC) circuit to resolve the dual-channel readout issue caused by inconsistent readout sequences between high-gain and low-gain signals in LOFIC architectures. This design achieves single-channel readout while maintaining digital correlated double sampling (DCDS) functionality. The prototype chip is fabricated using a 110-nm backside illuminated (BSI) CIS process, featuring a 5 μm × 5 μm pinned photodiode (PPD) pixel and a 14.32 fF LOFIC capacitor. Compared to conventional LOFIC architectures, the proposed selective overflow mechanism extends the DR from 101 dB to 140 dB, with a switching point Signal-to-Noise Ratio (SNR) of 20.5 dB. By selecting appropriate overflow gate parameters, the photo-response non-uniformity (PRNU) at the half-full-well code for the high conversion gain (HCG) output is measured at 0.50%, while the PRNU for the low conversion gain (LCG) output is 0.89%. At an ambient temperature of 60 °C, the dark current of the HCG signal is 181 e^-/s, and that of the LCG signal is 621 e^-/s.

P78 海报题目：A 16-Bit 10-GS/s DAC Achieving > 65 dBc SFDR and < -75 dBc IM3 up to the Nyquist in 28nm CMOS

报告人：马钶卓，清华大学

指导老师：李学清

摘要：This paper presents an approach to mitigating both current source unit deviations and inter-symbol interference (ISI) non-linearities in Nyquist current-steering digital-to-analog converters (DACs). This approach enables switching-activity-controlled data-weighted-averaging (SAC-DWA) with 50% redundant cells by exploiting the input frequency range and the time-domain randomized element transition rate (ETR), leading to an input-independent switching activity. Utilizing SAC-DWA, a 16-bit 10-GS/s DAC is designed in 28 nm CMOS and mounted in a BGA package. In this DAC, the proposed SAC-DWA decoder is implemented in an overflow-detection-based low-complexity state machine to achieve ultra-high speed at 10 GS/s. Additionally, a 1-D merged array placement is adopted to reduce the IR-drop mismatches between the segments of the most and least significant bits. Measurement results show that this DAC achieves spurious-free dynamic range (SFDR) > 70 dBc up to 2.86 GHz and SFDR > 65 dBc with third-order intermodulation distortion (IM3) < −75 dBc over the entire Nyquist band.

P79 海报题目：A 9.5-pJ/bit 40-Mbps Quasi-Static Body Channel Transceiver With Compact Adaptive Equalization

报告人：彭思博，上海交通大学

指导老师：赵健

摘 要： The key challenge in body-coupled communication (BCC) is achieving high-speed and energy-efficient data transmission in dynamically varying channels, particularly addressing variations in dominant pole frequency and channel gain caused by motion and environmental changes in the quasi-static band. This article proposes a broadband BCC transceiver (TRX) with a compact adaptive equalization (CAE) technique to compensate for these variations with minimal power and hardware overhead. The CAE includes three key components: a zero/gain tunable equalizer (ZGTE) for simultaneous gain and zero tuning, a zero-pole locking loop (ZPLL) to lock the equalizer's zero to the channel pole, and a gain control loop (GCL) to track fluctuations in channel gain. Fabricated in a 180-nm CMOS process, the

prototype demonstrates a 49.7× reduction in bit error rate (BER) and a 1.59× improvement in eye opening with ZPLL and GCL enabled, as measured in a 60-cm dynamic in vivo test. The system operates at a data rate of 40 Mbps with an energy efficiency of 9.5 pJ/bit for PAM-4 modulation.

P80 海报题目：A 128×96 Multimodal Flash LiDAR SPAD Imager with Object Segmentation Latency of 18μs Based on Compute-Near-Sensor Ising Annealing Machine

报告人：王靖一，复旦大学
指导老师：刘琦/黄张成

摘 要： This paper presents a 128×96 multimodal flash LiDAR SPAD imager integrated with a compute-near-sensor Ising-model annealing processor for dynamic object segmentation, framed as a combinatorial optimization problem (COP). The system enables real-time updates of Hamiltonian coefficients using a high-bandwidth output-while-write scheme, and accelerates Ising spin iterations by exploiting multimodal SPAD information, achieving a segmentation latency of 18μs.

P81 海报题目：A 24-MHz Crystal Oscillator with 6.9-μs Startup Time and 2% Injection-ΔF Tolerance Using Phase-Interpolator-Assisted Synchronized Injection

报告人：王鑫，南京邮电大学
指导老师：王子轩/蔡志匡

摘要： This article presents a 24-MHz fast startup crystal oscillator with a phase-interpolator-assisted synchronized injection technique. This technique ensures the phase consistency between the injection source and the crystal resonance even with a 2% injection-delta-F, rendering the synchronized injection more flexible and efficient. Additionally, a differential peak detection technique is proposed to detect the phase error incurred by delta-F, shortening the auxiliary non-injection period to merely 4 cycles. Fabricated in a 40-nm CMOS process, the proposed XO achieves a 6.9-us startup time and a 4.8-nJ startup energy with 2% injection inaccuracy when tested with a 24 MHz off-chip crystal. Compared to the traditional injection with constant frequency and phase, the startup time is reduced by 191.3 times. With a power consumption of 63 uW, the phase noise is measured to be -137.8 dBc/Hz at 1-kHz, corresponding to a FoM of 237 dBc/Hz.

P82 海报题目：A 0.037-mm^2, 65.8-nW Temperature and Capacitance Sensor With Analog Pulse-Width-Modulation Backscatter

报告人：吴滔滔，复旦大学
指导老师：闵昊

摘要： Battery-less RFID sensor tags in the Internet of Things (IoT) expect low-cost and power-efficiency multiparameter sensing solutions. Traditional sensor designs rely on time-multiplexed parameter selection to prevent output coupling, which introduces extra control logic and increases cost and design complexity. This paper presents a temperature and capacitance (T/C) sensor with analog pulse-width-modulated (PWM) backscatter. The sensor achieves self-decoupling T/C sensing through the proposed self-switching double sampling (SDS) interface, eliminating the demand for parameter selection. With double sampling, a temperature-sensitive current alternately charges a reference capacitor and a sensing capacitor, simultaneously translating T/C information into a PWM waveform. The low pulse width (LPW) and pulse width ratio (PWR) independently represent temperature and capacitance, enabling simultaneous and decoupled readout. Meanwhile, SDS reuses the PWM waveform as the double-

sampling control signal without external control logic. The PWM signal is sent back by analog PWM backscatter without the need for digitization. The SDS sensor employs a compact, ultra-low-power dual-slope relaxation oscillator (RxO) with inherent self-switching topology for T/C-to-PWM conversion. Fabricated in 55-nm CMOS technology, the sensor occupies 0.037 mm2 and consumes 65.8 nW at 0.8 V. Measurement results show that the T/C sensor achieves a temperature inaccuracy of －1.22/+1.17 ℃ (3σ) in －20~100 ℃ and a capacitance inaccuracy of －197/192 fF (3σ) in 0~35 pF.

P83 海报题目：A 48-Day-Duration Pasting Bioelectronic Device Realizing Closed-Loop Realtime Detection _x000b_and Precision Treatment for Type-1 Diabetes

报告人：吴晓媛，华东师范大学

指导老师：张润曦

摘要： Conventional management of type-1 diabetes (T1D) relies on finger-prick blood sampling or electrochemical methods, which prevent continuous monitoring and treatment. This paper presents a novel epidermal pasting bioelectronic device (PBD). The device integrates a 19fA-resolution bioluminescence analog front-end (BAFE) with TDM-SAR calibration and a hybrid-mode LED driver. It enables closed-loop realtime detection and precision treatment for T1D. The battery life reaches 48 days.

P84 海报题目：A Sub-1V 14b 5.8nW/Hz BW/Power Scalable CT Sensor Interface with a Frequency-Controlled Current Source Achieving a 225× Scalable Range

报告人：武辛婕，浙江大学

指导老师：虞小鹏/唐中

摘要： Precision and energy-efficient sensor interfaces have always been needed in IoT applications. To digitize weak signals (tens of mVs), such as shunt-based current and biomedical sensors, the interface should have low noise [1]–[4]. Moreover, to accommodate different use cases, the bandwidth (BW) and power dissipation of sensor interfaces should be highly scalable [5]–[7]. Sensor interfaces based on discrete-time (DT) ADCs, such as SAR ADCs [8], [9] and FIA-based ΔΣ ADCs [5]–[7] are BW/power scalable, but they usually suffer from kT/C noise (Fig. 27.3.1 top, left). Using a continuous-time (CT) first stage, such as an instrumentation amplifier (IA) [1], [3], [4] (Fig. 27.3.1 top, right), or an active RC integrator [10], [11], can suppress the sampling noise of the following stages, however, they usually consume fixed static power, limiting their BW/power scalability. This work presents an energy-efficient CT-sensor interface based on a Gm-C ΔΣ modulator (DSM) with a frequency-controlled current source (FCCS) and BW/power scalability. It achieves a near-consistent SNDR of ~84dB over a 225× BW range. Compared to the stateof-the-art BW/power scalable works [5-7], it achieves an input-referred noise density of 46nV/rtHz, and an FoM [15] of 178.2dB, showing >3.5× and 2.1dB improvements in noise and energy efficiency, respectively.

P85 海报题目：A 63.9-aF 17.6-bit Adaptive-Load and Configurable Zoom CDC

报告人：夏青江，北京大学

指导老师：陈中建

摘要： This paper presents a Zoom capacitance-to-digital converter (CDC) for single-ended capacitive sensors. An adaptive load scheme proposed reduces gain loss and signal attenuation in pseudo-differential ΔΣM. A configurable Zoom CDC introduced enhances performance at moderate resolution. The prototype is validated using two sensors with a 43.3-pF capacitance range, achieving 1)

63.9-aF resolution (17.6-bit ENOB) and 176.4 dB FoMs in Zoom mode, and 2) 4-μs response time, 173.8 fJ/conversion-step, and power–bandwidth scalability in SAR mode.

P86 海报题目：A Linear Dynamic Voltage Scaling Technique With Adaptive Minimum Voltage Headroom Tracking for Implantable Neurostimulation

报告人：徐洪磊，西北工业大学

指导老师：马彦昭

摘要：This letter presents a linear dynamic voltage scaling (DVS) technique using a dual-loop multistage charge-pump maintaining the minimum voltage headroom for implantable neurostimulation. By adopting an analog DVS with adaptive feedback divider, the stimulus current source could be always kept operating at the boundary of the saturation region and the linear region under different stimulus currents. Furthermore, a simple mode-switched control is introduced to improve the loop response of charge-pump. The design has been fabricated in a 0.18- μm BCD process. The DVS technique increases the measured stimulus efficiency up to 52.8% higher than a fixed supply voltage with a peak efficiency of 89.6% in the range of the stimulus current from 0.5 mA to 0.9 mA.

P87 海报题目：A 110μW 99.5dB-SNDR 20kHz-BW Intrinsically Linear CTDSM with Hybrid Gm-Boosting OTA and Tri-Level FIR DACs

报告人：许欣航，北京大学

指导老师：沈林晓

摘要：This paper presents a power-efficient CTDSM featuring a hybrid Gm-boosting OTA and tri-level FIR DACs. The input integrator employs a concise two-stage feedforward OTA with the hybrid Gm-boosting technique, reducing power consumption by 40% through independent noise/bandwidth optimization and multiple Gm-boosting strategies. This design incorporates an input-boosted OTA that achieves a high gain-bandwidth product (GBW) with a large output swing and a chopped inverter-stacking OTA that minimizes IRN through current reuse.

Combined with a tri-level FIR DAC with deadband switching, the proposed CTDSM, implemented in a 180nm CMOS process, achieves a peak SNDR of 99.5 dB, a dynamic range (DR) of 104 dB, and an SFDR of 110.3 dB. Consuming only 110 μW, the prototype achieves a Schreier FoMSNDR of 182.1 dB and maintains robustness across PVT variations without nonlinearity calibration.

P88 海报题目：A Time-Domain Accuracy-Boosted Temperature Compensated Crystal Oscillator

报告人：尹君扬，清华大学

指导老师：池保勇/邓伟

摘要：This article presents a megahertz temperature compensated crystal oscillator (TCXO) featuring a time-domain accuracy boosting scheme to enhance the signal-to-noise and distortion ratio (SNDR) at the oscillator core's tuning port. The proposed TCXO employs three key techniques: a time-domain architecture that progressively shapes and suppresses offsets in the sensed temperature and applied compensation, an enhanced-decimation filter implementation to eliminate noise from the temperature front end, and a low-noise, high-linearity load capacitance tuning interface to minimize phase noise (PN) and spurs. Implemented in a 0.18-μm CMOS process, the TCXO achieves ±0.6 ppm/±1.4 ppm frequency accuracy over −55 °C to 85 °C/ 115 °C, corresponding to a 38.6×/ 13.2×improvement over uncompensated cases while maintaining competitive noise performance compared with existing

solutions.

P89 海报题目：A 94.8-nW Battery-free Intelligent Silicon Platform for Distributed Multimodal Sensing with Adaptive and Event-driven Computing

报告人：张皓辰，澳门大学
指导老师：麦沛然

摘要： This poster presents an ultra-low power (ULP), battery-free intelligent silicon platform for distributed, multimodal sensing with adaptive, event-driven computing in edge devices. The proposed silicon platform incorporates hardware–software co-design in the implementation. At the algorithm level, a lightweight forward-forward (Lite-FF) algorithm is proposed to enable 1) distributed model training with low-bitwidth operation and a small memory footprint, and 2) event-driven feature transmission. At the circuit level, the digital compute-in-memory (CIM) architecture is employed to accelerate multiply-and-accumulate (MAC) operations with two key features for computation energy efficiency improvement: 1) a sparsity-adaptive input scheduler (SAIS) to skip redundant activation bit-level computations, and 2) a sign-magnitude bit significance accumulator (SM-BSA) to reduce bitline toggling by leveraging weight sparsity in sign magnitude format. Fabricated in 65 nm CMOS, the silicon platform consumes 94.8 nW and 340.4 nW in inference and training mode, respectively. Evaluated on a condition-based monitoring (CbM) task, the proposed framework can achieve a classification accuracy of 90.6% with dual-modal sensing while demonstrating the ability of on-chip training. The proposed compute engine can achieve a peak energy efficiency of 10.7 fJ/MAC at a 0.4 V supply voltage, outperforming the state-of-the-art nanowatt-class neural network (NN) accelerators by 1.76×.

P90 海报题目：An 871 nW 96.2 dB SNDR Pipelined Second-Order Noise-Shaping SAR ADC Employing Charge-Efficient CLS-Assisted Residue Amplifier

报告人：张山，浙江大学
指导老师：谭志超

摘要： This article presents a two-stage pipelined noise-shaping (NS) successive-approximation-register (SAR) analog-to-digital converter (ADC) for sub-micro-watt and high-resolution applications. However, it asks for an accurate residue amplification to avoid severe quantization noise leakage from the frontend stage. Therefore, a charge-efficient correlated-level-shifting (CECLS) assisted residue amplifier (RA) is designed by inserting the level-shifting network (LSN) in a two-stage floating inverter amplifier (FIA). In addition to the inherited low-power merit from FIA, it boosts the equivalent open-loop gain to 92 dB while preventing bandwidth reduction and charge-sharing effects, making the amplification more accurate and faster than prior CLS-assisted amplifiers. The prototype is fabricated using 55 nm CMOS technology and occupies an active area of 0.26 mm2. The measurement results show a 96.2 dB peak-SNDR and 871 nW power consumption under a 1.2 V supply voltage with a 16 kS/s sampling rate. Compared to the recent state-of-the-art ADCs with power under 10 μW and SNDR exceeding 90 dB, this ADC presents the best Schreier FoM of 180.8 dB.

P91 海报题目：A 0.16mm^2 450MHz-BW 72dB-SNDR Continuous-time Pipeline ADC with APF+HPF and APF+FIR Hybrid Delay Alignment Techniques

报告人：赵赫炀，清华大学
指导老师：孙楠

摘要： ADCs with a wide BW over 450MHz and 70dB DR are in high demand for communication applications, where continuous-time pipeline (CTP) ADC can be a power-efficient candidate from a system perspective [1]. However, CTP still faces two major challenges in practice: area consumption and component value variation. For larger input and higher DR, prior CTP works [1], [2] use an LC lattice to achieve accurate in-band delay alignment between the signal path and quantization path, suffering from a large inductor area (0.45mm2 in [2]). Works [3], [4] use RC all-pass filter (APF) as an alternative, but it suffers from inaccurate in-band delay alignment, leading to large input signal leakage. With an RC APF, the magnitude of the leakage with OSR around 4 is equivalent to the quantization error of a 4-bit quantizer, which limits the input magnitude and overall DR of CTP. The sub-ADC-DAC time-interleaving technique is adopted in [5] to attenuate the residue magnitude, but it costs large power and area. The other practical challenge is the process and temperature variations of passive components (R/L/C). Even small RC/LC variation (e.g., ±10%) can cause large delay misalignment and severe leakage, resulting in potential saturation and degraded DR. Therefore, meticulous RC/LC tuning is required in all CTP stages in prior works [1]–[5], which is a high implementation overhead.

P92 海报题目：A 0.18-μg Bias-Instability 0.8-μg/√Hz Resolution Silicon Oscillating Accelerometers with Low-Hysteresis Temperature Extraction and On-Chip Learning-Based Compensation

报告人：邹雨池，上海交通大学
指导老师：赵健

摘要： Temperature drift remains a major limitation to the long-term stability of silicon oscillating accelerometers. Conventional compensation techniques encounter two critical challenges: (1) hysteresis-induced errors in in-situ temperature measurements, and (2) time- and environment-dependent variations in compensation model coefficients, which hinder complete drift cancellation. This work introduces two key innovations to address these issues. First, a digitally programmable gain amplifier enables real-time measurement of the MEMS resonator's quality factor, allowing low-hysteresis temperature estimation by directly linking the resonator amplitude to its structural temperature. Second, a recursive least squares on-chip learning algorithm adaptively updates the compensation coefficients over time, effectively modeling temperature dependencies and suppressing longterm drift. The proposed readout integrated circuit, fabricated in a 0.18－μm CMOS process, integrates MEMS sensing and compensation functionalities. Experimental results demonstrate a bias instability of 0.18μg and a noise density of 0.8－μg/√Hz. These results validate the framework's capability for highprecision inertial sensing in UAVs, UUVs, and compact navigation systems operating under dynamic environmental conditions.

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  Strategic R&D roles with real-world impact
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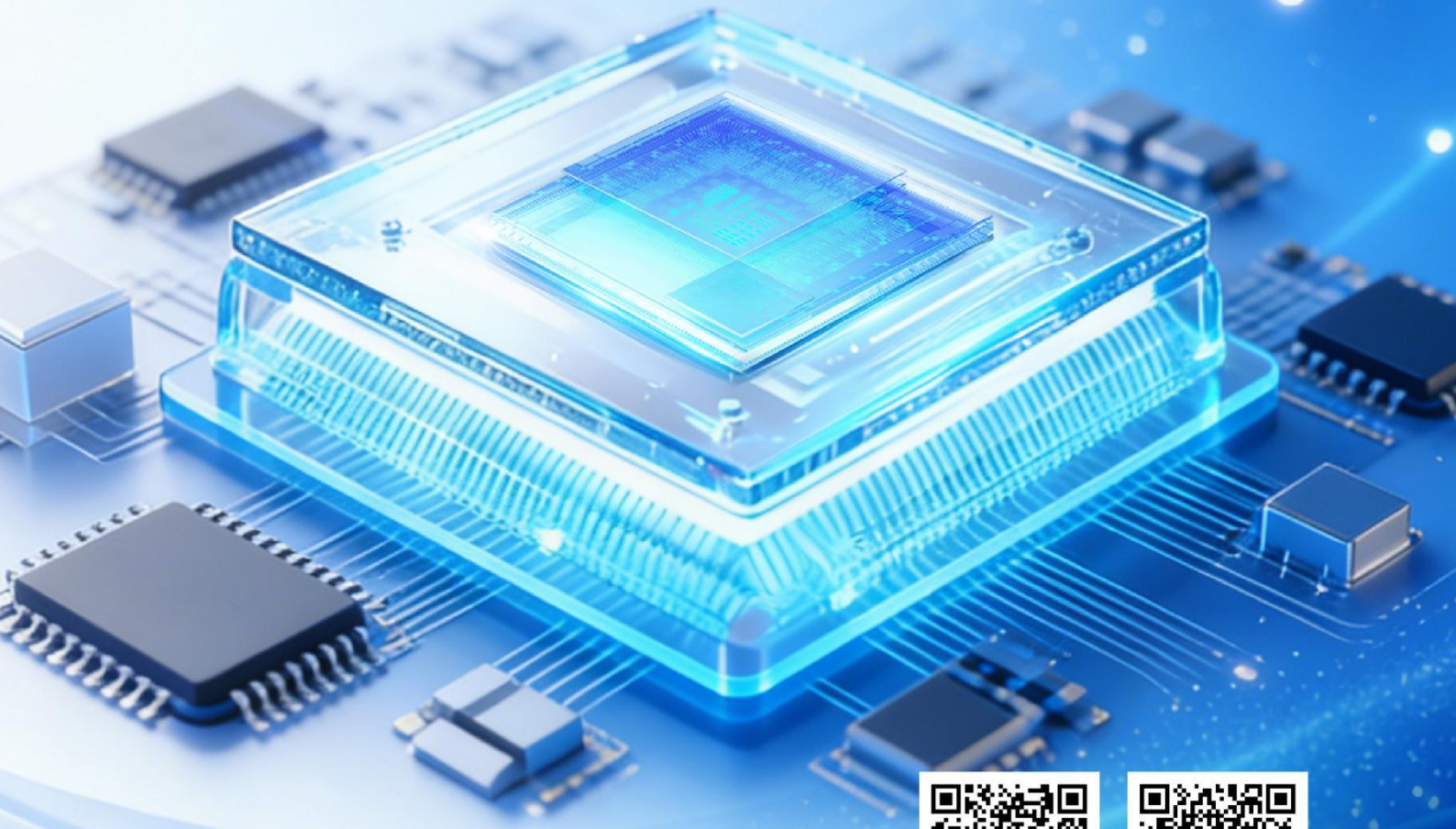
全球领先的
集成电路成品制造和
技术服务提供商



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江城实验室
YANGTZE LABORATORY

江城实验室

关于我们

江城实验室于 2021 年 2 月 18 日成立，是以集成电路先进封装为特色的综合性科研创新平台。实验室聚焦先进封装科学研究、技术创新及重大应用示范，吸引顶尖创新人才，产出重大科研成果。

实验室人员	科技攻关项目	国家发明专利
800+	70+	380+

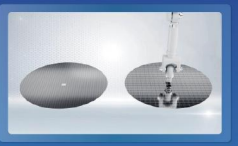
封装突破芯界 集成铸就智能

科研平台

高密度晶圆集成 (HeteroStar®-HBW)

特点：高速、低功耗

互连密度大，对准精度高
高速、低功耗，超高深宽比
访存带宽提升达 20TB/S



芯粒晶圆异质集成 (HeteroStar®-HIC)

特点：不同尺寸、不同功能芯片集成

互连间距、键合精度国际一流
支持硅基异构、多种基材异质集成
支持晶上系统和光电共封等应用

平面高密度芯粒异质封装集成 (HeteroStar®-HiSAP)

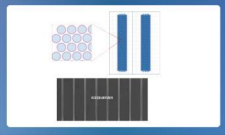
特点：高密芯粒系统集成

多芯粒系统短距互联
系统集成面积突破光罩限制
满足不同存算与互联架构设计

智能微显示交互 (HeteroStar®-AIDI)

特点：小体积，超高分辨率

高密度微缩像素
RGB 三色单片全彩
功耗大副降低



三维微纳传感 (HeteroStar®-3DMEMS)

特点：超精硅结构，高连通

双面硅结构加工
大规模通孔阵列
极限深宽比结构>20:1

具备国际领先的高密度封装能力，对接高校、科研院所、创新团队、高科技企业的智能芯片工艺解决方案。

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MEMO

主办单位

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清華大學 Tsinghua University

北京大學 PEKING UNIVERSITY

東南大學 SOUTHEAST UNIVERSITY

澳門大學 UNIVERSIDADE DE MACAU UNIVERSITY OF MACAU

TUHH

香港科技大學 THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

承办单位

华芯设集成电路技术中心

双钻支持单位

HUAWEI

Witmem 知存科技

钻石支持单位

JCET 长电科技

江城实验室 YANGTZE LABORATORY

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Sino link Technologies

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黄金支持单位

GigaDevice

威智科技 WIZARD TECHNOLOGY

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