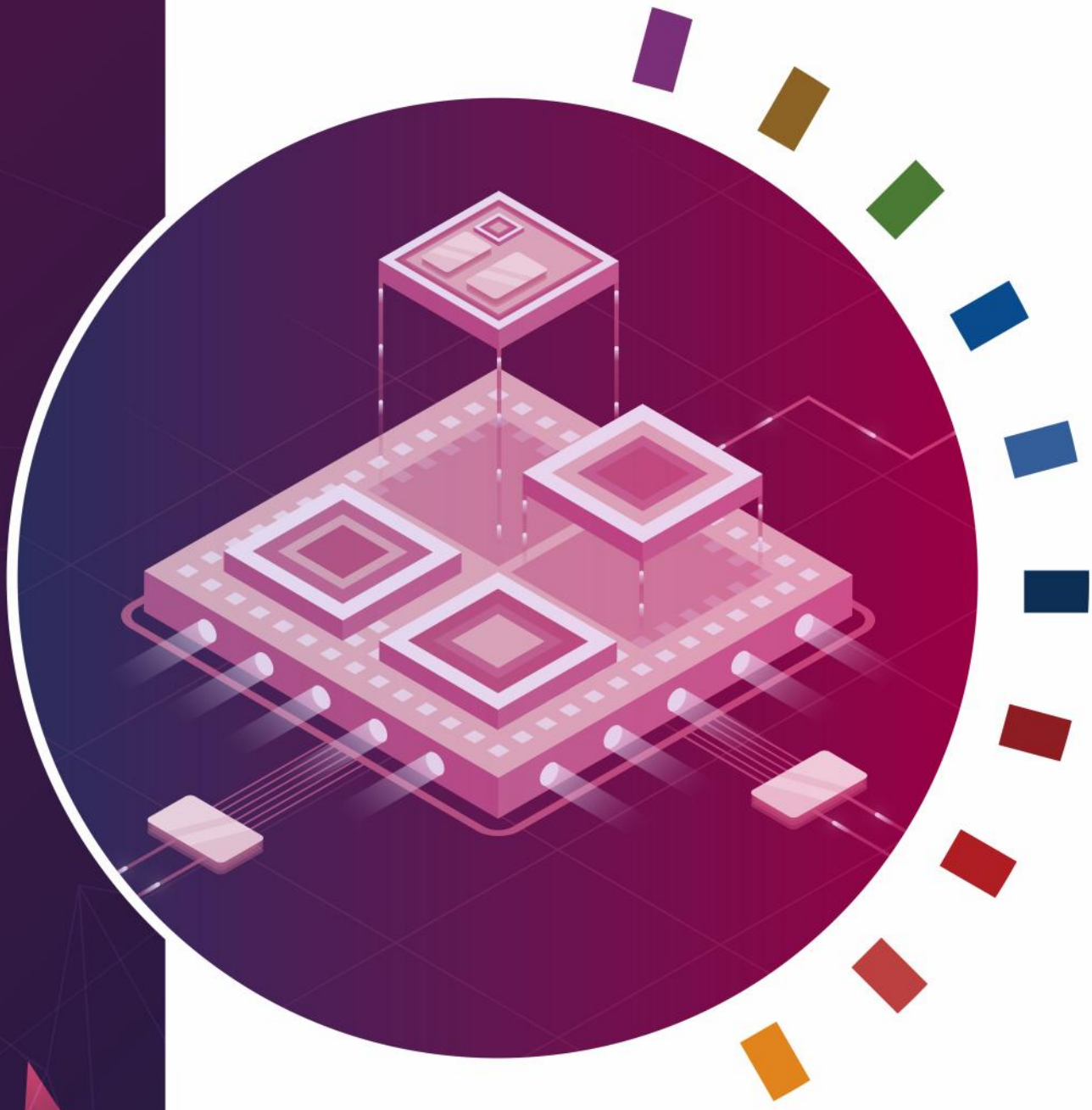
ICAC 2025

PROGRAM
会议 WORKSHOP 手册



华人芯片设计技术研讨会

WORKSHOP ON IC ADVANCES IN CHINA

中国 深圳 | 2025/3/25-28

CONTENT 目录

ORGANIZERS & SPONSORS 主办单位与支持单位

ORGANIZED BY

清华大学 复旦大学 电子科技大学 澳门大学 北京大学 东南大学 香港科技大学

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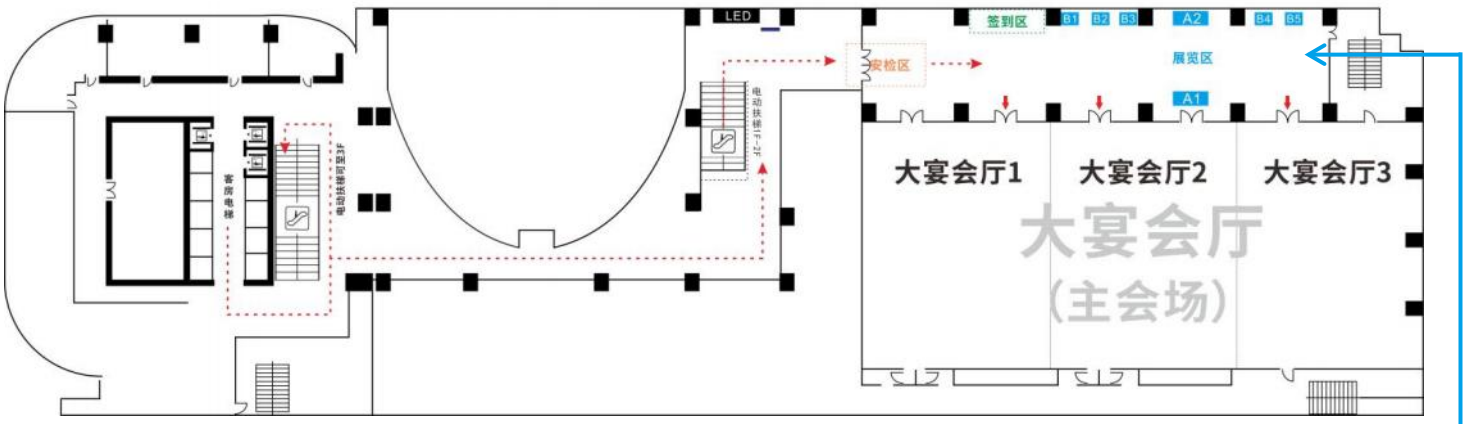
Haikun Jia, Tsinghua University

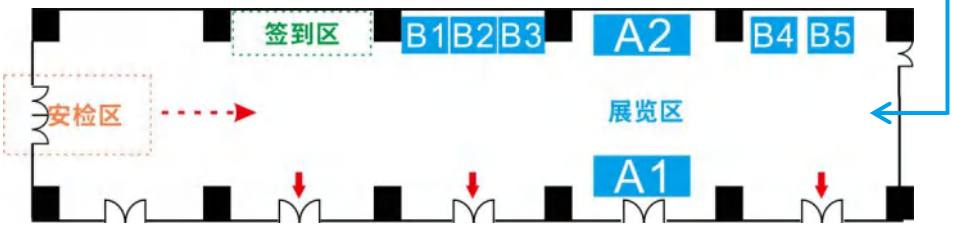
CONFERENCE VENUE 会议地点

中国深圳福田香格里拉大酒店

地址：广东省深圳市福田区中心城益田路 4088 号

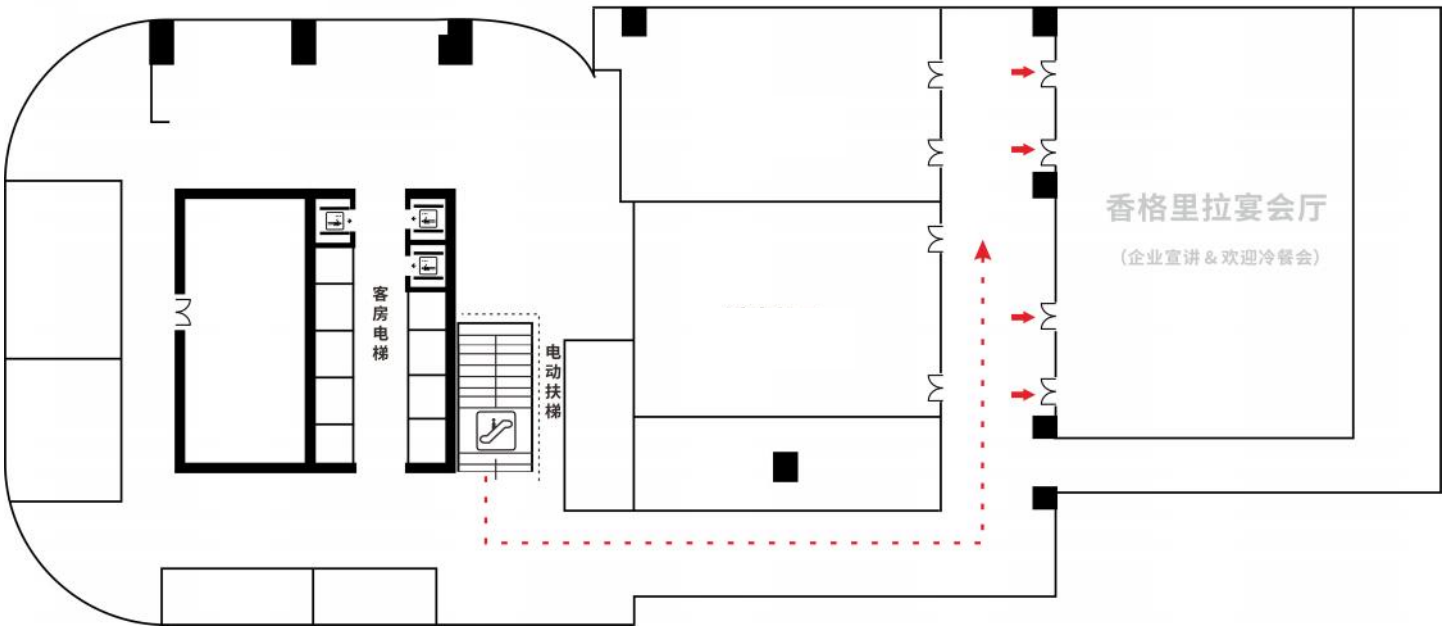
2F





A1	华为	A2	知存科技
B1	共模半导体	B2	思仪科技
B3	纳芯微电子	B4	杰华特微电子
B5	昕原半导体		

3F



PROGRAM AT A GLANCE 会议日程概览

2025 年 3 月 25 日 · 第 0 天		
10:00-20:00	会议签到及会议资料领取	大宴会厅序厅（2F）

2025 年 3 月 26 日 · 第 1 天		
08:30-10:10	培训班 1：Design Your Low Power Delta-Sigma ADC: From 0 to 1 谭志超，浙江大学	大宴会厅 1（2F）
08:30-10:10	培训班 2：mm-Wave Oscillator Design 殷俊，澳门大学	大宴会厅 3（2F）
10:30-12:10	培训班 3：2.5D/3D/3.5D Integration: Fabrication and Chiplet Partition 陈迟晓，复旦大学	大宴会厅 1（2F）
10:30-12:10	培训班 4：High-Performance PLLs: Evolution, Challenges, and Future Directions 邓伟，清华大学	大宴会厅 3（2F）
12:10-14:15	午　休	
14:15-14:30	ICAC 2025 开幕仪式 & ICAC 2024 最佳报告颁奖	大宴会厅（2F）
14:30-15:10	大会报告：Trends in the Power Semiconductor Technology 张波，电子科技大学	
15:10-15:50	大会报告：Recent Progress of Silicon based mm-wave and THz Integrated Circuits and Systems 马凯学，天津大学	
15:50-16:30	大会报告：Computing-in-Memory Processor in the Large-scale AI Model Era 尹首一，清华大学	
16:45-18:30	企业宣讲 & 欢迎冷餐会	香格里拉宴会厅（3F）
18:30-21:00	学生海报展示	大宴会厅 1（2F）

2025 年 3 月 27 日 · 第 2 天			
	大宴会厅 1	大宴会厅 2	大宴会厅 3
	Wireless Components and Transcievers 主持人：桂小琰	Integrated Power Circuits 主持人：路延	CIM Techniques I 主持人：涂锋斌
08:30-08:55	麦沛然	洪志良	张　锋
08:55-09:20	胡春晓	黄　沫	哈亚军
09:20-09:45	赵涤燹	屈万园	陈　勇
09:45-10:10	罗　讯	童志国	贾天宇
10:10-10:30	茶　歇		
	High-speed and High-resolution ADCs I 主持人：沈林晓	Amplifiers and Oscillators 主持人：潘思宁	Frequency Synthesizers and RFDACs 主持人：秦培
10:30-10:55	孙　楠	杨世恒	张　钊
10:55-11:20	陈知行	张奕涵	王　政
11:20-11:45	谭志超	胡远奇	罗　登
11:45-12:10	揭　路	肖知明	钱慧珍
12:10-13:30	午　休		
	Biomedical Innovations and Advanced Sensors 主持人：张奕涵	Application-Driven Power Management 主持人：刘寻	Digital Circuits for Emerging Applications 主持人：于维翰
13:30-13:55	钟龙杰	罗文基	刘勇攀
13:55-14:20	张雅聪	郭建平	刘雷波
14:20-14:45	陈　虹	刘　阳	焦海龙
14:45-15:10	陈铭易	赵广澍	涂锋斌
15:10-15:35	/	路　延	朱浩哲
15:35-15:50	茶　歇		
	Wireline Transceivers and Clock Generations 主持人：张钊	High Performance Oscillators 主持人：王政	Analog Circuits for Emerging Applications 主持人：张雅聪
15:50-16:15	潘　权	秦　培	王　成
16:15-16:40	桂小琰	吴　亮	潘思宁
16:40-17:05	郑旭强	舒一洋	鲁文高
17:05-17:30	许　灏	黄同德	聂凯明

2025 年 3 月 28 日 · 第 3 天			
	大宴会厅 1	大宴会厅 2	大宴会厅 3
	Millimeter-Wave Phased Arrays 主持人：郭开喆	Smart Sensor Interfaces 主持人：姜俊敏	High Performance Wireless Transceivers 主持人：周杰
08:30-08:55	余益明	罗宇轩	宋　飞
08:55-09:20	贾海昆	唐　中	阳至瞻
09:20-09:45	杨孟儒	李家明	王科平
09:45-10:10	王　力	张汐琳	李　巍
10:10-10:30	茶　歇		
	Efficient Circuits and Systems 主持人：司鑫	Emerging DC-DC Converters 主持人：邱浩	Mixed-Signal Circuits 主持人：王科平
10:30-10:55	单伟伟	程　林	祁　楠
10:55-11:20	王　扬	陈之原	赵潇腾
11:20-11:45	杨　杰	姜俊敏	王　辉
11:45-12:10	赵　健	黄俊威	陈卓俊
12:10-13:30	午　休		
	CIM Techniques II 主持人：陈迟晓	Wireless Power Transfer 主持人：程林	High-speed and High-resolution ADCs II 主持人：唐中
13:30-13:55	王　源	邱　浩	刘佳欣
13:55-14:20	司　鑫	薛仲明	沈林晓
14:20-14:45	于维翰	姚　远	沈　易
14:45-15:10	薛晓勇	潘东方	潘江鹏
15:10-15:25	茶　歇		
	Circuits and Systems Beyond 100GHz 主持人：余益明	Wireless Connectivity and Energy Harvester 主持人：潘东方	Wireless Transmitters and mm-Wave Amplifiers 主持人：杨孟儒
15:25-15:50	邓　伟	卢旭阳	周　杰
15:50-16:15	刘力源	陈秋锦	丰光银
16:15-16:40	陈　喆	张兆博	高　立
16:40-17:05	郭开喆	/	杨秉正
17:05-17:30	/	ICAC 2025 闭幕仪式 & ICAC 2025 最佳学生海报颁奖	/

CONFERENCE SCHEDULE 会议日程详情

2025 年 3 月 25 日 · 第 0 天

大宴会厅序厅

10:00-20:00	签到及会议资料领取

2025 年 3 月 26 日 · 第 1 天

大宴会厅 1

08:30-10:10	**培训班 1：Design Your Low Power Delta-Sigma ADC: From 0 to 1** 谭志超，浙江大学

大宴会厅 3

08:30-10:10	**培训班 2：mm-Wave Oscillator Design** 殷俊，澳门大学

大宴会厅 1

10:30-12:10	**培训班 3：2.5D/3D/3.5D Integration: Fabrication and Chiplet Partition** 陈迟晓，复旦大学

大宴会厅 3

10:30-12:10	**培训班 4：High-Performance PLLs: Evolution, Challenges, and Future Directions** 邓伟，清华大学

12:10-14:15 | 午 休

大宴会厅

14:15-14:30	**ICAC 2025 开幕仪式 & ICAC 2024 最佳报告颁奖**
14:30-15:10	**大会报告：Trends in the Power Semiconductor Technology** 张波，电子科技大学
15:10-15:50	**大会报告：Recent Progress of Silicon based mm-wave and THz Integrated Circuits and Systems** 马凯学，天津大学
15:50-16:30	**大会报告：Computing-in-Memory Processor in the Large-scale AI Model Era** 尹首一，清华大学

香格里拉宴会厅（3F）

16:45-18:30	企业宣讲 & 欢迎冷餐会

大宴会厅 1

18:30-21:00	学生海报展示

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Wireless Components and Transcievers 主持人：桂小琰	
08:30 **Talk #2.1**	**A BW-Extended Fourth-Order Gain-Boosted N-Path Filter Employing a Switched gm-C Network** 麦沛然，澳门大学
08:55 **Talk #2.2**	**A Wideband Replicas-Rejection Digital Transmitter Using Joint-Digital-Analog Interpolation and Filtering in 28nm CMOS** 胡春晓，复旦大学
09:20 **Talk #2.3**	**A Packaged 54-to-69-GHz Wideband 2T2R FMCW Radar Transceiver Employing Cascaded-PLL Topology and PTAT-Enhanced Temperature Compensation in 40-nm CMOS** 赵涤燹，东南大学
09:45 **Talk #2.4**	**RFIC: Amplifiers and Array-System** 罗讯，电子科技大学

大宴会厅 2

Integrated Power Circuits 主持人：路延	
08:30 **Talk #3.1**	**Energy Efficiency is the key in PMU and PA design** 洪志良，复旦大学
08:55 **Talk #3.2**	**Multi-phase Hybrid DC-DC Converters** 黄沫，澳门大学
09:20 **Talk #3.3**	**A 12A 89.3% Peak Efficiency and 26mV Undershoot 12V/1V Two-Stage Converter with Regulated Resonant Switched-Capacitor Regulators** 屈万园，浙江大学
09:45 **Talk #3.4**	**HOOP: An Auto-Current-Balanced and Easy-Scalable Hybrid Converters Ring for High Performance Computing** 童志国，澳门大学

大宴会厅 3

CIM Techniques I 主持人：涂锋斌	
08:30 **Talk #4.1**	**A 28nm 192.3TFLOPS/W Accurate/Approximate Dual-Mode-Transpose Digital 6T-SRAM CIM Macro for Floating-Point Edge Training and Inference** 张锋，中国科学院微电子研究所
08:55 **Talk #4.2**	**eCIMC: A 603.1-TOPS/W eDRAM-Based Cryogenic In-Memory Computing Accelerator Supporting Boolean/Convolutional Operations** 哈亚军，上海科技大学
09:20 **Talk #4.3**	**A 28-nm 19.9-to-258.5-TOPS/W 8b Digital Computing-in-Memory Processor With Two-Cycle Macro Featuring Winograd-Domain Convolution and Macro-Level Parallel Dual-Side Sparsity** 陈勇，清华大学
09:45 **Talk #4.4**	**Hardware Accelerators for Diffusion Models Leveraging SRAM Compute-in-Memory and Architecture Optimizations** 贾天宇，北京大学

10:10-10:30 | 茶 歇

大宴会厅 1

High-speed and High-resolution ADCs I 主持人：沈林晓	
10:30 **Talk #5.1**	**High-Speed Pipelined ADC** 孙楠，清华大学
10:55 **Talk #5.2**	**Diverge from The Origins: ADC and Us?** 陈知行，澳门大学
11:20 **Talk #5.3**	**Energy-Efficient Incremental Delta-Sigma ADCs** 谭志超，浙江大学
11:45 **Talk #5.4**	**Filter-Embedded PipeSAR ADC and Floating Charge-Transfering Amplifier** 揭路，清华大学

大宴会厅 2

Amplifiers and Oscillators 主持人：潘思宁	
10:30 **Talk #6.1**	**A 0.4μW/MHz Reference-Replication-Based RC Oscillator with Path-Delay and Comparator-Offset Cancellation Achieving 9.83ppm/°C from -40 to 125°C** 杨世恒，电子科技大学
10:55 **Talk #6.2**	**A 0.36nW, 820μm2, 32kHz Conduction-Angle-Adaptive Crystal Oscillator in 28nm CMOS for Real-Time Clock Applications** 张奕涵，香港科技大学
11:20 **Talk #6.3**	**A 2.30 NEF Split-Steering Amplifier for Switched-Capacitor Circuits With-14.2-dB CM-CM Gain and 100-V/μs Slew Rate** 胡远奇，北京航空航天大学
11:45 **Talk #6.4**	**A 64-Channel Inverter-Based Neural Signal Recording Amplifier With a Novel Differential-Like OTA Achieving an NEF of 0.84** 肖知明，南开大学

大宴会厅 3

Frequency Synthesizers and RFDACs 主持人：秦培	
10:30 **Talk #7.1**	**Design of low-voltage low-jitter PLL: From Integer-N to Fractional-N** 张钊，中国科学院半导体研究所
10:55 **Talk #7.2**	**Low Phase Noise Low Fractional-N Spur Frequency Synthesizer Techniques** 王政，电子科技大学
11:20 **Talk #7.3**	**Design of an All-Digital Fractional Output Divider Using Split-DTC-Based Background Calibration** 罗登，国防科技大学
11:45 **Talk #7.4**	**Linearization Techniques for RFDACs** 钱慧珍，西安电子科技大学

12:10-13:30 | 午 休

大宴会厅 1

Biomedical Innovations and Advanced Sensors 主持人：张奕涵	
13:30 **Talk #8.1**	**A 3-Axis MEMS Gyroscope with 2.8ms Wake-Up Time Enabled by a 1.5μW Always-On Drive Loop** 钟龙杰，西安电子科技大学
13:55 **Talk #8.2**	**A High-Voltage-Compliant 86% Peak Efficiency Current-Mode Stimulator With Dynamic Voltage Supply for Implantable Medical Devices** 张雅聪，北京大学
14:20 **Talk #8.3**	**ANP-O: A 67μW/Channel, 0.13nW/Synapse/Bit Nose-on-a-Chip for Non-invasive Diagnosis of Diseases with On-chip Incremental Learning** 陈虹，清华大学
14:45 **Talk #8.4**	**A 26-G Input-Impedance 112-dB Dynamic-Range Two-Step Direct-Conversion Front-End With Improved 1-Modulation for Wearable Biopotential Acquisition** 陈铭易，上海交通大学

大宴会厅 2

Application-Driven Power Management 主持人：刘寻	
13:30 **Talk #9.1**	**A 91.25% Peak Power-Conversion-Efficiency Capacitive Power Management IC Supporting up to 5.68mJ Burst Energy Delivery Using a Single External Capacitor for mm-Scale IoT Applications** 罗文基，澳门大学
13:55 **Talk #9.2**	**Design of DC-DC regulators with Low Quiescent Current and High Power Efficiency for Battery Powered IoT Devices** 郭建平，中山大学
14:20 **Talk #9.3**	**Pseudo Hysteretic Controlled Gap Time Modulated Isolated DC-DC Converter With Common-Mode Transient Immunity** 刘阳，西安电子科技大学
14:45 **Talk #9.4**	**High-Efficiency Ultrasound Energy Harvesting Interface with Auto-Calibrated Timing Control from -25 °C to 85 °C** 赵广澍，澳门大学
15:10 **Talk #9.5**	**A Bi-Directional Dual-Path Boost-48V-Buck Hybrid Converter for HV Power Transmission in Light-Weight Humanoid Robots** 路延，清华大学

大宴会厅 3

Digital Circuits for Emerging Applications 主持人：于维翰	
13:30 **Talk #10.1**	**3DGS 生成式感知芯片关键技术** 刘勇攀，清华大学
13:55 **Talk #10.2**	**A 28nm 4.05μJ/Encryption 8.72kHMul/s Reconfigurable Multi-Scheme Fully Homomorphic Encryption Processor for Encrypted Client-Server Computing** 刘雷波，清华大学
14:20 **Talk #10.3**	**Nebula: A 28nm 109.8TOPS/W 3D PNN Accelerator Featuring Adaptive Partition, Multi-Skipping, and Block-Wise Aggregation** 焦海龙，北京大学深圳研究生院
14:45 **Talk #10.4**	**A 28nm 0.22μJ/Token Memory-Compute-Intensity-Aware CNN-Transformer Accelerator with Hybrid-Attention-Based Layer-Fusion and Cascaded Pruning for Semantic-Segmentation** 涂锋斌，香港科技大学
15:10 **Talk #10.5**	**SLAM-CIM: A Visual SLAM Backend Processor With Dynamic-Range-Driven-Skipping Linear-Solving FP-CIM Macros** 朱浩哲，复旦大学

15:35-15:50 | 茶 歇

大宴会厅 1

Wireline Transceivers and Clock Generations 主持人：张钊	
15:50 **Talk #11.1**	**High-Speed SerDes and Optical Communications: Equalizations and Modulations** 潘权，南方科技大学
16:15 **Talk #11.2**	**A Low-Latency 200Gb/s PAM-4 Heterogeneous Transceiver for Retimed Pluggable Optics** 桂小琰，西安交通大学
16:40 **Talk #11.3**	**A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Injection-Locked Clock Multiplier Utilizing a Complementary-Injection Scheme and an Adaptive Pulsewidth Adjustment** 郑旭强，中国科学院微电子研究所
17:05 **Talk #11.4**	**An 8-to-28GHz 8-Phase Clock Generator Using Dual-Feedback Ring Oscillator in 28nm CMOS** 许灏，复旦大学

大宴会厅 2

High Performance Oscillators 主持人：王政	
15:50 **Talk #12.1**	**A Differential Series-Resonance CMOS VCO with Pole-Convergence Technique Achieving 202.1dBc/Hz FoMTA at 10MHz Offset** 秦培，华南理工大学
16:15 **Talk #12.2**	**A 47.3-to-58.4GHz Differential Quasi-Class-E Colpitts Oscillator Achieving 198.8dBc/Hz FoMT** 吴亮，香港中文大学（深圳）
16:40 **Talk #12.3**	**Class-G Impedance-Modulation Multi-Core Power Oscillator for High Pout and Power Back-Off Efficiency Enhancement** 舒一洋，电子科技大学
17:05 **Talk #12.4**	**An 18.5-to-23.6GHz Quad-Core Class-F23 Oscillator Without 2nd/3rd Harmonic Tuning Achieving 193dBc/Hz Peak FoM and 140-to-250kHz 1/f3 PN Corner in 65nm CMOS** 黄同德，南京理工大学

大宴会厅 3

Analog Circuits for Emerging Applications 主持人：张雅聪	
15:50 **Talk #13.1**	**Shushan: Cryogenic Silicon Integrated Circuits for the High Fidelity Quantum Interface** 王成，电子科技大学
16:15 **Talk #13.2**	**A 143dB Dynamic Range 119dB CMRR Capacitance-to-Digital Converter for High-Resolution Floating-Target Displacement Sensing** 潘思宁，清华大学
16:40 **Talk #13.3**	**A 320×256 6.9mW 2.2mK-NETD 120.4dB-DR LW-IRFPA with Pixel-Paralleled Light-Driven 20b Current-to-Phase ADC** 鲁文高，北京大学
17:05 **Talk #13.4**	**A 1920×1080 Array 2D/3D Image Sensor with 3μs Row-Time Single-Slope ADC and 100MHz Demodulated PPD locked-in Pixel** 聂凯明，天津大学

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Millimeter-Wave Phased Arrays 主持人：郭开喆	
08:30 **Talk #14.1**	**A Reconfigurable Phased-Array Transceiver Front-End for 5G New Radio** 余益明，电子科技大学
08:55 **Talk #14.2**	**Research on Millimeter-wave Multi-beam Phased Array in CMOS Process** 贾海昆，清华大学
09:20 **Talk #14.3**	**K/Ka-Band Hybrid-Packaged Four-Element Four-Beam Phased-Array Transmitter and Receiver Front-Ends With Optimized Beamforming Passive Networks** 杨孟儒，南京航空航天大学
09:45 **Talk #14.4**	**A Compact Ka-Band Phased-Array Transmitter with On-Chip Phase-Locked Loop** 王力，香港科技大学

大宴会厅 2

Smart Sensor Interfaces 主持人：姜俊敏	
08:30 **Talk #15.1**	**Sensor Interface Circuits for Large-Scale Tactile Sensing** 罗宇轩，浙江大学
08:55 **Talk #15.2**	**A Sub-1V 14b BW/Power Scalable CT Sensor Interface with a Frequency-Controlled Current Source** 唐中，杭州万高科技股份有限公司
09:20 **Talk #15.3**	**A 4,100μm2 Wire-Metal-Based Temperature Sensor with a Fractional-Discharge FLL and a Time-Domain Amplifier with ±0.2°C Inaccuracy (3σ) from −40 to 125°C and 45fJ·K2 Resolution FoM in 28nm CMOS** 李家明，澳门大学
09:45 **Talk #15.4**	**Millimeter-sized Wireless Electrochemical Sensing SoC** 张汐琳，清华大学

大宴会厅 3

High Performance Wireless Transceivers 主持人：周杰	
08:30 **Talk #16.1**	**A 28nm Multimode Multiband RF Transceiver with Harmonic Rejection TX and Spur Avoidance RX Supporting LTE Cat1bis** 宋飞，芯翼信息科技（上海）有限公司
08:55 **Talk #16.2**	**Power-efficient Transceiver Techniques for Long-Range IoT Applications** 阳至瞻，澳门大学
09:20 **Talk #16.3**	**A Low-Power Blocker-Tolerant Wideband Receiver With Bias-Tunable Mixer and Effective Switch Resistance Compensation** 王科平，天津大学
09:45 **Talk #16.4**	**Compact Full-Duplex Receiver with Wideband Multi-Domain Hilbert-Transform-Equalization Cancellation Based on Multi-Stage APFs Achieving 65dB SIC Across 120MHz BW** 李巍，复旦大学

10:10-10:30 | 茶 歇

大宴会厅 1

Efficient Circuits and Systems 主持人：司鑫	
10:30 **Talk #17.1**	**DSC-TRCP: Dynamically Self-Calibrating Tunable Replica Critical Paths Based Timing Monitoring for Variation Resilient Circuits** 单伟伟，东南大学
10:55 **Talk #17.2**	**A Versatile Transformer Accelerator With Low-Rank Estimation and Heterogeneous Dataflow** 王扬，清华大学
11:20 **Talk #17.3**	**An Energy-Efficient Unstructured Sparsity-Aware Deep SNN Accelerator With 3-D Computation Array** 杨杰，西湖大学
11:45 **Talk #17.4**	**A 0.67-to-5.4 TSOPs/W Spiking Neural Network Accelerator With 128/256 Reconfigurable Neurons and Asynchronous Fully Connected Synapses** 赵健，上海交通大学

大宴会厅 2

Emerging DC-DC Converters 主持人：邱浩	
10:30 **Talk #18.1**	**A Multi-Core Isolated DC-DC Converter with Embedded Magnetic-Core Transformer and Low EMI Emissions** 程林，中国科学技术大学
10:55 **Talk #18.2**	**Enhancing Efficiency in Piezoelectric Energy Harvesting: Cross-Flip Synchronized Switch Harvesting on Capacitors Rectifier and Multi-Output DC-DC Converters Utilizing Shared Capacitors** 陈之原，复旦大学
11:20 **Talk #18.3**	**Batter-to-36V Continous Current Boost Converter** 姜俊敏，南方科技大学
11:45 **Talk #18.4**	**A Dual-Loop Non-Uniform-Multi-Inductor Hybrid DC-DC Converter with Specified Inductor Current Allocation and Fast Transient Response** 黄俊威，澳门大学

大宴会厅 3

Mixed-Signal Circuits 主持人：王科平	
10:30 **Talk #19.1**	**Silicon-Photonic Transceiver Design for Co-Packaged Optics** 祁楠，中国科学院半导体研究所
10:55 **Talk #19.2**	**A Reference-Less CDR Using SAR-Based Frequency Acquisition Technique Achieving 55ns Constant Band-Searching Time and up to 63.64 Gb/s/μs Acquisition Speed** 赵潇腾，西安电子科技大学
11:20 **Talk #19.3**	**A 1.8GHz-3.0GHz Fully Integrated All-In-One CMOS Frequency Management Module Achieving -47/+42ppm Inaccuracy from -40°C to 95°C and -150/+70ppm After Accelerated Aging** 王辉，上海交通大学
11:45 **Talk #19.4**	**A Compute-in-Memory Annealing Processor with Interaction Coefficient Reuse and Sparse Energy Computation for Solving Combinatorial Optimization Problems** 陈卓俊，湖南大学

12:10-13:30 | 午 休

大宴会厅 1

CIM Techniques II 主持人：陈迟晓	
13:30 **Talk #20.1**	**SKADI: A 28nm Complete K-SAT Solver Featuring Dual-Path SRAM-Based Macro and Incremental Update with 100% Solvability** 王源，北京大学
13:55 **Talk #20.2**	**A 28nm 17.83-62.84TFLOPS/W Broadcast-Alignment Floating-Point-Compute-in-Memory Macro with Non-2's Complement MAC for CNNs and Transformers** 司鑫，东南大学
14:20 **Talk #20.3**	**Breaking the Readout Wall: Energy Efficient In-Memory Processing Techniques for AIoT** 于维翰，澳门大学
14:45 **Talk #20.4**	**High-Density SRAM Design for Computing in Memory** 薛晓勇，复旦大学

大宴会厅 2

Wireless Power Transfer 主持人：程林	
13:30 **Talk #21.1**	**A 6.78-MHz Single-Stage Regulating Rectifier with Dual Outputs Simultaneously Charged in a Half Cycle Achieving 92.2%-Efficiency and 131-mW Output Power** 邱浩，南京大学
13:55 **Talk #21.2**	**A 6.78MHz 94.2% Peak Efficiency Class-E Transmitter with Adaptive Real-part Impedance Matching and Imaginary-part Phase Compensation Achieving a 33W Wireless Power Transfer System.** 薛仲明，西安交通大学
14:20 **Talk #21.3**	**A 13.56-MHz Single-Input Dual-Output Wireless Power and Data Transfer System for Bio-Implants** 姚远，香港科技大学
14:45 **Talk #21.4**	**A Dual-LC-Resonant Isolated DC-DC Converter Achieving 65.4% Peak Efficiency and Inherent Backscattering** 潘东方，中国科学技术大学

大宴会厅 3

High-speed and High-resolution ADCs II 主持人：唐中	
13:30 **Talk #22.1**	**A Fully Dynamic Noise-Shaping SAR ADC Achieving 120dB SNDR and 189dB FoMs in 1kHz BW** 刘佳欣，电子科技大学
13:55 **Talk #22.2**	**Rail-to-Rail ADC Input Buffer Designs Employing Continuous-Time Correlated Level Shifting and Split Coarse-Fine Techniques** 沈林晓，北京大学
14:20 **Talk #22.3**	**Energy-Efficient Pipelined ADC with Parallel-Operation SAR Sub-Quantizer and Dynamic Deadzone Ring Amplifier** 沈易，西安电子科技大学
14:45 **Talk #22.4**	**Bandpass Delta-Sigma modulators based on N-path Filters** 潘江鹏，香港中文大学

15:10-15:25 | 茶 歇

大宴会厅 1

Circuits and Systems Beyond 100GHz 主持人：余益明	
15:25 **Talk #23.1**	**D-Band Distributed MIMO Radar Transceiver and System** 邓伟，清华大学
15:50 **Talk #23.2**	**A 3 THz CMOS Image Sensor** 刘力源，中国科学院半导体研究所
16:15 **Talk #23.3**	**Silicon-based THz Direct Modulation Communications** 陈喆，东南大学
16:40 **Talk #23.4**	**A 0.68-THz Receiver With Third-Order Subharmonic Mixing in 65-nm CMOS** 郭开喆，东南大学

大宴会厅 2

Wireless Connectivity and Energy Harvesters 主持人：潘东方	
15:25 **Talk #24.1**	**Integrated Wireless Power Transfer, Communication, and Actuation** 卢旭阳，上海交通大学
15:50 **Talk #24.2**	**A Single-Input RF Energy-Harvesting Interface With Compensated-CEPE Control and 3-D Hill-Climbing MPPT Achieving — 28.5 dBm Sensitivity** 陈秋锦，澳门大学
16:15 **Talk #24.3**	**A High-Effieiency Low-Cost Multi-Antenna RF Energy Harvesting System With Leakage Suppression** 张兆博，南方科技大学

大宴会厅 3

Wireless Transmitters and mm-Wave Amplifiers 主持人：杨孟儒	
15:25 **Talk #25.1**	**A Phase-Modulation Phase-Shifting Phased-Array Transmitter With Phase Self-Calibration and Deep PBOs Efficiency Enhancement** 周杰，电子科技大学
15:50 **Talk #25.2**	**Silicon-Based Wideband Low-Noise Amplifier for mm-Wave Wireless Communications** 丰光银，华南理工大学
16:15 **Talk #25.3**	**A Compact Millimeter-wave Reconfigurable Dual-band LNA with Image-rejection in 28-nm Bulk CMOS for 5G Application** 高立，华南理工大学
16:40 **Talk #25.4**	**A 56-to-64GHz Linear Power Amplifier with 30.2dBm Psat and 23.5% PAEpeak Using Scalable Matched-Zone-Expanding Radial Power Combining with EM-Loss Reduction in 40nm Bulk CMOS** 杨秉正，电子科技大学

大宴会厅 2

17:05-17:30	**ICAC 2025 闭幕仪式 & ICAC 2025 最佳学生海报颁奖**

PLENARY TALK 大会报告

2025 年 3 月 26 日 · 第 1 天

大宴会厅

Talk #1.1 / 14:30-15:10

张波

电子科技大学

张波，电子科技大学集成电路研究中心主任，教授、博导，天府杰出科学家，四川省优秀教师。兼（曾）任国家 01、02 科技重大专项总体组专家，中国电源学会元器件专委会主任，四川电子学会半导体集成技术专委会主任等。长期从事功率半导体芯片技术研究，以第一完成人两次荣获国家科技进步二等奖（2010 年度、2023 年度），并获国家及省部级科技奖励 18 项，发表 SCI 论文 800 余篇，授权中美发明专利 400 余项，带领电子科技大学功率集成技术实验室已培养毕业 1200 余名研究生，为全球功率半导体领域最大的人才培养基地；产学研合作成效显著，与企业合作开发工艺与产品 200 余项，为合作企业新增直接经济效益达数百亿元人民币。

TALK

Trends in the Power Semiconductor Technology

The presentation focuses on the trends in the power semiconductor technology. It analyzes the development trend of power semiconductor devices from the fields of “More Silicon“ and “More than Silicon“, and analyzes the development of silicon-based power semiconductor devices by taking “More MOSFET“ and “More IGBT“ as examples. The development of power semiconductor devices not only needs to continuously improve the performance of power semiconductor devices based upon the device structure, but also needs to improve the process, larger wafers, thinner wafers, smaller size, more integration, and using of VLSI advanced process is an important direction for the development of power semiconductor devices. The development of power semiconductor devices should merge “More Devices“ and “More Than Devices“. Different applications have different performance requirements for the same type of device. There is no best device, only the suitable product. In the More Than Silicon section, the presentation provides an analysis of the development trends of the most popular wide-bandgap power semiconductor devices.

2025 年 3 月 26 日 · 第 1 天

大宴会厅

Talk #1.2 / 15:10-15:50

马凯学

天津大学

天津大学讲席教授、博导、IEEE Fellow、中国电子学会会士、国家杰青、国务院特殊津贴专家。现任天津大学微电子学院院长、天津国家“芯火”双创平台负责人、智能传感材料全国重点实验室副主任、天津市集成电路协会会长、天津市成像与感知微电子技术重点实验室主任等。从业 27 年（企业 10 年）先后在航天 504 所和新加坡科技电子等单位工作。从事射频、毫米波电路与系统和天线传播研究，国际上提出集成悬置线集成电路和可重构毫米波芯片技术，承担国家重点研发专项和国家重点基金等项目。发表英文专著 3 部, IEEE 期刊文章 240 余篇，专利 60 余项，成果落地应用获天津市科技进步一等奖等奖项,入选天津市杰出人才和“天津发展人才先锋”十大年度人物等。曾任中国电子学会青年科学家微波与电路系统专委会首任主任和国际微波期刊 IEEE TMTT 副主编等。担任中国电子学会空间电子学分会副主任委员等。

TALK

Recent Progress of Silicon based mm-wave and THz Integrated Circuits and Systems

With the advantages of excellent penetration, broad bandwidth and good security, millimeter-wave (mm-wave) and Terahertz (THz) has been drawn much attention in China, USA, Europe and worldwide for both academy and industry society. mm-wave band has been already assigned for future 5G/6G applications and THz technique has been recognized as the one of ten techniques in 21 century which can change the future world. With down-scaling of the commercial silicon process, which has been verified as one of excellent candidates for commercial 5G/6G mm-wave and THz applications like communication and sensing etc. in terms of the low cost, compact size and high integrity etc. This talk will present the progress silicon based circuits and systems of mm-wave and THz. The chips development of our group in the frequency range like 28GHz/39GHz, 140GHz, 220GHz, 2.5THz and up to 28.3THz will also be introduced. The challenge and future trend of the silicon-based mm-wave and THz will also be presented.

2025 年 3 月 26 日 · 第 1 天

大宴会厅

Talk #1.3 / 15:50-16:30

尹首一

清华大学

尹首一，清华大学教授，集成电路学院副院长，IEEE Fellow**，国家杰出青年科学基金获得者，中国高被引学者。研究方向为可重构计算、人工智能芯片设计。 已发表学术论文** 200 **余篇，包括** ISSCC、VLSI、ISCA、MICRO、HPCA、DAC **和** IEEE JSSC、TPDS、TCSVT、TVLSI、TCAS-I/II **等集成电路和体系结构领域学术会议和权威期刊。出版《可重构计算》《人工智能芯片设计》专著** 2 **部。曾获国家技术发明二等奖、中国电子学会技术发明一等奖、中国发明专利金奖、教育部技术发明一等奖、江西省科技进步二等奖、中国电子学会优秀科技工作者奖、中国电子信息领域优秀科技论文奖。现任集成电路领域国际会议** ISCA、MICRO、FPGA **和** A-SSCC **的技术委员会委员，《中国科学：信息科学》编委，国际期刊《**ACM Transactions on Reconfigurable Technology and Systems**》及《**Integration, the VLSI Journal**》的** Associate Editor。

TALK

Computing-in-Memory Processor in the Large-scale AI Model Era

With the rapid development of large-scale AI models represented by DeepSeek, AI computing has entered a new era. The massive parameter scale and multimodal learning capabilities of large models enable them to handle more complex and general-purpose intelligent tasks, while also raising tremendous demand for high-performance AI processors. However, the frequent and extensive data movement severely restricts the AI processor performance due to the von Neumann bottleneck. Computing-in-memory (CIM) architecture, which deeply integrates compute and memory, offers a promising solution to break through this limitation and achieve a balance between high performance and energy efficiency. However, in the large-scale AI model era, CIM processors face new challenges such as mixed-precision computing, sparsity processing, massive parameter storage, and inter-chip communication. This report will discuss how to design CIM processors with multi-level architecture innovations to tackle these challenges and provide high-performance and efficient support for the large-scale AI model deployment.

TUTORIAL 芯片设计培训班

2025 年 3 月 26 日 · 第 1 天

大宴会厅 1

08:30-10:10

谭志超

浙江大学

Zhichao Tan (Senior Member, IEEE) received the B.Eng. degree from Xi'an Jiaotong University, Xi'an, China, in 2004, the M.Eng. degree from Peking University, Beijing, China, in 2008, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 2013.

He was a Staff IC Design Engineer working on low-power, high-precision analog/mixed-signal circuit design with Analog Devices Inc., Wilmington, MA, USA, from 2013 to 2019. He joined Zhejiang University, Hangzhou, China, as a Faculty Member in 2019. His research interests include energy-efficient sensor interfaces, precision analog circuits, and ultra-low-power analog-to-digital converters (ADCs). This has resulted in over 85 technical journal and conference papers. He holds five U.S. patents.

Dr. Tan is a TPC member of the IEEE Custom Integrated Circuits Conference. He was a TPC member of the IEEE Asian Solid-State Circuits Conference. He has served as Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: REGULAR PAPERS, IEEE Sensors Journal, and IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.

TUTORIAL

Design Your Low Power Delta-Sigma ADC： From 0 to 1

Delta-Sigma ADCs are the most widely used solutions to high-precision conversion applications. This tutorial provides a comprehensive overview of delta-sigma ADCs with basic principles and design examples. We start with the concepts of oversampling and noise shaping. We cover various behavioral topologies and circuit implementations of delta-sigma ADCs, revealing the trade-offs and design considerations for higher energy efficiency. Recent advances in low-power delta-sigma ADCs will also be provided. This tutorial provides intuitive explanations and design insights, aiming to help the beginners have a solid understanding and quickly get started with designing their own delta-sigma ADCs.

2025 年 3 月 26 日 · 第 1 天

大宴会厅 3

08:30-10:10

殷俊

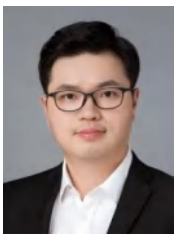
澳门大学

殷俊于 2004 和 2007 年分别获得北京大学微电子学士和硕士学位，并于 2013 年获得香港科技大学电子与计算机工程博士学位。现为澳门大学模拟与混合信号超大规模集成电路国家重点实验室副教授。他的研究方向包括时钟产生与低功耗无线收发机芯片，于本领域高水平国际期刊与会议发表论文超过 90 篇。殷教授现担任国际固态电路会议 ISSCC 以及欧洲固态电路会议 ESSCIRC 的技术委员会成员。他还曾担任电路与系统领域旗舰期刊-电路与系统学报 TCAS-I 的副主编（2020-2023），以及亚洲固态电路会议 A-SSCC 的技术委员会成员（2019, 2021-2022）。

TUTORIAL

mm-Wave Oscillator Design

High-performance, low-phase-noise oscillators are heavily demanded by high-throughput and high-fidelity mm-wave transceivers. The content of this tutorial includes: (1) the oscillator's performance matrix and key Figure of Merit (FoM); (2) the reactive-load design, namely - inductors/transformers and tunable capacitors, for achieving high quality factor and the design challenge for mm-wave oscillators; (3) various oscillator topologies to reduce phase noise at the mm-wave frequency, such as Class-C and harmonic shaping; (4) the design of multi-core synchronized oscillator, which provides an opportunity for further reducing phase noise; (5) frequency tuning range extension for multi-core oscillators with the aid of mode-switching and multi-resonance techniques.



2025 年 3 月 26 日 · 第 1 天

大宴会厅 1

10:30-12:10

陈迟晓

复旦大学

陈迟晓。复旦大学芯片与系统前沿技术研究院副研究员，集成芯片与系统全国重点实验室集成芯片创新中心主任、绍芯实验室（复旦-绍兴研究院）副主任、国家优青、上海市青年科技启明星。主要研究领域包括面向 AI 芯片的跨层次设计方法学、感存算一体电路与架构、Chiplet 异质异构集。以第一、通信作者发表多篇集成电路设计领域的高水平论文，包括 ISSCC、MICRO、HPCA、DAC、IEEE JSSC, TCAS-I/II，JETCAS 等。任亚洲固态电路会议 A-SSCC 技术委员会成员。

TUTORIAL

2.5D/3D/3.5D Integration: Fabrication and Chiplet Partition

随着人工智能时代大模型、大算力需求的飞速发展，基于传统单芯片高性能处理器的设计方法面临存储墙、功耗墙和面积墙等诸多技术瓶颈。基于精密半导体工艺的 2.5D/3D 集成技术为新一代高性能处理器提供了新的基于。本次培训将介绍 2.5D/3D/3.5D 集成工艺的基本原理，如硅中阶层、硅通孔等。同时，也将介绍高性能计算处理器芯片设计中，在基于上述 2.5D/3D 工艺时，互连接口的电路设计，以及系统架构如何实现分解，并介绍团队在基于有源硅中介层（Active Interposer）的设计要点。

2025 年 3 月 26 日 · 第 1 天

大宴会厅 3

10:30-12:10

邓伟

清华大学

清华大学长聘副教授，入选国家高层次人才计划和国家青年人才计划。电子科技大学学士和硕士，日本东京工业大学博士，曾在美国苹果公司总部任资深主任工程师，负责面向高速无线通信 SoC 的毫米波和混合信号芯片设计。现任职清华大学集成电路学院，主要研究方向为硅基射频/毫米波/太赫兹芯片设计与系统集成。

现任 ISSCC、VLSI、CICC、RFIC、A-SSCC 和 ESSCIRC 的技术委员会成员，IEEE SSCS 杰出讲师，以及 IEEE JSSC、IEEE SSC-L、半导体学报等期刊副主编或客座编辑，负责射频和无线方向。在 JSSC、IEEE T-CAS I、IEEE T-MTT 等期刊以及 ISSCC、VLSI 等国际会议发表论文 160 余篇，其中在 JSSC 和 ISSCC 发表论文 40 余篇；主持射频和无线芯片设计领域的多项国家重点科研项目。

TUTORIAL

High-Performance PLLs: Evolution, Challenges, and Future Directions

Phase-locked loop (PLL) is one of the key techniques for both communication and radar systems. Various functions in communication and radar systems, including clock generation, frequency synthesis, serial-to-parallel conversion, frequency and phase modulation, clock synchronization and distribution, coherent and non-coherent demodulation, clock and carrier recovery, directly or indirectly rely on PLLs. High performance PLL is one of the cutting-edge topics in the field of integrated circuit and system design. It involves various research directions such as mixed-signal circuit design, digital algorithms, and system-level architecture. This lecture will discuss the high-performance PLL circuit and architecture evolution, review the latest research progress and discuss the future development trends of high-performance PLLs.

INVITED TALK 邀请报告

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #2.1 / 08:30-08:55

麦沛然

澳门大学

麦沛然，澳门大学教授、模拟与混合信号超大规模集成电路国家重点实验室主任、微电子研究院副院长、长江学者讲座教授、澳门教育功绩勋贤、葡国科学院院士(外籍) 、中国科学院海外专家、IEEE Fellow、IET Fellow 和英国皇家化学会会士(RSC Fellow)。麦教授先后担任 IEEE SSCS 和 CASS 理事会委员、CASS 杰出演讲人主席、IEEE SSCS 和 CASS 杰出演讲人。麦教授主要从事集成电路和跨学科系统研究，在模拟和射频电路理论与设计、数字微流控技术与应用、微型核磁共振和成像等领域具有广泛影响力。先后主持国家重点实验室项目、粤港澳聯合實驗室项目、港澳科技成果来粤转化项目、澳门科学技术发展基金重点研发专项和国家科技部联合项目等 10 余项。孵化高科技公司实现了模拟电路和数字微流控技术的产业化。麦教授先后担任 IEEE Solid-State Circuits Letters (SSCL) 总主编，IEEE Press、JSSC、TCAS-I、TCAS-II、JETCAS 和 SSCL 等高级/副主编，国际会议 ISSCC, ESSCIRC 和 A-SSCC 委员和联合创办华人芯片设计技术研讨会 ICAC。麦教授 2011 年获国家科学技术进步二等奖、2019 年获国庆 70 周年纪念章和选为国庆 70 周年彩车人物代表、国庆 75 周年国宴代表、2012 年起获澳门科技发明奖和特别奖共 9 项、2022 年获澳门首个腾讯科学探索奖和 2023 年获 ISSCC 70 周年杰出贡献者奖等。麦教授长期致力于电路设计普及和推广，在世界一流大学和芯片公司作专题讲学 100 余次，并多次于 IEEE 国际会议作主题演讲，在顶级期刊和国际学术会议上发表论文 500 余篇，在 IEEE 核心系列期刊上发表论文 150 余篇(含 JSSC 54 篇)，获授权中国及美国发明专利 30 余项。2011 至 2025 年间连续 15 年发表国际顶尖会议 ISSCC 论文共 44 篇。

TALK

A BW-Extended Fourth-Order Gain-Boosted N-Path Filter Employing a Switched gm-C Network

This work is a bandwidth (BW)-extended gain-boosted N-path filter with a switched gm–C network, in which a 4th-order response is achieved with the subtraction method by shifting the baseband (BB) admittance with poly-phase gm cells in the BB. It features not only in-band RF gain and high- Q bandpass response but also other valuable properties, such as a wide passband BW and a high linearity. In addition, a class-A/-B amplifier is employed to provide the RF gain, in which the linearity is optimized with a tunable bias voltage. Fabricated in a 65-nm CMOS process, our proposed filter measures a 10.7–12.7-dB voltage gain and a 5.3–6.2-dB noise figure (NF) over a 0.5–1.5-GHz RF range. With gm-linearity optimization, our filter centered at 1 GHz exhibits an out-of-band input-referred 3rd-order intercept point (OB-IIP3) of 18.2 dBm and a passband BW of 50 MHz. The ultimate stopband rejection of the filter is >50 dB. The power consumption is 11.1–15.9 mW, and the die area is 0.083 mm^2.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #2.2 / 08:55-09:20

胡春晓

复旦大学

Chunxiao Hu received the B.S. degree from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2017, the M.S. degree from the University of Chinese Academy of Sciences, Beijing, China, in 2020, and the Ph.D. degree with the School of Microelectronics from Fudan University, Shanghai, China, in 2024. Her research interests focus on energy-efficient all-digital transmitters, digitized RF circuits and digital baseband signal processing circuits.

TALK

A Wideband Replicas-Rejection Digital Transmitter Using Joint-Digital-Analog Interpolation and Filtering in 28nm CMOS

A wideband replicas-rejection DTX with joint-digital-analog interpolation and filtering technique is proposed. Polyphase architecture with equivalence order of operations is employed for better replicas rejection with low power consumption. Integration of analog interpolation into DPA along with pre-filter further eliminates replicas to support wideband applications. The DTX achieves wide frequency coverage of 2.1-5.1GHz, peak Pout of 27.8dBm with 30.4% SE, >42dBc wideband replicas rejection, and only 0.88mm2 core size with a single 1.1V supply.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #2.3 / 09:20-09:45

赵涤燹

东南大学

赵涤燹，东南大学教授，紫金山实验室教授，天锐星通首席科学家。主要研究方向为 5G 毫米波通信和宽带卫星通信 CMOS 毫米波芯片和集成相控阵，发表论文 120 余篇。研究成果入选 2020 年度高等学校十大科技进展，国家十三五科技成果展，2021 年度中国电子学会科学技术奖（技术发明）一等奖，2022 年度中国半导体十大研究进展，2022 年度信息通信领域十大科技进展，2023 年度国家技术发明二等奖。

TALK

A Packaged 54-to-69-GHz Wideband 2T2R FMCW Radar Transceiver Employing Cascaded-PLL Topology and PTAT-Enhanced Temperature Compensation in 40-nm CMOS

This talk presents a highly integrated V-band frequency-modulated-continuous-wave (FMCW) radar transceiver (TRX) in 40-nm bulk CMOS. It incorporates two identical transmitter (TX) and receiver (RX) channels, enabling not only traditional forward sensing but also full-360° detection. The FMCW synthesizer is based on a cascaded-phase-locked-loop (PLL) topology, enhancing chirp quality while reducing the necessity for complex off-chip components. A proportional-to-absolute-temperature (PTAT)-enhanced temperature compensation (TC) technique is proposed to improve the temperature robustness at V-band. The impacts of clock synchronization and temperature insensitivity of the TRX on FMCW radar systems are also discussed. For broadband, high-linearity, and low-noise operation within limited stages, RF front-ends are carefully designed with the optimization strategy elaborated. The proposed TRX achieves a 3-dB bandwidth ranging from 54 to 69 GHz. The RX features a 67-dB tuning range of the conversion gain (CG) and a 10-dB noise figure (NF). The Psat of TX is 12.8 dBm. The PTAT-enhanced TC effectively minimizes variations in CG, NF, and PSAT , maintaining less than 2.1-, 2.9-, and 2.5-dB changes, respectively, from -55 °C to 105 °C. The FMCW generator achieves a chirp rate of 468.5 MHz/μs with a bandwidth of 7.2 GHz, demonstrating a minimal 0.019% chirp error.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #2.4 / 09:45-10:10

罗讯

电子科技大学

罗讯，博士，电子科技大学教授；国家高层次人才计划入选者、IEEE 杰出青年工程师奖获得者、爱思唯尔-斯坦福大学全球前 2%顶尖科学家（终身/年度）。研究方向：射频集成电路及其系统集成、可重构无源电路与模组、微型化三维集成封装等。兼任/曾任 IEEE Microwave and Wireless Components Letters 责任主编、IEEE Journal of Microwaves 领域编辑、IEEE Open Journal of the Solid-State Circuits Society 副编辑、IEEE Microwave Magazine 特邀编辑等；兼任 IEEE IMS 技术分委会主席，兼任/曾任 ISSCC、EuMW、RFIC、CICC 技术委员会委员等。

TALK

RFIC: Amplifiers and Array-System

This presentation will firstly focus on the power amplifier (PA) and array-system requirements of 5G-Advanced (5G-A) RFICs. Then, the on-chip fast self-calibration switched-capacitor PA and wideband digital-RF phased-array transceiver using conventional CMOS technology will be discussed.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #3.1 / 08:30-08:55

洪志良

复旦大学

洪志良，瑞士苏黎世高等理工学院博士，复旦大学教授，博导。

TALK

Energy Efficiency is the key in PMU and PA design

Whether use new architecture or innovel circuit technique, PMU and PA designers will pay the energy efficiency in the first! This presentation will introduce our two works, "A Fully Integrated Digital Polar Transmitter With Single-Ended Doherty PA and DLL-Based Three-Segment Hybrid DTC in 28 nm CMOS" and "A 94.4% Peak Efficiency Coupled-Inductor Hybrid Step-Up Converter With Load-Independent Output Voltage Ripple", published in JSSC 2024.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #3.2 / 08:55-09:20

黄沫

澳门大学

于 2005，2008，2014 年分别在中山大学微电子学与固体电子学专业获得本科，硕士，博士学位。2008 至 2014 年，在广晟微电子有限公司，作为项目经理参与了 TD-LTE，TD-SCDMA 等多款商用芯片的研发设计。2014 年 12 月至 2016 年 9 月，在澳门大学 AMSV 国家重点实验室任博士后。2016 年 10 月至 2019 年 8 月，在华南理工大学电子与信息学院，任副教授。2019 年 9 月至今，加入澳门大学 AMSV 国家重点实验室，任助理教授。主要研究方向为电源管理和能量 IC 设计。获授权 23 项中国发明专利，2 项美国专利。黄沫博士获得了 ISSCC 2017 菅野卓雄远东杰出论文奖（中国大陆和港澳地区首次）。指导的博士生获得 2024 SSCS 博士成就奖。现担任 ISSCC 和 CICC 的 TPC 成员，以及 JoS，MEJ 的副主编。

TALK

Multi-phase Hybrid DC-DC Converters

This report presents the design methodology of a multi-phase hybrid converters with inherent inductor current balancing, together with fast transient response and wide VCR range.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #3.3 / 09:20-09:45

屈万园

浙江大学

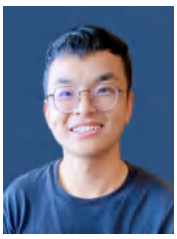
屈万园博士为浙江大学集成电路学院教授、博士生导师、教育部青年长江学者，博士毕业于韩国科学技术院， 2008 年至 2017 年就职于韩国 LG 公司从事集成电路研发工作，历任工程师、资深工程师、责任工程师/项目主管；2017 年起加入浙江大学并工作至今，长期从事数模混合集成电路设计相关研究工作，主要研究方向为面向三维异构集成的高密度电源管理芯片设计，包括混合电源拓扑的架构构建方法和优化理论、高动态电源环路的控制策略和驱动技术等。

在产业领域，领导量产多款国际领先的高性能电源管理芯片，获授权美国发明专利 9 项、韩国发明专利 5 项、中国发明专利 3 项；在学术领域，发表集成电路设计领域最高水平的国际固态电路会议 ISSCC 和固态电路期刊 JSSC 论文多篇，包括浙江大学为第一单位的首篇 ISSCC 论文，获评国际固态电路会议 2021 年度丝绸之路奖、2022 年度亮点论文。目前担任多个 IEEE 高水平会议技术委员会成员。

TALK

A 12A 89.3% Peak Efficiency and 26mV Undershoot 12V/1V Two-Stage Converter with Regulated Resonant Switched-Capacitor Regulators

This work presents a two-stage 12V/1V converter for the vertical power delivery, which adopts a regulated resonant switched-capacitor (RReSC) second stage. The proposed RReSC always operates in the ideal non-regulation mode during steady-state, while maintain voltage regulation during the transients. Therefore, compared with the prior two-stage counterparts, this work shows the best system level efficiency of 89.3% and the best load transient responses with 26mV undershoot under a 4A load step.



2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #3.4 / 09:45-10:10

童志国

澳门大学

童志国，先后于 2018 年，2021 年，2024 年于天津大学，复旦大学，澳门大学取得学士，硕士，博士学位。现任澳门大学博士后研究员，主要研究方向为应用于高性能计算和人形机器人的电源管理芯片设计；并在集成电路领域顶级会议 ISSCC 和期刊 JSSC 发表 8 篇论文，其中第一作者发表 5 篇（含共一 1 篇）。并获 2024-2025 IEEE 固态电路学会博士生成果奖，PwrSoC 2023 最佳学生海报奖等。

TALK

HOOP: An Auto-Current-Balanced and Easy-Scalable Hybrid Converters Ring for High Performance Computing

AI is booming. So is the computing power used to train AI models. To satisfy the enormous current demand, the power solution providing large current and high efficiency is strongly required. This work presents an auto-current-balanced and easy-scalable hybrid converters ring structure. It features Hybrid converters with a power ring (O) for current balance and a back ring (O) for phase shedding for computing Power delivery, named as HOOP. By placing the HOOP structure on the backside of the xPU load in a ring configuration, the current can be delivered vertically to the xPUs via short paths, greatly reducing both the on-board and in-package I^2R losses. Implemented with 180nm BCD process, a maximum current of 16A with four chips is implemented, and a single-chip current density of 1.1A/mm2 is achieved.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #4.1 / 08:30-08:55

张锋

中国科学院微电子研究所

张锋，中科院微电子所研究员，博士生导师。从事先进集成电路研究二十余年，先后包括主持重点研发计划项目（两项）、863 计划、自然科学基重点项目金等多个国家级课题，参与了十余项国家重大项目的研发，完成了多款芯片的研制开发。在 nature electronics、isscc、JSSC、TCASI 等杂志发表文章 70 余篇。

TALK

A 28nm 192.3TFLOPS/W Accurate/Approximate Dual-Mode-Transpose Digital 6T-SRAM CIM Macro for Floating-Point Edge Training and Inference

To address the high energy efficiency requirements for inference and training computations in edge computing, we propose a digitally reconfigurable SRAM in-memory computing macro unit. It supports INT4, INT8 fixed-point formats and FP8, BF16 floating-point formats. It can be configured to operate in approximate or precise computation modes to balance the trade-off between energy efficiency and accuracy. The average energy efficiency for FP8 floating-point operations can reach 192 TFLOPS/W.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #4.2 / 08:55-09:20

哈亚军

上海科技大学

哈亚军教授于 1996 年获浙江大学电子工程学士学位，2000 年获新加坡国立大学电子工程硕士学位，2004 年获比利时鲁汶大学电子工程博士学位。他是上海科技大学教授，IEEE 电路与系统学会理事会理事（Board of Governors），IEEE Transactions on Circuits and Systems II: Express Briefs（2022-2023）主编(Editor-in-Chief)（2022-2023），国家自然科学基金“外国资深学者”，“重点国际（地区）合作研究”和“叶企孙”科学基金获得者，上海高能效与定制人工智能 IC 工程研究中心主任，以及上海科技大学后摩尔器件和集成系统中心主任。他曾是新加坡信息通信研究所 I2R-BYD 联合实验室主任，以及新加坡国立大学电气与计算机工程系的兼职副教授。他的研究兴趣包括 FPGA 电路/架构/工具、超低功耗数字集成电路和系统，以及以上研究在智能汽车、机器学习和硬件安全中的应用。他已在 TCAS I & II 、TVLSI、TC、JSSC 以及 DAC 和 ISSCC 等国际知名期刊和会议上发表了一百五十多篇学术论文，并获得多项最佳论文奖。他是 ISICAS 2022 国际会议的技术委员会共同主席(TPC Co-Chair)，包括 IEEE Transactions on Circuits & Systems I、IEEE Transactions on Circuits & Systems II、IEEE Transactions on Very Large Scale Integration (VLSI) Systems 等国际期刊的编委（Associate Editor），也曾担任过 ASP-DAC 2014 国际会议的共同大会主席（General Co-Chair）等。

TALK

eCIMC: A 603.1-TOPS/W eDRAM-Based Cryogenic In-Memory Computing Accelerator Supporting Boolean/Convolutional Operations

Cryogenic in-memory computing (IMC) presents a promising solution to achieve higher energy efficiency in data-intensive computations at extremely low temperatures. However, existing IMC macros fail to fully exploit the cryogenic device characteristics, such as ultra-low leakage, to optimize the entire circuits at cryogenic temperatures. This article presents a 144-Kb embedded dynamic random access memory (eDRAM)-based cryogenic IMC accelerator (eCIMC), supporting energy-efficient operations in different modes, including the conventional memory operation, the Boolean operation, and the convolutional operation. First, we optimize the cryogenic three-transistor (C3T) eDRAM bitcell to support multi-mode operations with high retention time. Second, we design an adaptive and reconfigurable sense amplifier (ARSA) to efficiently process both memory and Boolean operations by taking advantage of the C3T to store the reference voltage. Third, we present a 4-bit flash analog-to-digital converter (ADC) with 15 ARSAs and a four-cycle reference voltage generation scheme to achieve fast and low-power cryogenic convolutions. Measurement results of our test-chip show that the eCIMC achieves an average energy efficiency of 603.1 TOPS/W (4b ×4 b) and a computing density of 284 TOPS/mm2 (4b ×4 b). Moreover, the retention time of our eCIMC has been significantly improved to 9.1 s at 4.2 K.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #4.3 / 09:20-09:45

陈勇

清华大学

陈勇博士，2005 年毕业于中国传媒大学（原北京广播学院）广播电视工程专业；2010 年在中国科学院微电子研究所完成博士学位；2010 年进入清华大学微电子研究所做博士后研究；2013 年起在新加坡南洋理工大学 VIRTUS 做 Research Fellow；2016 年至 2024 年在澳门大学的模拟与混合信号超大规模集成电路国家重点实验室，先后任助理教授和长聘副教授；2023 年入选国家海外高层次人才引进计划创新项目（海外长江）；2024 年加入清华大学电子系，现任长聘副教授。陈勇博士，一直专注集成电路的人才培育和原创研发，主持了国家海外高层次人才引进计划创新项目（海外长江）。已有三名博士生获得优秀青年科学基金项目（海外）资助。在模拟/混合信号/射频/毫米波/亚太赫兹/有线通信等领域的主要国际期刊及国际会议发表学术论文 160 多篇，授权中国专利 19 项。另外，担任多种期刊的副主编、主题主编或客座主编和多个国际会议的技术委员。于 2009 年荣获“海西”（两岸三地）研究生集成电路设计竞赛的二等奖；2020 年荣获澳门科学技术发明一等奖；2022 年荣获澳门科学技术发明二等奖；连续三年 (2020-2022) 荣获 IEEE TVLSI Systems 期刊的最佳副主编奖；2022 年荣获 IEEE TVLSI Systems 期刊的最佳审稿人奖；2023 年 IEEE 固态电路协会（SSCS）首届 SSCS 审稿人奖；2024 年 IEEE SSCS 杰出审稿人奖。指导学生获得 IEEE APCCAS 2019 的最佳论文奖；IEEE RFIC 2021 最佳学生论文奖（三等奖）和 PRIME 2023 的金叶奖。

TALK

A 28-nm 19.9-to-258.5-TOPS/W 8b Digital Computing-in-Memory Processor With Two-Cycle Macro Featuring Winograd-Domain Convolution and Macro-Level Parallel Dual-Side Sparsity

Recently, computing in memory (CiM) has been proven to be an energy-efficient and promising architecture for AI algorithms. And yet, current CiM schemes generally suffer from limited throughput compared to their digital counterparts, and the key reason is that the CiM macro calculation must iterate through multiple cycles. Thus, the need to reduce the calculation cycle of the macro while keeping high energy efficiency and the necessity of developing acceleration methods for the universal CiM-based processor have become major issues faced by the current CiM architectures. To surmount these critical problems, we propose a processor based on a two-cycle CiM macro. Our work makes three main contributions: (i) we present a Radix16-based digital-CiM macro with look-up table optimization to reduce dynamic power consumption; (ii) we devise a hybrid Winograd microarchitecture and dataflow that supports (2,3) and (4,3) Winograd convolution, meaning that a good compromise can be reached between the accuracy of the algorithm and the reduction in workload; (iii) we propose a macro-level parallel dual-side sparse CiM core that uses a horizontal direction compression method to reduce the input cycle of activation data and improve the mapping efficiency of the weight data in the macros. A prototype of the processor is fabricated in a 28-nm CMOS, which achieves a peak system energy efficiency of 19.9-258.5-TOPS/W for a voltage supply of 0.6–1.1 V, and an operating frequency of 78–287 MHz, a 2.25–7.05× higher than other state-of-the-art CiM processors.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #4.4 / 09:45-10:10

贾天宇

北京大学

贾天宇，北京大学集成电路学院助理教授、博雅青年学者。美国西北大学博士，哈佛大学博士后，前卡耐基梅隆大学助理研究教授。研究兴趣包括人工智能加速器、SoC 芯片架构设计、敏捷设计方法等。在 ISSCC、VLSI、JSSC、MICRO 等芯片领域会议期刊发表科研论文 50 余篇。承担基金委重点项目、重点研发计划课题等多个国家级项目，曾获 2020 年固态电路协会博士成就奖 IEEE SSCS Predoctoral Achievement Award，2020 年美国西北大学 ECE 系最佳博士论文奖等。

TALK

Hardware Accelerators for Diffusion Models Leveraging SRAM Compute-in-Memory and Architecture Optimizations

The emergence of Diffusion models has attracted widespread attention in the field of artificial intelligence generated content (AIGC). Although Diffusion demonstrates impressive image generation capabilities, it faces hardware deployment challenges due to its unique model structure and computational requirements. This presentation will discuss accelerator architectures leveraging SRAM compute -in-memory and architecture bandwidth optimizations to meet the flexible data reuse requirements in diffusion models. The accelerator is evaluated for multiple diffusion models for image, 3D and video generations, with significant energy efficiency improvements obtained.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #5.1 / 10:30-10:55

孙楠

清华大学

孙楠，清华本科，哈佛博士，IEEE Fellow。他曾获美国德克萨斯大学奥斯丁分校终身教职，目前担任清华大学电子工程系长聘正教授。2013 年获美国自然科学基金 Career Award，2018 年入选国家海外高层次人才计划，2020 年获 IEEE 固态电路协会 New Frontier Award，2023 年获北京市五四青年奖章。曾任 IEEE 电路与系统协会和固态电路协会杰出讲师，JSSC 和 TCAS-I 编委，CICC 大会主席，以及 ISSCC 和 ASSCC 的技术委员会委员。他担任过多家世界知名芯片设计公司的咨询顾问。他培养了 27 名博士生，其中 11 人在中美高校任教，包括 Gatech、ASU、清华、北大、成电、西电、西交等。他在集成电路芯片设计领域顶级期刊 JSSC 和会议 ISSCC 发表论文 60 余篇。

TALK

High-Speed Pipelined ADC

This talk will present two high-speed pipelined ADC design: 1) A 3GS/s 12b Pipelined ADC with Gated-LMS-Based Piecewise-Linear Nonlinearity Calibration; and 2) An 8b 10GS/s 2-Channel Time-Interleaved Pipelined ADC with Concurrent Residue Transfer and Quantization, and Automatic Buffer Power Gating

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #5.2 / 10:55-11:20

陈知行

澳门大学

陈知行 1985 年出生于中国澳门。在 2008 年他取得了美国华盛顿大学（西雅图）电子工程学士学位。分别于 2012 年和 2015 年在澳门大学取得硕士和博士学位。他目前是澳门大学模拟与混合信号超大规模集成电路国家重点实验室的副教授和 IEEE 固态电路澳门分会的主席。因其在微电子方面的研究成果，获得中华人民共和国教育部 - 高等学校科学研究优秀成果奖科学技术(自然科学奖)一等奖，并共 5 次获得澳门科学技术发展基金的技术发明奖。他负责指导的论文获得 ISSCC2024 菅野卓雄远东杰出论文奖，他是 2015 年 IEEE 固态电路协会预博士成就奖的得奖者，也是 2014 年欧洲固态电路会议最佳论文奖的共同获奖者。他的指导学生获得 IEEE 固态电路协会预博士成就奖及亚洲固态电路会议学生设计竞赛——杰出设计奖。他在数据转换器、时钟电路及飞时测距感测等领域共有 27 篇固态电路期刊（JSSC）和 22 篇国际固态电路会议（ISSCC）论文。他是 IEEE 高级会员、也是 2023 亚洲固态电路会议的技术评审委员。他的研究兴趣包括高速奈奎斯特，噪声整形 ADC 和低抖动时钟电路

TALK

Diverge from The Origins: ADC and Us?

This year, once again, it is not surprising that China stands out at ISSCC, particularly in the data converter sub-committee. Over two-thirds of the papers are from China. This simultaneously rings the bell that our innovations will shape the data converter community. As researchers, it is crucial for us to remain committed to maintaining a sustainable and healthy academic environment. In this talk, I will share my thoughts and examples from our group.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #5.3 / 11:20-11:45

谭志超

浙江大学

Zhichao Tan (Senior Member, IEEE) received the B.Eng. degree from Xi'an Jiaotong University, Xi'an, China, in 2004, the M.Eng. degree from Peking University, Beijing, China, in 2008, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 2013.

He was a Staff IC Design Engineer working on low-power, high-precision analog/mixed-signal circuit design with Analog Devices Inc., Wilmington, MA, USA, from 2013 to 2019. He joined Zhejiang University, Hangzhou, China, as a Faculty Member in 2019. His research interests include energy-efficient sensor interfaces, precision analog circuits, and ultra-low-power analog-to-digital converters (ADCs). This has resulted in over 85 technical journal and conference papers. He holds five U.S. patents.

Dr. Tan is a TPC member of the IEEE Custom Integrated Circuits Conference. He was a TPC member of the IEEE Asian Solid-State Circuits Conference. He has served as Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: REGULAR PAPERS, IEEE Sensors Journal, and IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.

TALK

Energy-Efficient Incremental Delta-Sigma ADCs

Incremental data converters are optimal choices in sensor interface circuits with high accuracy, low latency, and simpler filter design. This report will first distinguish the incremental converters from the free-running counterparts. Then, advanced circuit operating styles like pseudo-pseudo-differential operation and popular dynamic amplifiers are included. Finally, two state-of-the-art case studies will be presented.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #5.4 / 11:45-12:10

揭路

清华大学

揭路，助理教授， 2013-2017 年于浙江大学信息与电子工程学院获学士学位，2017-2021 年于美国密歇根大学（University of Michigan）电气与计算机工程系（ECE）获博士学位，获国家海外青年人才项目支持、北京市青年人才托举项目支持。2022 年 5 月加入清华大学集成电路学院任职助理教授。主要研究方向为先进数模混合集成电路设计，重点包括高精度、高速及低功耗的混合架构模数转换器（ADC）、可重构数模混合电路、数模混合计算等。近年在集成电路设计领域的一流会议和期刊上发表论文 30 余篇，提出了多种新型 ADC 架构并多次刷新同类 ADC 的指标记录。目前担任 CICC、ASSCC、ICTA 会议技术委员会委员(TPC)以及 JSSC、TCASI、TCASII 等多个期刊的审稿人。

TALK

Filter-Embedded PipeSAR ADC and Floating Charge-Transfering Amplifier

This work presents a filter-embedded pipe-SAR ADC with 70.1dB SNDR over 80MHz BW. It introduces a progressive conversion scheme that mitigates the speed penalty of the filtering operation, and adopts a dynamic floating-charge transferrer to achieve high-speed, high-efficiency and robust residue amplification. The prototype ADC consumes 4.9mW, achieves a Schreier FoM of 172.2dB, provides >30dB out-of-band suppression for full-scale blockers, and is highly scalable in the clock frequency.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #6.1 / 10:30-10:55

杨世恒

电子科技大学

杨世恒，电子科技大学研究员、博士生导师。本科（2014 年）、博士（2019 年）毕业于澳门大学，历任澳门大学模拟与混合信号超大规模集成电路国家重点实验室研究助理，博士后研究员及研究助理教授。研究方向为模拟、射频集成电路设计。在集成电路设计领域顶级会议、期刊发表多篇论文，担任 IEEE Solid-State Circuits Letters 副主编。

TALK

A 0.4μW/MHz Reference-Replication-Based RC Oscillator with Path-Delay and Comparator-Offset Cancellation Achieving 9.83ppm/°C from -40 to 125°C

It reports an open-loop reference-replication-based RC oscillator that can concurrently calibrate the temperature-sensitive path delay and comparator offset. A dynamic loop control allows substantial power savings. The prototyped 10MHz RC oscillator in 65nm CMOS consumes 4.06μW, corresponding to a power efficiency of 0.4μW/MHz. The achieved TC is 9.83 ppm/°C from -40 to 125 °C, and the die area is 0.0085mm2. This work outperforms them in term of temperature coefficient (to 9.83 ppm/°C) and energy efficiency (0.4 μW/MHz), while showing the best-in-class timer's stability FoM of 174dB and power-jitter FoM of 285dB.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #6.2 / 10:55-11:20

张奕涵

香港科技大学

张奕涵，2013 年本科毕业于清华大学微纳电子系，2020 年博士毕业于哥伦比亚大学电子工程系博士学位。现为香港科技大学助理教授，主要研究方向为低功耗电路与系统设计，与面向生物医疗应用的集成电路与系统设计，其研究成果曾发表于 ISSCC/VLSI/CICC 等集成电路会议，与 Nature Communications /PNAS/JSSC 等集成电路与跨领域期刊上。

TALK

A 0.36nW, 820µm2, 32kHz Conduction-Angle-Adaptive Crystal Oscillator in 28nm CMOS for Real-Time Clock Applications

This talk introduces our latest work on ultra-low power crystal oscillator design, which aims to advance state-of-the-art performance while reclaiming the ease of use at sub-nW power regime. Unlike recently published pulse-injection crystal oscillators, our proposed circuit uses amplitude-domain information to adaptively control the crystal oscillator's conduction angle. Such a class-C-like operation can be easily implemented using charge pumps in advanced technology nodes. Our proposed topology, "conductive-angle-adaptive crystal oscillator" (CAAXO), was verified using 28 nm CMOS technology. The prototype IC occupies only 820 µm2 of active area and achieves 0.36 nW of power, with inherent startup capability, holding the promise to serve as a pin-to-pin upgrade of Pierce oscillators.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #6.3 / 11:20-11:45

胡远奇

北京航空航天大学

任北京航空航天大学集成电路科学与工程学院副院长，长期从事高精度模拟及数模混合信号集成电路设计研究。主持国自然重点、北自然重点、企业委托等项目 10 余项，获批经费 3000 余万元。目前担任科技部“十四五”国家重点研发计划“微纳电子技术”重点专项总体专家组成员、IEEE 旗舰期刊 TBioCAS 编委等职务。

TALK

A 2.30 NEF Split-Steering Amplifier for Switched-Capacitor Circuits With-14.2-dB CM-CM Gain and 100-V/µs Slew Rate

This article presents three techniques to improve the split-steering amplifier's (SSA) performance and robustness. At the system level, differential-mode charge neutralization (DMCN) is introduced first to reset the circuit with minimum burden. Second, a DMCN-compatible common-mode feedforward (CMFF) strategy is introduced to reduce the impact of common_x0002_mode (CM) disturbance without introducing extra noise or sacrificing the bandwidth. The above two techniques are universal and can be applied in other pseudo-differential (PD) amplifier architectures. As for circuit implementation, two ring amplifiers (RAs) with different dead zones (DZs) are paralleled with the SSA to improve the slew rate (SR) of the overall amplifier. Dynamic bias adjustment is used to increase the response speed of the RAs and ensure that they will not be activated after slewing, which is critical to keep the overall amplifier low noise. The measured results demonstrate a −14.2-dB CM-CM gain and 11.7 times SR boosting. The measured noise efficiency factor (NEF) is 2.30, almost 1.49 times overperforming previous works.

肖知明

南开大学

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #6.4 / 11:45-12:10

肖知明本科毕业于华中科技大学，博士毕业于美国佛罗里达大学，在美国凌特科技（ADI）从事模拟芯片设计 8 年，现任南开大学电子信息与光学工程学院教授，主要从事低功耗模拟集成电路、数模混合芯片的设计与研究工作。获国家入选国家青年人才计划、南开大学百名青年学科带头人计划支持。以第一或通信作者身份发表 ISSCC、VLSI、CICC、JSSC、TCAS-I&II、TPE、TIE 等学术论文 43 篇，获已授权国家发明专利 26 项，版图专著 12 项。2021 年创立上海芯享程半导体有限公司，专注高精度信号链芯片、低静态功耗电源管理芯片的产业化，目前已量产 4 颗车规级，8 颗工规级芯片。

TALK

A 64-Channel Inverter-Based Neural Signal Recording Amplifier With a Novel Differential-Like OTA Achieving an NEF of 0.84

This article presents an inverter-based multichannel low-power low-noise neural signal recording amplifier with a novel differential-like operational transconductance amplifier (OTA). The differential-like OTA consists of two asymmetric branches. The inverting branch used for multichannel inputs has more inverters in parallel than that of the noninverting branch used for reference. Two virtual rails with very low impedance are designed in the differential-like OTA to effectively reduce the noise-efficiency-factor (NEF) and crosstalk in input channels. The NEF and the effective average current per channel decreases as the number of channels increases. Furthermore, by optimizing the current ratio of the inverting and the noninverting branches of the OTA, the NEF of the proposed amplifier is minimized and approaches the NEF of an ideal inverter of $\sqrt{2}/2$ as the channel counts increase to infinity. The area per channel is reduced even more significantly as the channel counts increase. The proposed amplifier architecture with 4-channel, 16-channel, and 64-channel configurations were fabricated and measured. The results show that the noise, power, and area performance were all improved by integrating more channels in parallel. For the 64-channel amplifier, the measured NEF is 0.84, the effective average current per channel is 422 nA and the area per channel is only 0.044 mm2.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #7.1 / 10:30-10:55

张钊

中国科学院半导体研究所

张钊，男，博士，中国科学院半导体研究所研究员，博士生导师。2022 年国家自然科学基金“优秀青年科学基金”获得者，2022 年入选中国科学院高层次人才引进计划。研究工作围绕高性能锁相环和时钟生成器、高速高能效光通信/有线通信收发器等高速高频集成电路设计技术的难点展开。近五年在相关领域共发表学术论文 50 余篇，包括 JSSC, ISSCC, VLSI 十余篇。主持多项国自然、北京市科技计划、知名企业横向等项目。担任知名 SCI 期《Electronics Letters》的编委。

TALK

Design of Low-voltage low-jitter PLL: From Integer-N to Fractional-N

In this talk, we will first discuss the key design considerations and techniques to design low-voltage low-jitter PLL. Then, give a breif review about our design of integer-N low-voltage PLLs. Based on these techniques in the integer-N design, we will introduce our latest research results about "A 0.65V-VDD 10.4-to-11.8GHz Fractional-N Sampling PLL Achieving 73.8fsrms Jitter, -271.5dB FoMN, and -61dBc In-band Fractional Spur in 40nm CMOS", which have been published in ISSCC 2025.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #7.2 / 10:55-11:20

王政

电子科技大学

王政，电子科技大学教授。长期从事硅基射频、毫米波、太赫兹集成电路的理论及设计研究，在硅基毫米波、太赫兹集成电路领域取得了一系列国际领先的、原创性的研究成果，在集成电路设计领域顶尖会议 IEEE ISSCC 和期刊 IEEE JSSC 上发表了多篇论文。研究成果包括设计并实现了 210GHz 基于基频的全集成 CMOS 收发机系统、超低抖动毫米波频率综合器芯片等。

TALK

Low Phase Noise Low Fractional-N Spur Frequency Synthesizer Techniques

With the increasing demand for transmission rate and modulation order in communication systems, achieving lower phase noise and jitter performance has become an urgent bottleneck in the field of frequency source that needs to be overcome. In 5G communication, the output signal jitter requirement of the frequency synthesizer is less than 100fs, and the frequency synthesizer will face more stringent jitter and spur performance requirements in future high-speed communication systems. This talk presents innovative circuit technologies to face the challenges of current frequency synthesizers in terms of phase noise, fractional spur, etc. It introduces the latest progress and circuit techniques of silicon-based fractional-N frequency synthesizers.

罗登

国防科技大学

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

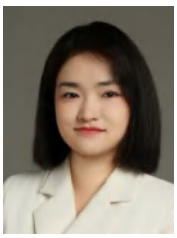
Talk #7.3 / 11:20-11:45

国防科技大学计算机学院助理研究员。主要研究方向为抗辐照数模混合集成电路设计，包括抗辐照高速数模/模数转换器、抗辐照高性能锁相环以及高速串行接口电路等。同时对面向生物医疗应用的低功耗集成电路设计感兴趣，主要包括低功耗神经信号采集器与刺激器的设计。

TALK

Design of an All-Digital Fractional Output Divider Using Split-DTC-Based Background Calibration

In modern system-on-chips (SoCs), compact, low-jitter and low-power on-chip clock generators are essential for delivering multiple output frequencies to various modules, including microprocessors, IO interfaces, and power-management systems. Conventional clock generators using multiple phase-locked loops (PLLs) often face challenges such as high-power consumption and increased chip area. In contrast, employing multiple fractional output dividers (FODs) driven by a single PLL provides a more compact and power-efficient alternative. FODs can be implemented using either digital-to-time converters (DTCs) or digital-to-phase converters (DPCs). Among these, DTC-based FODs are commonly adopted due to their superior power efficiency and reduced area requirements. However, DTC-based FODs are prone to variations in process, voltage, and temperature (PVT), and any gain error or integral nonlinearity (INL) in the DTC can significantly degrade jitter performance. To calibrate the gain and INL of the DTC, a reference clock is required to detect these errors. Previous methods have utilized additional delay-complementary DTCs or pulse-to-voltage converters to generate reference clock for DTC gain calibration. However, these techniques often neglect DTC INL, achieving only limited spur performance. Although the background gain and INL calibration based on an auxiliary PLL can reduce the spurs effectively, the additional PLL increases the chip area and circuit complexity significantly. This paper presents an FOD using split-DTC-based background calibration for both DTC gain and INL, achieving 257fs worst-case integrated jitter and less than −77dBc spurious tones. Owing to the split-DTC-based background calibration, all circuits are designed with standard cells except for the DTCs, making it possible to greatly reduce the area with advanced processes.



2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #7.4 / 11:45-12:10

钱慧珍

西安电子科技大学

钱慧珍，西安电子科技大学集成电路学部教授、博导。任 IEEE MTT 学会微波/毫米波集成电路技术委员会成员，IEEE 高级会员，中国电子学会高级会员。发表论文 80 余篇，其中集成电路旗舰期刊、集成电路“奥林匹克会议”IEEE ISSCC 十余篇，授权发明专利 40 件。获国家优秀青年基金，中国首位 IEEE MTT 学会杰出博士生奖，最佳论文奖等其他 IEEE 奖项十多项。长期研究微波/毫米波/太赫兹集成电路，数字密集型射频集成电路，片上相控阵无线传输系统，可重构无源电路等。

TALK

Linearization Techniques for RFDACs

To meet the increasing requirements of wireless communications with large data-rate, transmitters with high linearity and low distortion are dramatically demanded. The nonlinearity of RFDACs comes from impedance variation versus code/frequency, LO leakage, PVT variation, I/Q mismatch, non-ideal high data-rate baseband signals, memory effect, etc. Various linearization techniques for RFDACs including DPD, open-loop linearization technique with invariant impedance and scalable LO leakage, on-chip self-calibration, etc. will be compared and discussed. Two design examples, a 21-31GHz DPD-less quadrature RFDAC for 4096QAM and a self-calibration SCPA for 1024-QAM will be introduced in detail.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #8.1 / 13:30-13:55

钟龙杰

西安电子科技大学

钟龙杰(1991)，西安电子科技大学集成电路学院副教授，国家级青年人才，隶属朱樟明教授团队。承担项目：头部企业(SL)高精度加速度计与陀螺仪开发、头部企业(HW)低噪声高精度传感器前端放大器、国自然面上/青年高性能 MEMS 加速度计模拟前端、浙江省科技厅"尖兵""领雁" 子课题面向高精度激光雷达 MEMS 振镜技术等。工作/教育经历：西安电子科技大学微电子学院专任教师(2021-今)、东南大学电子科学与工程学/微电子学院专任教师(2019-2020)、西安电子科技大学博士(2013-2019)、新加坡南洋理工大学公派联培(2017-2018)、西安电子科技大学本科(2008-2012)。学术任职：IEICE Electronics Express (AE)。研究简介：围绕 MEMS AFE 展开研究。授权国家发明专利 5 项(转换 1 项)，相关技术在士兰微获得应用，华为优秀结项。所研制MEMS加速计芯片于2018/2020/2023年发表JSSC三次，以一作/通信身份发表IEEE JSSC/TCASI/VLSI/CICC 等论文 10 余篇。受邀担任 IEEE JSSC/TCSAI/TVLSI/ IoT/TAES/JSENS 等期刊审稿人。

TALK

A 3-Axis MEMS Gyroscope with 2.8ms Wake-Up Time Enabled by a 1.5μW Always-On Drive Loop

A low always-on current (847nA), fast start-up time (2.8ms), Always-on MEMS Gyroscope achieves ±5% start-up time stability Over −40 to +85 °C temperature rang is presented. The instability problem in the always-on mode due to parasitic relaxation oscillation (PRO) effect triggered by temperature variation is solved by using the duty-cycle automatic optimization (DAO) technique. Compared to state-of-the-art, this work solves the instability problem and further reduces the start-up time by 1.9X.

张雅聪

北京大学

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #8.2 / 13:55-14:20

张雅聪，北京大学集成电路学院副研究员，硕士生导师。2003 年在天津大学电子科学与技术专业获得工学学士学位，2008 年在北京大学微电子学与固体电子学专业获得理学博士学位，2008 年 7 月至 2011 年 2 月在北京大学信息科学技术学院做博士后研究。主要研究方向为模拟/混合信号集成电路设计，特别是低噪声/低功耗探测器接口芯片研究，如辐射探测器前端电路芯片、电信号采集与电刺激芯片、红外焦平面阵列读出电路芯片等。在 JSSC、TCAS、ISSCC、ISCAS 等国际期刊和会议上发表学术论文 50 余篇，已授权专利 10 余项，多款芯片得到工程化应用，曾于 2017 年获教育部科技进步一等奖（排名 3/10）。

TALK

A High-Voltage-Compliant 86% Peak Efficiency Current-Mode Stimulator With Dynamic Voltage Supply for Implantable Medical Devices

This work introduces a high-voltage (HV) compliant, energy-efficient current-mode stimulator featuring a proposed boost-based dynamic voltage supply (DVS) to minimize the voltage dropout. The stimulator employs an activate-on-demand asynchronous strategy, instructing the boost converter to generate the dynamically increased high voltage that tracks the electrode's voltage drop, thus achieving a near-adiabatic stimulation. The strategy relies on measuring the boost's varying voltage conversion ratio (VCR), which is facilitated by an 8-bit voltage ratio quantizer (VRQ) proposed in this article. Furthermore, the boost converter employs a low-power, fast-speed, HV gate driver (HVGD) to control its p-type power switch that connects the inductor to the HV output. This article also presents a dedicated digital circuit that generates the pulse signals for controlling the n-type power switch and the HVGD. This digital circuit is driven by a five-phase clock from a current-starved ring oscillator. A highly efficient rotationally symmetric level shifter is utilized for the ring oscillator's output, translating its level and improving its rise/fall time. The boost converter reaches a peak efficiency of 90.2%, enabling the stimulator to achieve an end-to-end energy efficiency of up to 86% during a biphasic stimulation of 6 mA. The stimulator IC, fabricated using 0.18-μm bipolar–CMOS–DMOS (BCD) technology, occupies a compact area of 2.16 mm2. It exhibits low static power consumption at 1.78 μW, promising battery-powered implants with an extended lifetime and a reduced form factor.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #8.3 / 14:20-14:45

陈虹

清华大学

陈虹，清华大学集成电路学院，教授，博导，IEEE 高级会员，IEEE 异步电路国际会议（ASYNC）2023 年大会主席，IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) 副主编，Tsinghua Science and Technology 客座主编。研究方向为极低功耗电路与系统设计，包括异步电路设计、亚阈电路设计、异步脉冲神经网络加速器等，部分成果已产业化。拥有发明专利 32 项，发表国内外期刊及国际会议论文 130 余篇，3 本学术专著。荣获 2013 年 IEEE ISCAS 最佳演示奖，IEEE ASYNC2021 和 ASYNC2023 最佳论文提名。2016 年国家级教学成果奖二等奖，2017 中国电子学会科学技术奖二等奖，2019 年北京医学科技进步三等奖，2020 年中华医学科技进步三等奖，2020 年北京市科技进步一等奖，2023 年国家科技进步二等奖。2018、2019 国际大学生类脑计算大赛优秀指导教师等。

TALK

ANP-O: A 67μW/Channel, 0.13nW/Synapse/Bit Nose-on-a-Chip for Non-invasive Diagnosis of Diseases with On-chip Incremental Learning

Portable electronic noses (E-noses) are proposed to detect possible pathological changes in the body by analyzing the patient's exhaled gas. However, the composition of exhaled gas varies greatly depending on the environment with changing conditions and patients using different devices in different locations, which makes the E-nose difficult to maintain a satisfying accuracy in detecting diseases for different patients. Besides, the overall power consumption issue poses a great challenge for power-constrained portable E-noses. To overcome these challenges, we introduce ANP-O: a 67 μ W/Channel 0.13nW/Synapse/Bit E-nose system including a 16-channel gas sensor array, 16 ADC-free analog front-end circuits, and an asynchronous olfactory processor. ANP-O has three key features: 1) On-chip incremental learning enables retraining the network rapidly and locally to overcome accuracy degradation. 2) An ADC-free front-end circuit improves system response by minimizing conversion latency and enhances power efficiency through direct analog signal processing. 3) Event-driven asynchronous logic effectively decreases the switching power brought by a global clock. The proposed E-nose obtains 98.23%,98.0% and 97.7% for 9-class flammable and toxic gases (FTs) with few-shot learning, 10-class volatile organic compound gases (VOCs) with one-shot incremental learning, and 2-class diagnosis of lung cancer patients with batch learning, respectively.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #8.4 / 14:45-15:10

陈铭易

上海交通大学

陈铭易，博士，欧洲微电子研究中心(IMEC)博士后，现任上海交通大学电子信息与电气工程学院长聘教轨副教授，博士生导师，IEEE 高级会员，中国电子学会会员。长期从事高性能模拟与混合信号集成电路的设计研究，重点研究领域包括精密传感接口芯片、超高分辨率模数转换器芯片、微能量采集和电源管理芯片等。近三年先后主持国家自然科学基金面上项目、十四五国家重点研发计划课题、上海市浦江人才、企业委托开发等项目 9 项。作为核心技术负责人，完成国内首款面向非侵入式脑机接口的八通道 24 位模数转换器芯片的自主研发，在 IEEE JSSC、SSC-L、TIE、TBCAS、TCAS-II、VLSI Symposium 等国际期刊和会议发表论文 50 余篇，申请发明专利 20 项，美国发明专利 1 项。研究成果获欧盟委员会颁发的 “玛丽-居里”卓越奖。在工业界一线从事芯片设计的九年期间，研发了数十款用于消费电子和无线通信领域的数模混合信号芯片，其中多款芯片成功实现量产。

TALK

A 26-G Input-Impedance 112-dB Dynamic-Range Two-Step Direct-Conversion Front-End With Improved 1-Modulation for Wearable Biopotential Acquisition

We presents a high dynamic range (DR) direct conversion front-end (Direct-FE) IC enabling the wearable acquisition of weak bio-potentials superposed onto large motion artifacts (MAs). The prototype IC has been fabricated in a standard 0.18-μm CMOS process. Beneffting from the proposed feedback (FB) two-step direct conversion architecture with an improved 1-modulation, as well as a novel differential difference ampliffer (DDA) and a dynamic-element-matching (DEM) technique, it achieves a peak input range of 3.56 VPP, an inputreferred noise (IRN) of 2.2 μVrms, an input impedance of 26 G, and a ±1.8-V electrode dc offset (EDO) tolerance, while consuming only 63-μW power. Compared with state-of-the-art DirectFEs, the proposed work demonstrates an advanced DR (112 dB) and a competitive FOMDR (175 dB). The prototype IC has been validated based on in vivo experiments, demonstrating its capability for artifact-tolerant wearable bio-potential acquisition.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #9.1 / 13:30-13:55

罗文基

澳门大学

罗文基教授，于 2006、2011 年分别获得香港科技大学计算机工程学士学位和电子与计算机工程博士学位。他曾于 2011 年以客座助理教授任职于香港科技大学，目前是澳门大学模拟与混合信号超大规模集成电路国家重点实验室和科技学院的副教授。主要研究领域包含用于无线通信及生物医学应用的超低功耗感应电路和集成能量采集技术的开发。罗文基教授持有 9 项中国、美国专利，并发表国际论文 100 余篇。
罗教授是 IEEE 国际固态电路会议（ISSCC）的技术委员会成员，共同获得包括 2013 年优质电子设计亚洲研讨会（ASQED）最佳论文奖，2015 年亚洲固态电路会议（A-SSCC）杰出设计奖，和 2016 年亚洲及南太平洋设计自动化会议（ASPDAC）最佳设计奖。罗教授现正担任 IEEE 生物医学电路与系统和 IEEE 感官系统的技术委员会成员，并曾出任 IEEE 电路与系统学会及固态电路学会杰出讲师，ISSCC 技術委员会成员及 ISSCC 2024 遠東區主席。

TALK

A 91.25% Peak Power-Conversion-Efficiency Capacitive Power Management IC Supporting up to 5.68mJ Burst Energy Delivery Using a Single External Capacitor for mm-Scale IoT Applications

We present a power management system designed to address the challenge of burst power consumption in miniaturized IoT devices, where peak power demands can escalate to the mW level despite average system power being in the sub-μW range. Existing mm-scale solid-state batteries struggle with high internal resistance, limiting their load-driving capability. To overcome this, the proposed system employs a single external storage capacitor (CSTO) charged to a high voltage (HV) and an on-chip step-up/down switched-capacitor (SC) converter to efficiently deliver burst energy. The system integrates a 2:1 SC and a continuously scalable conversion ratio (CSCR) SC stage to maximizes energy extraction efficiency (EEE). Fabricated in a 180nm BCD process, the IC occupies an active area of 4.62mm^2 and achieves a peak power conversion efficiency (PCE) of 91.25%. With a 22μF MLCC, the system delivers 146μJ of burst energy, achieving a peak EEE of 70.9%. By using a 220μF tantalum capacitor, the burst energy can be further increased to 5.68mJ with an EEE of 69.8%. The proposed system significantly improves EEE and burst energy delivery compared to prior work, making it highly suitable for energy-constrained IoT applications.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #9.2 / 13:55-14:20

郭建平

中山大学

郭建平博士，中山大学电子与信息工程学院（微电子学院）教授、微电子科学与工程教研室主任、IEEE 固态电路学会广州分会主席、广东省集成电路工程技术研究中心副主任。主要从事模拟与数模混合集成电路的研究与设计，研究方向为电源管理及激光雷达芯片。

在集成电路设计方向发表学术论文 100 余篇，含多篇集成电路设计顶级期刊/会议（JSSC/ISSCC）论文。发表的 LDO 频率补偿技术广泛应用于国内头部芯片公司产品中，发表的全集成 FVF-LDO 论文单篇被引超过 400 次（谷歌学术），为近十年来被引最高的 LDO 芯片论文之一。主持研发了十余款商用量产芯片，其中部分电源管理芯片已应用于国内知名通信厂商。授权中国发明专利 40 项，其中 20 余项已成功实施转让，激光雷达芯片实现了产业化应用。

郭建平教授指导了众多学生开展大创及竞赛等学科实践活动，指导的学生在 2020-2022 年连续三年获得集创赛模拟 IC 赛道全国一等奖，2023-2024 连续两年获得 IEEE ICTA 最佳论文奖。指导多名学生在本科阶段完成了芯片流片，并在 IC 设计领域旗舰期刊或会议发表多篇学术论文。

TALK

Design of DC-DC Regulators with Low Quiescent Current and High Power Efficiency for Battery Powered IoT Devices

Two DC-DC regulators with low quiescent current and high power efficiency for internet of thing (IoT) applications will be introduced. An ultra-low quiescent current dual-mode DC-DC buck converter will be firstly presented. Based on the compensator in the valley-current mode, a built-in mode tracking technology is proposed to achieve the predictable and seamless mode transition without load current sensing circuits. Implemented in a 0.18-μm BCD technology, the proposed converter achieves 144-nA quiescent current and has an efficiency higher than 90% over 10-μA to 500-mA loading range within the supply range of a single lithium-ion battery. Then we will present a low-power single-inductor multiple-output (SIMO) DC-DC converter. An asynchronous balanced power-distributive control (BPDC) is proposed to reduce the delay charging period of the channels to mitigate the cross regulation. Implemented in a 0.18-μm BCD technology, the proposed SIMO converter achieves a quiescent current of 1.2 μA and a peak efficiency of 91.8%. Moreover, the cross regulation has minimized to be 0.04 mV/mA when the load currents of other channels change simultaneously.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #9.3 / 14:20-14:45

刘阳

西安电子科技大学

刘阳，西安电子科技大学华山特聘教授，入选国家级青年人才计划，杭州市海外引才计划。于 2023 年在香港科技大学获得博士学位。2023 年至 2024 年，在香港科技大学从事博士后研究员工作，2025 年加入西安电子科技大学杭州研究院，担任华山特聘教授。已发表 IEEE 期刊及会议论文 13 篇，包含 JSSC 两篇、CICC 一篇。曾被提名 CICC 最佳论文奖。主要研究方向为电源管理芯片，包括隔离电源、隔离驱动、无线充电等。

TALK

Pseudo Hysteretic Controlled Gap Time Modulated Isolated DC-DC Converter With Common-Mode Transient Immunity

A pseudo hysteretic controlled gap time modulated isolated DC-DC converter is presented. A pseudo hysteretic controller is designed to bound the output voltage with fast load transient and small output voltage ripple, and implement gap time modulation based on the load current, and gap time modulation is used to adjust the power delivered by a Class-D power amplifier with high efficiency. A high impedance load shift keying (LSK) scheme is also proposed with common-mode transient immunity (CMTI) to complete the global feedback loop without requiring an additional transformer or capacitor. The prototype is implemented in a standard 65nm CMOS technology. With an input voltage of 2.5V, the proposed converter generates an isolated output voltage that ranges from 1.8V to 2.2V with a peak efficiency of 73.3% and an output voltage ripple of only 20mV. With a load current transient step of 40mA to 150mA, this converter demonstrates unobservable overshoot and undershoot. CMTI is demonstrated with common-mode transients that measure +8kV/□s and –12kV/μs.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #9.4 / 14:45-15:10

赵广澍

澳门大学

赵广澍，澳门大学博士后研究员，分别于 2014 年，2018 年，2024 年在南开大学,南安普顿大学以及澳门大学获得学士，硕士和博士学位。共计发表论文 14 篇，以第一/共一作者身份发表 JSSC, TCAS-I,TCAS-II 等文章，获 2024 年 CICC 最佳学生论文奖提名。任 IEEE TCAS-I/II, IET RPG, Integration, Microelectronics, IEEE ISCAS 等期刊/会议审稿人。目前的主要研究方向为压电能量收集系统以及低功耗模拟电路设计。

TALK

High-Efficiency Ultrasound Energy Harvesting Interface with Auto-Calibrated Timing Control from -25 °C to 85 °C

This work presents a high-efficiency ultrasound energy harvesting interface with auto-calibrated timing control, featuring: 1) the proposed CP auto-calibration, consisting of the half bias-flip time detection and adaptive closed-loop time calibration (ACTC) to improve the system's robustness against piezoelectric transducer (PZT) materials and environmental variations; 2) the proposed charge recycling bootstrapping driver to reduce conduction loss and improve the CP autocalibration accuracy as well as the peak voltage flipping efficiency; and 3) the proposed coarse detection and fine calibration technique to eliminate the inherent timing offset and increase the acceptable input excitation frequency range. The fabricated chip prototype in 0.18-μm silicon on insulator (SOI) CMOS process can adapt to both PZT5A (nominal CP ~ 114 pF) and PZT5H (nominal CP ~ 190 pF) and is capable of operating over a wide temperature range from −25 ◦C to 85 ◦C. With the proposed coarse detection and fine calibration technique, this work demonstrates a high measured peak power conversion efficiency of 94.5%, corresponding to a ~23% improvement when compared with the prior ultrasound energy harvesting interface while achieving a favorable figure of merit (FoM) of 8.13×.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #9.5 / 15:10-15:35

路延

清华大学

路延，清华大学长聘教授、兴华讲席教授，国家高层次海外引进人才，国家优青（港澳），博士生导师。分别于 2006 和 2009 年获华南理工大学微电子学士和硕士学位，2013 年博士毕业于香港科技大学电子与计算机工程系。2014 至 2024 年就职于澳门大学微电子国家重点实验室；2024 年 7 月 1 日加入清华大学电子工程系。主要研究方向包括电源管理芯片设计、无线能量传输电路与系统等。发表学术论文近 200 篇，其中 IC 设计领域顶尖论文 ISSCC+JSSC 共 28+33 篇。曾获 2013-14 届 IEEE 固态电路协会博士生成果奖、IEEE 电路与系统协会 2017 杰出青年作者奖、ISSCC 2017 菅野卓雄远东最佳论文奖。曾任 JSSC、TCAS-I 和 TCAS-II 客座编辑、ISSCC 技术委员、CICC 电源分会主席、IEEE SSCS 杰出讲师。现任 IEEE JEDS 副编辑及《半导体学报》方向 2-集成电路设计与应用-副主编。

TALK

A Bi-Directional Dual-Path Boost-48V-Buck Hybrid Converter for HV Power Transmission in Light-Weight Humanoid Robots

Humanoid robots have high potential to replace human labors for various tasks in the near future. Thick and heavy cables in humanoid robots account for a certain portion of the total weight. This talk presents a bidirectional dual-path boost-buck converter reusing the parasitic cable inductor for 48V-bus power delivery, to reduce the system weight. Also, the proposed phase alignment scheme greatly reduces the cable current ripple in such high-voltage conversion case. We achieve a peak chip efficiency of 96.7% at 16.5W output, and a maximum transmission power of 45W.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #10.1 / 13:30-13:55

刘勇攀

清华大学

刘勇攀，博士，清华大学电子工程系长聘教授，教育部长江学者，电路与系统研究所所长，北京信息科学与技术国家研究中心超感知创新团队。研究兴趣包括领域通用计算、感存算一体化芯片与系统技术。基于“器件-架构-算法”跨层次协同优化路线，研制了系列人工智能加速器、非易失处理器等高能效计算芯片。在 ISSCC、JSSC 等集成电路设计杂志及会议上发表了 300 余篇论文。担任 ISSCC、CICC、ASSCC 等国际会议的技术委员会委员，ICAC 技术委员会主席等，主持自然科学基金重点，国家重点研发计划等重点项目 10 余项。担任 ASSCC、AICAS 会议 Tutorial Speaker 和 IEEE CASS Distinguished Lecturer，曾获首届 DAC 会议 40 岁以下发明创新奖，教育部技术发明一等奖等。

TALK

3DGS 生成式感知芯片关键技术

3D rendering plays a crucial role in emerging applications like virtual reality and embodied AI. Unlike traditional Neural Radiance Fields (NeRF) method, the novel 3D Gaussian Splatting approach (3DGS) circumvents NeRF's frequent sampling and intensive network inference. However, the variability in Gaussian distribution shapes poses significant challenges on resource-constrained edge devices, due to more kinds of operators and higher bitwidth requirements than NeRF. This work presents a shape-aware 3D GS processor. The architecture can reduce computational and memory access overhead through online shape analysis.

Key features include: 1) A shape-aware reconfigurable computation architecture supporting hybrid rasterizing and interpolating. 2) An online Shape-aware Early Skipping Controller (SESC) that employs hardware-friendly shape analysis to omit input-dependent ineffective computations. 3) A cache-based Gaussian management utilizing shape-aware Z-order spatial scheduling and SH-reused temporal scheduling. Finally, the future applications of such generative sensing techniques are discussed.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #10.2 / 13:55-14:20

刘雷波

清华大学

刘雷波，清华大学集成电路学院长聘教授、博士生导师，教育部国家重大人才计划特聘教授，国家级一流本科课程负责人。

1999 年和 2004 年分别在清华电子工程系和微电子所获得学士和博士学位。2004 年留在清华微电子所任教，2006 年~2017 年分别在欧洲微电子中心、麻省理工学院、林肯大学、牛津大学进修与访问。长期从事软件定义芯片、硬件安全和密码芯片、VLSI 数字信号处理等研究工作。发表高水平论文 300 余篇、授权发明专利 150 余项（美国专利 20 余项）、撰写著作 9 部、参与制定国家标准 1 项。担任国际权威期刊《IEEE Circuits and Systems Magazine》副主编、中国工程院院刊《信息与电子工程前沿》执行副主编；密码硬件顶级会议 CHES、集成电路设计顶级会议 ISSCC、体系结构顶级会议 ISCA，及电子设计自动化顶级会议 DAC 的 TPC 委员，集成电路设计一流会议 A-SSCC 的 TPC 委员和大会主席等；中国密码学会密码芯片专委会副主任委员。关键技术在一系列国家重大工程中取得批量应用。获国家技术发明二等奖、中国专利金奖、教育部技术发明一等奖、中国电子学会技术发明一等奖、世界互联网大会 15 项世界互联网领先科技成果等奖励。主持 3 门课，获首批国家级一流本科课程、清华大学本科生精品课、北京市青年教师教学竞赛一等奖、清华大学青年教师教学竞赛一等奖、清华大学青年教师教学优胜奖、MOOC 教学先锋奖等多个教学奖励，所负责的大规模网络开放课程（MOOC）入选首批教育部高校在线教学国际平台，并获得清华大学“良师益友”称号。

TALK

A 28nm 4.05μJ/Encryption 8.72kHMul/s Reconfigurable Multi-Scheme Fully Homomorphic Encryption Processor for Encrypted Client-Server Computing

A 28nm reconfigurable multi-scheme FHE processor is proposed to provide unified support on both client and server for encrypted computing. Reconfigurable PE array, parallel execution strategy with memory access optimizations, on-chip data generation, and cache-aware scheduling method are combined to enable energy-efficient execution of BGV/BFV/CKKS schemes. This 5.4 mm2 processor achieves 4.05 μJ/encryption at 0.7V for client-side operations and 20.92 kHMul/s at 1.0V for server-side evaluations.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #10.3 / 14:20-14:45

焦海龙

北京大学深圳研究生院

焦海龙，博士，北京大学深圳研究生院长聘副教授，博士生导师。2012 年于香港科技大学获得电子及计算机工程学博士学位。2013 年 9 月加入荷兰埃因霍温理工大学电子工程系，任职 Tenure-track Assistant Professor，2016 年 9 月获得终身教职。2015 年 2 月起，兼任比利时鲁汶微电子中心（IMEC）三维集成部门访问研究员。2017 年 1 月全职加入北京大学深圳研究生院信息工程学院，任职副教授，2023 年 1 月升任长聘副教授。焦海龙博士的主要研究方向为低功耗超大规模集成电路设计，重点关注超低电压超低功耗电路设计、低功耗高能效存算一体芯片、低功耗高能效片上人工智能。已在相关领域发表国际期刊（如 IEEE JSSC、IoT Journal、TCAS-I、TCSVT、JBHI）及国际会议（如 ISSCC、DAC、ICCAD、ASSCC）论文 100 余篇。

TALK

Nebula: A 28nm 109.8TOPS/W 3D PNN Accelerator Featuring Adaptive Partition, Multi-Skipping, and Block-Wise Aggregation

A 28-nm on-chip accelerator, Nebula, is developed for 3D point cloud analysis. Tree-based adaptive partitioning sampling, sampling-based multi-skipping, and block-wise delayed-aggregation are proposed to reduce sampling latency, skip redundant operations, and reduce external memory access, respectively. Evaluated with the state-of-the-art benchmarks, Nebula achieves up to 109.8 TOPS/W energy efficiency (@20 MHz), 5.6 TOPS/mm2 area efficiency (@200 MHz), and 5263.2 fps frame rate (@200 MHz).

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #10.4 / 14:45-15:10

涂锋斌

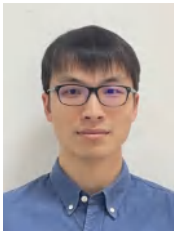
香港科技大学

涂锋斌博士，香港科技大学电子及计算机工程学系助理教授，国家优秀青年科学基金获得者。涂博士于 2019 年在清华大学微纳电子系获得博士学位，同年获北京市优秀毕业生及清华大学优秀博士学位论文奖。他于 2019~2022 年在加州大学圣塔芭芭拉分校 SEAL Lab 担任博士后研究员，2022~2023 年在香港智能晶片与系统研发中心（ACCESS）担任博士后研究员。他的研究方向包括存算一体架构和 AI 芯片设计。他设计的 AI 芯片 ReDCIM 和 Thinker 分别荣获 2023 年度中国半导体十大研究进展和 2017 年国际低功耗电子与设计会议 ISLPED 设计竞赛奖。他获得 2024 年世界人工智能大会 WAIC·云帆奖“璀璨明星”。已出版《神经网络加速器的计算架构及存储优化技术研究》《人工智能芯片设计》专著 2 部。已发表 60 余篇学术论文，包括 ISSCC、JSSC、DAC、ISCA、MICRO 等集成电路和体系结构领域权威期刊和学术会议。

TALK

A 28nm 0.22μJ/Token Memory-Compute-Intensity-Aware CNN-Transformer Accelerator with Hybrid-Attention-Based Layer-Fusion and Cascaded Pruning for Semantic-Segmentation

Hybrid models integrating CNN and Transformer (ConvFormer) have achieved significant advancements in semantic segmentation tasks, which are critical for autonomous driving and embodied AI. CNN enhances the multi-scale feature extraction ability of the Transformer to achieve pixel-level classification, but the large token length demand (>16K) of semantic segmentation incurs significant computation and memory overheads. In this work, we design a ConvFormer accelerator with a hybrid attention mechanism and a KV-weight-reused scheduler to minimize external memory access. Additionally, we introduce a cascaded feature map pruning strategy to reduce 91.10% computation in segmentation heads. Our chip achieves 52.9TOPS/W energy efficiency and 0.22μJ/token energy consumption, obtaining 3.86-10.91× system-level energy reduction over the SOTA Transformer accelerators. This is the first AI chip ISSCC paper from Hong Kong, with support by ACCESS (AI Chip Center for Emerging Smart Systems, sponsored by InnoHK funding).



2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #10.5 / 15:10-15:35

朱浩哲

复旦大学

朱浩哲，复旦大学芯片与前沿技术研究院助理研究员/博士后。他在 2017 年、2022 年于复旦大学微电子学院分别取得学士和博士学位。他的研究方向包括存算一体芯粒与集成芯片系统、高能效存算一体电路、具身智能领域专用处理芯片等。他以第一或通讯作者在 ISSCC、JSSC、MICRO、A-SSCC、HPCA 等本领域高水平期刊或会议上发表论文，研究成果曾获 A-SSCC 2024 Distinguished Design Award 等奖项。

TALK

SLAM-CIM: A Visual SLAM Backend Processor With Dynamic-Range-Driven-Skipping Linear-Solving FP-CIM Macros

Simultaneous Localization and Mapping (SLAM), a pivotal technology in robotics, autonomous vehicles, and surveillance, has gained prominence with the emergence of edge intelligence. Developing energy-efficient, low-latency SLAM systems is essential due to resource constraints and real-time demands. Compute-in-memory (CIM) architectures have been proven to be efficient for matrix multiplications. However, applications for SLAM raise new challenges in memory access and computation aspects: the linear system solving requires row transformation and causes frequent CIM updates, while the backend optimization causes redundant memory access; Backend optimization dominates SLAM's computation and requires high precision and high dynamic range. Thus, we propose SLAM-CIM, a visual SLAM backend processor for edge robotics. A dynamic-range-driven-skipping CIM macro is designed to realize energy-efficient FP-MAC operations. A preconditional-conjugate-gradient-based in-memory linear solver is designed to achieve linear system solving without additional row transformations. This reduces memory access by 2.08× and linear-system-solving latency by 3.84×. SLAM-CIM further minimizes CIM weight updates through incremental bundle adjustment, increasing average CIM utilization by 2.8×. A silicon prototype is fabricated using 28-nm CMOS technology. The measurements show that SLAM-CIM achieves accurate and efficient SLAM operations with an average energy efficiency of 31.53 TFLOPS/W.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #11.1 / 15:50-16:15

潘权

南方科技大学

南方科技大学长聘教授，入选国家级高层次人才计划，国家级青年人才计划。2005 年毕业于中国科学技术大学电子科学与技术系，获理学学士学位；2014 年毕业于香港科技大学电子及计算机工程学系，获哲学博士学位。主要研究工作集中在高速模拟/射频集成电路设计，主要包括：高速有线通信集成电路、光通信集成电路和硅光互连研究。作为负责人不仅在国际主流会议/期刊上发表 80 多篇高水平学术论文，同时有超过 8 年丰富的国内外工作经验，包括 4 年硅谷业界最前沿的工作经验。曾获得 IEEE 电路系统协会杰出青年作者奖，南方科技大学校长青年科研奖、优秀教学奖和优秀书院导师奖。

TALK

High-Speed SerDes and Optical Communications: Equalizations and Modulations

High-speed SerDes and Optical Circuits have become extremely attractive since they are extensively adopted in high-speed communications, such as local area networks, board-to-board, and data center-to-data centers. In this talk, the key techniques, including equalization, modulation, and crosstalk cancellation, are discussed and analyzed.

桂小琰

西安交通大学

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #11.2 / 16:15-16:40

桂小琰，教授，博士生导师，IEEE 高级会员。博士毕业于加州大学尔湾(UC Irvine)，2008-2012 年在 Broadcom 任设计工程师和主任科学家，现任西安交通大学微电子学院教授、博士生导师，主要研究领域为高速有线通信/光通信和无线通信集成电路设计。

在国际权威学术期刊和会议发表论文 60 余篇，授权中国发明专利 7 项，美国发明专利 1 项；在主要研究领域主持各类纵向和企业科研项目三十余项，获得国家级教学成果二等奖 1 项，陕西省高等教育教学成果特等奖 1 项，华为技术有限公司火花奖 1 项，陕西省高等学校科学技术研究优秀成果二等奖 1 项，2023 IEEE MTT-S IWS 最佳学生论文奖，2023 IEEE ICTA 最佳论文奖。

TALK

A Low-Latency 200Gb/s PAM-4 Heterogeneous Transceiver for Retimed Pluggable Optics

A low-latency solution for 200Gb/s pluggable optics is presented. The link includes a 200G transceiver with a 200Gb/s analog MUX/DEMUX in 130nm SiGe and a 100Gb/s mixed-signal transceiver in 28nm CMOS achieving BER of 1e-12 transferring PRBS7 at 200Gb/s.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #11.3 / 16:40-17:05

郑旭强

中国科学院微电子研究所

郑旭强，中科院微电子研究所研究员，长期从事高速串行接口 SerDes 的研究，当前核心工作集中在：（1）10~32 Gb/s 传统 NRZ 调制高速串行接口与 DIE2DIE 单端高速并行接口的应用研究；（2）56~112 Gb/s PAM4 调制高速串行接口的样品研制；（3）200+Gbps 幅度/相干调制高速 DSP 关键技术研究。主持科技部重点研发计划、自然科学基金、中科院重点部署及横向研发等项目。近年来在 JSSC、TCAS-I、TCAS-II、CICC、ESSCIR 等国际知名期刊和会议发表论文 50 余篇，授权专利 11 项。担任 JSSC、TCAS-I、TVLSI 等期刊的评审工作。

TALK

A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Injection-Locked Clock Multiplier Utilizing a Complementary-Injection Scheme and an Adaptive Pulsewidth Adjustment

This talk will present a ring voltage-controlled oscillator (RVCO)-based pulse-injection-locked clock multiplier (ILCM) with a complementary-injection scheme, an adaptive pulsewidth adjustment, and a hybrid frequency tracking loop (FTL). The developed complementary-injection scheme introduces a combination of traditional narrow-pulse injection and wide-pulse injection to achieve phase error cancellation and enhance noise suppression. Based on the derived optimal pulsewidth principle, the proposed adaptive pulsewidth adjustment technique automatically maintains the optimal noise suppression across process, voltage, and temperature (PVT) variations. To achieve enhanced in-band noise suppression and extend the locking range, a hybrid FTL that incorporates a conventional phase-locked loop (PLL), a developed timing-adjusted loop (TAL), and an automatic locking mechanism (ALM) is designed. Fabricated in a 28-nm CMOS process, the ILCM occupies an active area of 0.133 mm2. The measurement results show that it achieves 43.9-fs rms jitter and −59.1-dBc spur level. The calculated FoM is −255.5 dB, which outperforms other state-of-the-art works.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 1

Talk #11.4 / 17:05-17:30

许灏

复旦大学

许灏，复旦大学微电子学院青年研究员，加州大学洛杉矶分校（UCLA）电子与计算机工程博士学位，长期从事射频与混合信号集成电路设计研究，2017-2019 年于 Broadcom 参与开发基于 DSP 的高速有线收发机，2019-2021 年于 Apple 参与无线收发机，2021 年至今在复旦大学工作，发表 IEEE JSSC、ISSCC、TCAS-I 等高水平论文 40 余篇。

TALK

An 8-to-28GHz 8-Phase Clock Generator Using Dual-Feedback Ring Oscillator in 28nm CMOS

This work proposes an 8-phase 8-28GHz clock generator consisting of a dual-feedback ring oscillator injection locked by a delay locked loop. The dual-feedback ring oscillator decouples the feedback loop setting the frequency and the feedback loop locking the phases, thus significantly expanding the maximum operation frequency. Fabricated in a 28nm CMOS process, the 8-phase clock generator maintains the output jitter less than 40fs and the maximum phase error less than 3° across 8-28GHz.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #12.1 / 15:50-16:15

秦培

华南理工大学

Pei Qin received the B.Sc. degree in electronic science and technology from the University of Electronic Science and Technology of China, Chengdu, China, in 2010, and the Ph.D. degree in electronic engineering from the City University of Hong Kong, Hong Kong, in October 2016. From November 2016 to February 2022, she was a Senior IC Design Engineer with HiSilicon, focusing on all digital phase-locked loop (ADPLL) IC design. In March 2022, she joined South China University of Technology, Guangzhou, China, where she is currently an Associate Professor. She is working on the research areas of analog/RF front-end and phase-locked loop (PLL) integrated circuit design.

TALK

A Differential Series-Resonance CMOS VCO with Pole-Convergence Technique Achieving 202.1dBc/Hz FoMTA at 10MHz Offset

Voltage controlled oscillator with ultra-low phase noise is extensively pursued for various applications, such as high-speed wireless/wireline communications, high-speed AD/DAs, etc. In this paper, we present a differential series-resonance VCO topology with a pole-convergence technique. The proposed VCO achieves a PN@10MHz of -152.89dBc/Hz from 9.122GHz, a TR of 17.7% (7.65GHz to 9.135GHz), and a 190dBc/Hz and 202.13dBc/Hz peak FoM and FoMTA at 10MHz offset, and the core area is 0.39× 0.49mm2.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #12.2 / 16:15-16:40

吴亮

香港中文大学（深圳）

吴亮博士分别于 2004 年和 2007 年获得复旦大学的本科和硕士学位，并于 2012 年获得香港科技大学电子及计算机工程学系的博士学位。他于 2018 年加入香港中文大学（深圳）理工学院任职助理教授，于 2014 年 1 月起任粤港澳毫米波与太赫兹联合实验室联席主任。他的主要研究方向为毫米波与太赫兹信号源及射频收发机集成电路芯片等。

TALK

A 47.3-to-58.4GHz Differential Quasi-Class-E Colpitts Oscillator Achieving 198.8dBc/Hz FoMT

A mm-wave single-core VCO is reported. Instead of relying on harmonic extraction or multi-core coupling, the PN is significantly improved by Quasi-Class-E Colpitts oscillation based on a two-port resonator. It enables fundamental oscillation, waveform shaping for power efficiency enhancement, and PN suppression. The 40nm CMOS prototype measures an FTR of 47.3 to 58.4GHz (21.1%) and PN from −124.9 to −119.8 at 10MHz offset with 5.5 to 10.5 mW power consumed, achieving 198.8dBc/Hz peak FoMT.

舒一洋

电子科技大学

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #12.3 / 16:40-17:05

舒一洋，电子科技大学“百人计划”特聘研究员、博士生导师。研究方向为射频/微波/毫米波集成电路设计，主要研究宽频、高性能、高能效振荡器与频率源芯片。发表集成电路、微波领域期刊会议论文 40 余篇，成果入选 ISSCC2023、ISSCC2021 会议亮点论文。授权国内外专利 6 项。获 IEEE SSC-Society Predoctoral Achievement Award、IEEE MTT-Society Graduate Fellowship Award、IEEE RFIC 最佳学生论文奖、IEEE IWS 最佳学生论文奖等奖项。担任 IEEE JSSC、TCAS-I、SSCL 等期刊审稿人。

TALK

Class-G Impedance-Modulation Multi-Core Power Oscillator for High Pout and Power Back-Off Efficiency Enhancement

Power oscillator can directly generate the signal to the output with a high system efficiency. However, the peak output power and the efficiency at deep power back-off (PBO) are limited. In this report, the architecture of impedance-modulation multi-core power oscillator is proposed. The reconfigurable power-combining matching resonator is introduced and analyzed to obtain high efficiencies and low phase noise at peak and PBO states. Meanwhile, the output matching is investigated to maintain the high efficiency along with the tuning of oscillation frequency. To verify the mechanism, a dual-core power oscillator with Class-G supply switching is designed and fabricated in a 40-nm CMOS technology. The digitally controlled tail resistor array is used to tune the output power continuously. Measurements exhibit a 33% tuning range from 2.3 to 3.2 GHz. The peak output power is 10 dBm, while the efficiencies at 0-/3-/6-/9-dB PBOs are 39%, 37%, 33%, and 30%, respectively.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 2

Talk #12.4 / 17:05-17:30

黄同德

南京理工大学

黄同德，南京理工大学副教授，博士生导师。2013 年博士毕业于香港科技大学电子与计算机工程系，2014-2016 年瑞典查尔姆斯理工大学博士后、2017 年瑞典查尔姆斯理工大学 researcher 研究员，2017 年 7 月加入南京理工大学。主要研究雷达收发芯片、相控阵芯片与频率源芯片等，主持多项军委科技委重点项目、国防装备项目、国家自然科学基金项目、江苏省科技厅重点研发/前沿基础计划等，相关研究成果发表在 IEEE ISCC, CICC, ASSCC, IEEE Trans 与 Letters 等。

TALK

An 18.5-to-23.6GHz Quad-Core Class-F23 Oscillator Without 2nd/3rd Harmonic Tuning Achieving 193dBc/Hz Peak_x000b_ FoM and 140-to-250kHz 1/f3 PN Corner in 65nm CMOS

A low-phase-noise (-138.2dBc/Hz) and high FoM (193dBc/Hz) at 10MHz offset, low 1/f3 phase-noise corner (160kHz) quad-core class-F23 VCO (18.5-23.6GHz) without extra 2nd/3rd harmonic-tuning is presented. A circular trifilar transformer is proposed to extend the differential-mode resonance around the 3rd harmonic frequency, meanwhile achieving low inductance and maintain a high Q-factor. An 8-shape stacked inductor is designed to extend the common-mode resonant peak around the 2nd harmonic frequency.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #13.1 / 15:50-16:15

王成

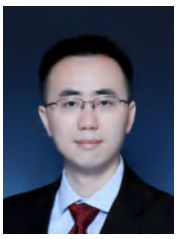
电子科技大学

王成，电子科技大学 电子科学与工程学院，教授/博导，国家青年人才。2008 年本科毕业于清华大学工程物理系；2011 年硕士毕业于中国工程物理研究院研究生部；2020 年博士毕业于美国麻省理工学院(MIT)电气工程与计算机科学系。2011 年~2015 年，担任中国工程物理研究院电子工程研究所助理研究员；2019 年-2020 年，担任美国亚德诺半导体(ADI) 研究科学家；2021 年 3 月，加入电子科技大学电子科学与工程学院。曾以一作或通讯作者身份，发表 Nature Electronics 封面论文 1 篇，ISSCC 会议论文 5 篇，JSSC 论文 4 篇等。荣获 2024 年度四川省青年五四奖章，2022 年度麻省理工科技评论“35 岁以下 35 人”（中国），SSCS 博士前成就奖，MIT 微系统实验室优秀论文奖和国家留学基金委优秀自费留学生奖等系列奖项。作为技术委员会主席 TPC chair，主办 IEEE IMWS-AMP 2023 和 RFIT 2024 国际会议。

TALK

Shushan: Cryogenic Silicon Integrated Circuits for the High Fidelity Quantum Interface

Cryogenic CMOS and SiGe integrated circuits working at 4K or below have been adopted at the sensing and manipulation of large-scale Qubit arrays in quantum computing, aiming at solving the scalability, fidelity and speed bottlenecks of quantum computing. Additionally, this technology is also highly potential in wireless sensing, astronomy and other cutting-edge research of physics. This presentation provides a research overview of the Integrated Physics Group (IPG), University of Electronic Science and Technology of China (UESTC). It mainly focuses on the recently launched cryogenic quantum measurement and control chipset “Shusha” series, including the superconducting quantum readout chip “Emei”, the superconducting quantum manipulation chip “Konka”, and the silicon-based quantum manipulation chip “Xiling”.



2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #13.2 / 16:15-16:40

潘思宁

清华大学

潘思宁 2013 年本科毕业于清华大学电子工程系，获学士学位，2016/2021 年在荷兰代尔夫特理工大学微电子系获硕士/博士学位（均获荣誉学位），2021 年至 2022 年在荷兰代尔夫特理工大学从事博士后研究，2022 年 4 月全职回国加入清华大学集成电路学院，任教研系列助理教授。主要从事智能传感器电路，CMOS 基准源，存算一体电路等模拟/数模混合电路研究。在芯片设计顶级会议 ISSCC 及顶级期刊 JSSC 发表论文共 26 篇，其中一作/通讯 13 篇。

TALK

A 143dB Dynamic Range 119dB CMRR Capacitance-to-Digital Converter for High-Resolution Floating-Target Displacement Sensing

This paper presents a capacitive displacement sensor, in which sensing capacitance is converted to phase shift via a low-pass RC front-end and then digitized by a high-resolution Phase-Domain Delta-Sigma modulator (PDΔΣM). With inherent high/low-pass noise filtering provided by the front-end/readout circuits, both low-frequency and high-frequency interferences are rejected, which can be reflected from the sensor's CMRR of 119dB near DC and 97dB around 100MHz. Also, the prototype sensor achieves a >143dB (35.2aF~500pF) dynamic range (DR) without sub-ranging and less than 24.7ppm/°C temperature drift.

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #13.3 / 16:40-17:05

鲁文高

北京大学

鲁文高，博士、研究员。2000 年、2005 年分别获北京大学学士、博士学位，主要从事模拟 IC 的科研与教学，现任北京大学集成电路学院副院长，集成电路设计系主任，入选国家级高层次人才计划。

TALK

A 320×256 6.9mW 2.2mK-NETD 120.4dB-DR LW-IRFPA with Pixel-Paralleled Light-Driven 20b Current-to-Phase ADC

Peking University presents a 320×256, 120.4dB Long-Wavelength Infrared Focal Plane Array. Leveraging on a pixel-parallel, low-power, 20b ADC architecture based on a light-current-controlled oscillator, the sensor acquires images at 60fps with 2.2mK NETD, while consuming 6.4mW of power.

聂凯明

天津大学

2025 年 3 月 27 日 · 第 2 天

大宴会厅 3

Talk #13.4 / 17:05-17:30

聂凯明，博士，英才副教授，国家级青年人才，主要从事高端 CMOS 图像传感器芯片设计与模拟集成电路设计与研究，负责和领导设计完成十余款大规模高端 CMOS 图像传感器芯片。 主持包括国家重点研发计划课题、国家自然科学基金联合基金重点项目、国家自然科学基金面上项目和青年项目在内的科研项目 10 余项。作为第一作者或通讯作者发表在本领域高水平期刊 IEEE JSSC、IEEE TCASI 和 IEEE TCASVT 上在内的学术论文 20 余篇，获得中国发明专利授权 10 余项，获得美国发明专利授权 2 项。获评 2018、2022、2023 年天津市科技进步一等奖、2023、2024 年中国国际大学生创新大赛国家级金奖指导教师等荣誉。

TALK

A 1920×1080 Array 2D/3D Image Sensor with 3μs Row-Time Single-Slope ADC and 100MHz Demodulated PPD locked-in Pixel

Time of flight (ToF) range sensor provides three dimensional depth information of objects in the form of a two dimensional array by cooperating with near infrared active light emitters. The application of ToF has been extremely widespread, such as robotics, automotive, augmented reality, etc. We recently have presented a 1920×1080 array 2D/3D image sensor with 3μs row-time single-slope ADC (SSADC) and 100MHz demodulated locked-in pixel. To obtain reliable depth information, a backside-illuminated 6μm ×6μm PPD pixel with high built-in electric field is used to accelerate charge transfer. Storage diodes are designed to collect demodulated electrons for correlated double sampling readout. The 2-tap pixel and differential multiplexing readout architecture realize both image modes (2D and 3D) working with full-HD resolution. To overcome the limitation of quantization speed in conventional structures, we introduce a 4-bit time-to-digital converter (TDC) into the 8-bit SSADC for residual information quantization, achieving 3μs row-time and 12-bit readout accuracy. A prototype chip is fabricated in a 110-nm BSI CIS process. The designed PPD enabled a low depth noise of under 0.43% over the range of 0.3–1.5 m, with a modulation frequency of 100 MHz. By adopting the high-speed SSADC, the 2D and 3D frame rates achieve 300fps and 60fps, respectively.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #14.1 / 08:30-08:55

余益明

电子科技大学

余益明博士，2017 年毕业于电子科技大学，2018 年，加入电子科技大学担任讲师，2021 年晋升为副教授，2020 年至 2021 年期间，前往美国普林斯顿大学从事博士后研究。余益明博士专注于毫米波硅基阵列前端芯片及其关键电路宽带化技术等方面的前沿研究。近 5 年以一作或通讯作者身份在 IEEE ISSCC、JSSC 等国内外集成电路领域高水平学术期刊和会议上发表论文 35 余篇；申请国家发明专利 30 余项、国际发明专利 3 项，其中授权 15 余项。

TALK

A Reconfigurable Phased-Array Transceiver Front-End for 5G New Radio

A 5G NR phased array transceiver is proposed by implementing reconfigurable frequency converters covering both the 24~30GHz and 36~40GHz bands, while only requiring a LO range of 10~12GHz with 4~6GHz IF. The transceiver achieves >43dB image-rejection ratio with competitive gain and linearity in all the bands. Besides, a built-in calibration method is further proposed to compensate for gain and phase errors in each channel, which improves the RMS gain and phase errors at least by 0.2dB and 4°.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #14.2 / 08:55-09:20

贾海昆

清华大学

贾海昆，副教授，博士生导师。2009 年本科毕业于清华大学微纳电子系，2015 年博士毕业于清华大学微纳电子系。2015 年至 2016 年在香港科技大学从事博士后研究工作。2016 年至 2019 年在硅谷从事高速串口设计工作。2019 年 9 月入职清华大学集成电路学院。主要研究方向为硅基毫米波/太赫兹集成电路设计以及高速串行接口技术。作为负责人承担科技部重点研发计划课题、国家自然科学基金等科研项目。近五年在 ISSCC/JSSC/VLSI/TMTT 等集成电路设计领域顶级学术会议和期刊上发表高水平学术论文 80 余篇。

TALK

Research on Millimeter-wave Multi-beam Phased Array in CMOS Process

Millimeter-wave multi-beam phased array is one of the most critical components in satellite communication, which can greatly improve the capacity of satellite communication. However, as the number of beams increases from dual-beam to quad-beam and then to octa-beam, the complexity of the phased array has increased sharply, bringing various challenges such as the chip area, power amplifier's signal peak-to-average ratio, channel isolation, and insertion loss of the power divider/combiner network. Innovative circuit techniques and system architectures are needed to make breakthroughs. This report introduces some research progress in the circuit and system architecture of millimeter-wave multi-beam phased array in CMOS process.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #14.3 / 09:20-09:45

杨孟儒

南京航空航天大学

杨孟儒，2024 年博士毕业于东南大学，现任南京航空航天大学集成电路学院特聘副研究员，目前研究方向为面向宽带卫星通信的毫米波相控阵芯片。

TALK

K/Ka-Band Hybrid-Packaged Four-Element Four-Beam Phased-Array Transmitter and Receiver Front-Ends With Optimized Beamforming Passive Networks

This article presents K/Ka-band four-element four-beam phased-array transmitter (TX) and receiver (RX) front-ends. Hybrid-packaged technology is employed, consisting of one TX/RX 65-nm CMOS beamformer and four 0.1-μm GaAs power amplifiers (PAs)/low-noise amplifiers (LNAs). Each beam maintains a full connection to every antenna element without degrading array gain. A compact and symmetrical layout floor-plan is proposed to reduce signal routing complexity. Signal distribution and combination are performed through two optimized tree-type and rectangular-shaped beamforming networks to improve the beam-to-beam consistency and isolation. The TX/RX CMOS beamformer provides an energy-efficient solution by adopting low-power phase/amplitude controls. The second harmonic trap is co-optimized with the transformer-based matching to enhance linearity in the TX. A new L-type inductor-enhanced matching network is devised in the RX to broaden bandwidth. In addition, the digital circuit introduces a voting mechanism to improve fault tolerance. Utilizing fanout wafer-level chip-scale packaging, both hybrid-packaged TX and RX front-ends occupy an area of 50 mm2. The proposed TX demonstrates a measured small-signal gain of 23.5–26.5 dB across 17.7–20.2 GHz. The output 1-dB compression point (P1 dB) and the maximal power-added efficiency (PAEMAX) reach 21.2–23.2 dBm and 26%–30%, respectively. The proposed RX achieves a measured average gain of 24 dB across 27.5–30 GHz with a minimal noise figure (NF) of 3.1 dB. Both TX and RX exhibit uniform performance across all channels, while consuming a maximal power of 2600 and 264 mW, respectively, equivalent to 162.5–16.5 mW per element per beam.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #14.4 / 09:45-10:10

王力

香港科技大学

王力博士 2016 年本科毕业于华中科技大学，2021 年博士毕业于香港科技大学，2022~2024 年在香港科技大学做博士后研究。主要研究方向包括高速光电互联、时钟及数据恢复、高带宽存储器接口、毫米波相位阵列及频率综合等。发表论文 30 余篇，中美专利 5 项，一作文章十余篇，包括 JSSC, VLSI，CICC, ESSERC 等。担任 JSSC, TMTT, SSCL 等多个期刊审稿人。

TALK

A Compact Ka-Band Phased-Array Transmitter with On-Chip Phase-Locked Loop

Millimeter-wave (mmWave) phased-array transmitters play a vital role in 5G communications by enabling precise beam steering with high directivity. This presentation introduces a Ka-band, 4-element phased array transmitter (TX) that features an intermediate-frequency local-oscillator phase shifting (IFLO PS) architecture, demonstrating exceptional power and area efficiency, highly linear gain-invariant phase shifting, and phase-invariant gain control. The TX utilizes a sliding-IF architecture, integrating an on-chip phase-locked loop (PLL) with a divider to generate a 22.4-GHz radio-frequency local oscillator (RFLO) and a 5.6-GHz IFLO. By employing a Mux-and-Interpolation-based IFLO phase shifter and a transadmittance-transimpedance IF variable gain amplifier (VGA), the TX achieves an impressive measured RMS phase error of 0.63° to 0.85°, a minimal RMS PS-induced gain error of 0.02 to 0.05 dB, and a remarkably low RMS gain control-induced phase error of 0.3° to 0.6°. The on-chip PLL is compact, occupying a core area of only 0.057 mm^2, and features an integrated jitter of 61.2 fs.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #15.1 / 08:30-08:55

罗宇轩

浙江大学

罗宇轩 2014 年本科毕业于电子科技大学，2018 年博士毕业于新加坡国立大学，2018 年至 2020 年于新加坡国立大学任博士后研究员，2020 年加入浙江大学任百人计划研究员。罗博士专注于模拟/混合信号集成电路设计的研究，研究兴趣包括传感器专用接口电路、高精度模拟电路等。罗博士担任了 IEEE ICTA 会议 TPC 成员，2022 年 IEEE APCCAS 会议传感器电路与系统分会场主席及 2024 年 IEEE ICTA 会议培训课程主席。自 2024 年起，罗博士担任 IEEE CASS 学会职业发展中心主任。罗博士获得了由新加坡工程师协会颁发的 2018 年度卓越工程成就奖。

TALK

Sensor Interface Circuits for Large-Scale Tactile Sensing

Covering robots entirely with electronic skins (e-skins) has been a long-term aspiration. However, the number and density of the tactile sensors are limited by factors such as routing complexity, signal latency, and power consumption. This talk will introduce sensor interface circuits for robotic tactile sensing, including techniques such as analog multiplexers, nueral-inspired event-driven circuits and inter-chip communication protocols. The proposed techniques can effectively tackle the problems above and significantly improve the integration density and scale of the e-skin system.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #15.2 / 08:55-09:20

唐中

杭州万高科技股份有限公司

唐中博士本科和博士毕业于浙江大学，2020 年至 2023 年在荷兰代尔夫特理工大学担任博士后研究员，现为杭州万高科技股份有限公司模拟设计部经理，研究方向为高性能数模混合集成电路设计。研究成果发表在集成电路知名期刊或会议 40 余篇，包含第一/通讯作者期刊 JSSC 和 ISSCC 10 篇。其博士论文入选中国电子学会优秀博士论文奖，以及第三期电子信息前沿青年学者出版工程。曾获 ICAC 2024 最佳报告奖。

TALK

A Sub-1V 14b BW/Power Scalable CT Sensor Interface with a Frequency-Controlled Current Source

This work presents a bandwidth/power scalable CT sensor interface. A frequency-controlled current source is proposed to enable a gm-C CTDSM to achieve a near-consistent SNDR of ~84dB over a 200× bandwidth/power range. Operated from a sub-1V supply, it has an input-referred noise density of 46nV/rtHz and a FoM of 178.2dB.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #15.3 / 09:20-09:45

李家明

澳门大学

李家明博士現為澳門大學微電子研究院之助理教授。他於 2016 年從澳門大學獲得博士學位。在 2017 至 2019 年間他在哈佛大學擔任博士後，在 Donhee Ham 教授之實驗室設計高吞吐量之核磁共振系統。現時主要研究領域為模擬芯片設計、傳感器前端電路、核磁共振系統微型化、及芯片跨學科的應用及交叉創新。他已發表超過 50 篇同儕審查期刊及會議文章，當中包括 6 篇發佈於 IEEE 國際固態電路研討會(ISSCC)及 10 篇發佈於 IEEE Journal of Solid-State Circuits 之論文。指導的學生獲得了 IEEE SSCS Predoctoral Achievement Award, IEEE SSCS/IEEE CAS Student Travel Grant、IEEE Bioesensors Best Paper Award、華人芯片研討會最佳學生海報等獎項。

TALK

A 4,100μm2 Wire-Metal-Based Temperature Sensor with a Fractional-Discharge FLL and a Time-Domain Amplifier with ±0.2°C Inaccuracy (3σ) from −40 to 125°C and 45fJ·K2 Resolution FoM in 28nm CMOS

A 4,100μm2 wire-metal-based temperature sensor in 28nm CMOS features two innovations: 1) a fractional-discharge scheme to shrink the discharge window to 10% of the operating period, preserving the power consumption while avoiding area-consuming resistors; 2) a time-domain amplifier to amplify the output of the sensing frontend with sub-1V VDD, with chopping to mitigate the dc-offset and 1/f-noise. It achieves 3σ inaccuracy of +/-0.2°C from −40 to 125°C and best-in-class resolution FoM of 45fJ·K2.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #15.4 / 09:45-10:10

张沏琳

清华大学

Milin Zhang is an associate professor in the department of Electronic Engineering, Tsinghua University. She received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2004 and 2006, respectively, and the Ph.D. degree in the Electronic and Computer Engineering Department, Hong Kong University of Science and Technology (HKUST), Hong Kong. After finishing her doctoral studies, she worked as a postdoctoral researcher at the University of Pennsylvania (UPenn). She joined Tsinghua University in 2016. Her research interests include designing of smart sensors, sensor interface circuit and system design for biomedical applications.

She serves and has served as the Senior Associate Editor (SAE) of TCAS-Ⅱ, Associate Editor (AE) of TBioCAS, the TPC member of ISSCC, CICC, A-SSCC and CASS. She is the Chapter chair of the SSCS Beijing chapter. She is the Distinguished Lecturer of CASS and IEEE WiE. She has received the Best Paper Award of the BioCAS Track of the 2014 International Symposium on Circuits and Systems (ISCAS), the Best Paper Award (1st place) of the 2015 Biomedical Circuits and Systems Conference (BioCAS), the best student paper award (2nd place) of ISCAS 2017, the Best Paper Award of ICM 2024.

TALK

Millimeter-sized Wireless Electrochemical Sensing SoC

Inflammatory cytokines play a crucial role as biomarkers in the management of chronic diseases like autoimmune disorders, cardiovascular diseases, and cancer. However, key obstacle lies in achieving both high sensitivity and a wide dynamic range in an electrochemical implant system specifically tailored for the detection of inflammatory cytokines. Existed electrochemical sensing solutions rely on three-electrode (3E) systems or Ion-Sensitive Field-Effect Transistors (ISFETs). The contact between the solution and the electrode surface affects the current sensitivity. This work proposes a millimeter-sized, high sensitivity, wide dynamic range electrochemical sensing IC with 16-channel thin-film OECT integrated onto the top. Ultrasonic wireless power and backscatter wireless communication technology are utilized.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #16.1 / 08:30-08:55

宋飞

芯翼信息科技（上海）有限公司

宋飞，2009 年博士毕业于北京大学微电子系，现担任芯翼信息科技射频模拟部总监。

TALK

A 28nm Multimode Multiband RF Transceiver with Harmonic Rejection TX and Spur Avoidance RX Supporting LTE Cat1bis

A low-cost (QFN) 28nm RF transceiver supporting LTE Cat1bis for IoT applications is presented. The low-power IC consumes 40mW in receive mode and 113mW in TX mode covering 0.6 to 2.7GHz. The receiver achieves an FDD/TDD sensitivity of better than -99dBm.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #16.2 / 08:55-09:20

阳至瞻

澳门大学

阳至瞻于 2016 年在南京航空航天大学获得学士学位，2019 年在电子科技大学获得硕士学位，2024 年在澳门大学获得电气与计算机工程博士学位。他目前是澳门大学模拟与混合信号超大规模集成电路国家重点实验室的博士后研究员，致力于研究面向物联网的低功耗收发芯片与频率源。

TALK

Power-efficient Transceiver Techniques for Long-Range IoT Applications

This presentation introduces advanced radio technologies for next-generation IoT applications, delivering extended range and superior energy efficiency. The innovations include: (1) an ultra-low-power (ULP) active RF tag achieving 20.8% transmission efficiency at -20.3 dBm EIRP; and (2) a multimodal wake-up receiver with 2D identification, demonstrating -68/-82 dBm sensitivity at ultralow power consumption of 9.9 nW/39.6 μW. These breakthroughs establish new insights for energy-efficient, long-range IoT communications.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #16.3 / 09:20-09:45

王科平

天津大学

王科平，天津大学微电子学院教授、博士生导师。主要研究方向为：宽带射频与毫米波集成电路、射频集成电路与微纳传感器协同设计、应用于物联网和生物医疗系统的超低功耗无线集成电路等。主持国家重点研发计划项目重点专项（首席）一项，国家自然基金委联合重点项目一项、面上项目两项，JKW 国防创新项目两项等国家级项目。获天津市科技进步一等奖、中国电子学会科技进步二等奖，入选国家级青年人才。在集成电路领域共发表论文百余篇，包括 JSSC/ISSCC 论文九篇，授权美国/中国发明专利二十余项。

TALK

A Low-Power Blocker-Tolerant Wideband Receiver With Bias-Tunable Mixer and Effective Switch Resistance Compensation

This paper presents a mixer-first blocker-tolerant receiver (RX) with effective switch resistance (RSW) compensation and high-Q selectivity. By analyzing the impact of non-ideal 1/N LO duty-cycle and effective RSW on mixer-first RX, an effective RSW compensation technique is proposed to mitigate noise figure (NF) and out-of-band (OB) third-order intercept point (IIP3) performance degradation caused by reduced LO conduction duty-cycle at high frequencies. A bias-tunable mixer is then designed, enabling dynamic adjustment of the mixer's bias voltage and improvement of the effective RSW over the entire frequency band. It improves NF and OB-IIP3 performance at the high frequencies with extremely low-power consumption of LO drivers. In addition, the proposed RX achieves high-Q selectivity by combining an auxiliary N-path filter at RF and an analog finite-impulse-response (AFIR) filter at baseband (BB). The RX prototype, fab-ricated in a 55-nm CMOS process, achieves wide-band tunable high-Q selectivity from 0.4 to 2.6 GHz with the double side-band (DSB) NF from 2.4 to 3.5 dB. The RX achieves +15.4/19.2 dBm OB-IIP3 at 10/80 MHz offset. When the -10/0 dBm continuous-waveform (CW) blockers were injected at 40 MHz offset, the DSB-NF only increased to 5.4/11.6 dB. Over the frequency range of interest, total RX power consumption is 5.4 to 11.8 mW, with the LO driver requiring only 2.9 mW/GHz. The active chip area is 0.29 mm2.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #16.4 / 09:45-10:10

李巍

复旦大学

李巍，复旦大学微电子学院研究员，博士生导师。1986 年 1989 年分获哈尔滨工程大学电子工程工学学士学位和硕士学位，2001 年获比利时根特大学电子工程博士学位。1989 年始在哈工程从事射频微波电路及系统教学科研工作，参与若干国家“七五”“八五”计划课题。1997 年加入比利时根特大学工学院 INTEC-design 实验室，参与欧盟 APON 项目研发。2002 年加入上海诺基亚贝尔研发创新中心，参与移动通信协议标准研发。2004 年加入复旦大学微电子学院及集成芯片与系统全国重点实验室，先后主持和参与“新一代宽带无线移动通信网”国家科技重大专项课题、国家自然科学基金项目、国家 863/973 计划课题、上海市科技创新行动计划集成电路设计专项、国家重点实验室课题、国家重点研发计划课题、其它省部委课题等。发表含 JSSC, TMTT, TCAS-I/II, TVLSI, ISSCC, S-VLSI, ESSCIRC, A-SSCC 等 140+篇同行评议论文，拥有 30+项发明专利，曾获上海技术发明奖一等奖。主要研究方向为硅基射频/模拟/毫米波集成电路关键技术。

TALK

Compact Full-Duplex Receiver with Wideband Multi-Domain Hilbert-Transform-Equalization Cancellation Based on Multi-Stage APFs Achieving 65dB SIC Across 120MHz BW

An 0.5-5GHz FD RX with wideband multi-domain HTE cancellation based on multi-stage APFs is presented. Cascading low noise 1st order APF and 2nd order APF with Gm and Q tunability are proposed in cancellers to meet >120MHz bandwidth and required gain/delay flatness. FD RX achieves 34-39.7 dB SIC for 80MHz modulated signal with NF degradation of 1.2-2.1dB, while occupying only 0.5 mm2 active chip area. For 120MHz BW, total SIC of 65dB is measured with initial circulator isolation of 28dB.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #17.1 / 10:30-10:55

单伟伟

东南大学

单伟伟，东南大学青年首席教授、教育部长江学者特聘教授、国家优秀青年基金获得者。博士毕业于清华大学。现为东南大学国家 ASIC 工程中心常务副主任、江苏省集成电路设计自动化省高校重点实验室主任。研究方向为高能效集成电路设计及其设计方法学，包括低功耗定制电路、弹性调节自适应设计方法、高能效智能芯片等。研究成果在 SCI 和 EI 会议上发表 60 余篇论文，含集成电路顶会 ISSCC、顶刊 JSSC 、IEEE TCASI/II/CAD 等期刊、VLSI Symposium、 ESSCIRC、DAC、CICC、A-SSCC 等。授权第一发明人发明专利 30 余项（成果转化 5 项）。获国家科技进步二等奖、中国电子学会技术发明一等奖。

TALK

DSC-TRCP: Dynamically Self-Calibrating Tunable Replica Critical Paths Based Timing Monitoring for Variation Resilient Circuits

We propose a dynamically self-calibrating tunable replica CPs (DSC-TRCP) based adaptive voltage scaling (AVS) which integrates the advantages of both in-situ and indirect monitoring methods while overcoming their disadvantages. Our TRCP is dynamically calibrated to follow the selected CPs. We also propose a low-overhead, low-latency timing monitor (called Mini-Razor) inserted at the half-path point to cooperate with TRCP to monitor the timing of the main circuit. Applied on a BNN accelerator and implemented in a 28nm CMOS technology, the maximum calibration error between DSC-TRCP and actual CPs does not exceed 2.1% under different PVT variations. Operating at 31 MHz and 0.55 V, the chip provides a 58% reduction in power consumption with only a 0.65% increase in area cost, and offers up to 232% frequency gain in the near-threshold region. Our DSC-TRCP achieves high AVS gains with low costs and ensures the effectiveness of monitoring

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #17.2 / 10:55-11:20

王扬

清华大学

清华大学副研究员，长期从事人工智能加速器相关技术研究，近三年以第一/共一作者在集成电路/体系架构顶级会议/期刊 ISSCC/VLSIC/ ISCA/JSSC/TCAS-I 等发表论文 21 篇，共发表论文 40 余篇，成果获得“中国半导体学报十大进展提名奖”，入选“中国芯片科学十大进展”；担任 JSSC、AICAS、OJ-SSCS、TCAS-I 会议与期刊审稿人，主持科技部重大项目课题、国家自然基金青年基金项目。

TALK

A Versatile Transformer Accelerator With Low-Rank Estimation and Heterogeneous Dataflow

Transformer model has demonstrated outstanding performance in the field of artificial intelligence. However, its remarkable performance comes at the cost of substantial computational complexity, posing limitations on deploying transformers from cloud to edge due to power and throughput constraints. There are two main challenges in designing a transformer accelerator for practical tasks. First, a transformer has inconsist ent bottlenecks due to input length changes: for short inputs, such as using vision transformer (ViT) for ImageNet or bidirectional encoder representations from transformers (BERT) for general language understanding evaluation (GLUE), the linear layer of the model becomes the computational bottleneck. In contrast, for long inputs, such as high-resolution images or long-text tasks, attention computation becomes the bottleneck. Second, even for a given input length, different layers in the model exhibit various computational characteristics and workloads, such as matrix sizes and data reuse strategies. This article introduces Ayaka, a versatile transformer accelerator designed to address these issues. Ayaka uses a cross-layer sparse prediction approach based on random projection (RP), enabling simultaneous sparsification of attention computation and linear layers, thereby enhancing throughput for various bottlenecks for different input lengths. Furthermore, Ayaka optimizes the sparse attention computation by leveraging the input translation invariance of softmax. In addition, Ayaka features a heterogeneous dataflow processing element (HDPE) design, dynamically adjusting stationary matrix operands based on the current computation to maximize on-chip data reuse and reduce memory footprint. With these features, Ayaka is so far the first accelerator that accelerates the whole attention layer. Evaluation of 12 typical models and tasks shows that it achieves a peak energy efficiency of 49.7 TOPS/W, which is 1.20–258.9× higher than the state-of-the-art works.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #17.3 / 11:20-11:45

杨杰

西湖大学

杨杰，西湖大学工学院研究员。2010 年、2015 年分别于天津大学与中国科学院半导体所获学士与博士学位；2015 年至 2019 年在加拿大卡尔加里大学从事博士后研究，2019 年 4 月加入西湖大学工学院。先后入选杭州市“西湖明珠工程”人才项目、杭州市海外高层次人才，并主持国家科技创新 2030-“脑科学与类脑研究”重大项目课题、浙江省“尖兵”研发攻关计划等科研项目。主要研究方向包括侵入式高通量脑机接口芯片、脑-语言神经解码以及类脑计算芯片。近五年，以第一作者或通讯作者在 IEEE JSSC、TBioCAS、JBHI、TBME、TNSRE、TCAS-II 等期刊发表论文 30 余篇。

TALK

An Energy-Efficient Unstructured Sparsity-Aware Deep SNN Accelerator With 3-D Computation Array

Deep spiking neural networks (DSNNs), such as spiking transformers, have demonstrated comparable performance to artificial neural networks (ANNs). With higher spike input sparsity and the utilization of accumulation (AC)-only operations, DSNNs have great potential for achieving high energy efficiency. Many researchers have proposed neuromorphic processors to accelerate spiking neural networks (SNNs) with dedicated architectures. However, three problems still exist when processing DSNNs, including redundant memory access among timesteps, inefficiency in exploiting unstructured sparsity in spikes, and the lack of optimizations for new operators involved in DSNNs. In this work, an accelerator for deep and sparse SNNs is proposed with three design features: a 3-D computation array that allows parallel computation of multiple timesteps to maximize weight data reuse and reduce external memory access; a parallel non-zero data fetcher that efficiently searches non-zero spike positions and fetches corresponding weights to reduce computation latency; and a multimode unified computation scheduler that can be configured to maximize energy efficiency for spiking convolution (SCONV), spiking Q,K, and V matrix generation, and spiking self-attention (SSA). The accelerator is implemented and fabricated using 40-nm CMOS technology. When compared with state-of-the-art sparse processors, it achieves the best energy efficiency of 0.078 pJ/SOP and the highest recognition accuracy of 77.6% on ImageNet using the spiking transformer algorithm.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #17.4 / 11:45-12:10

赵健

上海交通大学

赵健，上海交通大学集成电路学院副教授，IEEE 高级会员。从事专用传感接口芯片、生物医疗电子技术的研究。近年来在 IEEE-JSSC、ISSCC、VLSI-C 等期刊和会议发表论文 70 余篇，入选上海市“晨光计划”人才项目。先后担任 IEEE TbioCAS 与 IEEE TCAS-I 期刊的副编辑、国内高起点新刊《Cyborg and Bionic Systems》青年编委。入选 IEEE CASS Distinguished Lecturer。担任 IEEE CASS Digital Communication 常务委员，曾任 IEEE 上海分会 Young Professional Affinity Group 主席。

TALK

A 0.67-to-5.4 TSOPs/W Spiking Neural Network Accelerator With 128/256 Reconfigurable Neurons and Asynchronous Fully Connected Synapses

Recently, the fields of brain science and brain-inspired computing have witnessed rapid advancements. We are currently in a transitional period where “studying the brain” and “utilizing the brain” are developing collaboratively and will continue to do so in a long time. Current brain-inspired computing accelerators are often designed for specific tasks, making it challenging to simultaneously meet the demands of efficient biological neural network simulation and high-energy-efficiency brain-inspired computing. This report introduces a reconfigurable CMOS accelerator that can accommodate both requirements. It elaborates on technologies such as log-domain reconfigurable neurons and asynchronously fully connected synapses in time domain. Finally, it provides to achieve more efficient computing with limited silicon resources and to promote synchronized progress and breakthroughs in brain science and brain-inspired computing.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #18.1 / 10:30-10:55

程林

中国科学技术大学

程林，现任中国科学技术大学国家示范性微电子学院教授、副院长。主要研究方向为功率及模拟集成电路设计， 包括高压 / 高速直流 - 直流转换器、隔离电源芯片、无线充电芯片、模拟前端芯片等。在国际会议和期刊上发表论文 70 多篇，其中以第一或通讯作者发表集成 ISSCC 和 JSSC 论文 27 篇。曾获 2025 年 IEEE ASP-DAC Special Feature Award, 2020 年 IEEE ASP-DAC Best Design Award、 2018 年香港科学会青年科学家（提名奖）和 2015 年 IEEE 固态电路协会 Pre-Doctoral Achievement Award 。现任 ISSCC 技术委员会 Power Management 分委会成员。

TALK

A Multi-Core Isolated DC-DC Converter with Embedded Magnetic-Core Transformer and Low EMI Emissions

A multi-core isolated DC-DC converter with an embedded magnetic-core transformer is proposed, reducing conducted EMI and output voltage ripple. Each core oscillates at different frequencies, suppressing radiated EMI without frequency hopping. Fabricated in a 0.18μm BCD process and assembled in an LGA package, the converter achieves 53.2% peak efficiency, <5mV ripple, and meets CISPR-32 Class-B EMI compliance on a two-layer PCB.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #18.2 / 10:55-11:20

陈之原

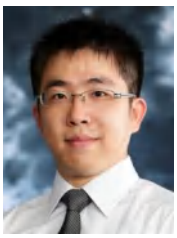
复旦大学

陈之原分别于 2011 年、2013 年和 2018 年在澳门大学获得学士、硕士和博士学位。自 2018 年起，他任职于复旦大学微电子学院，现为青年研究员。其研究兴趣包括超低功耗管理系统、太阳能与压电能量采集系统。他是 IEEE 国际电路与系统研讨会的评审委员会成员，也是 SCI 期刊《Energies》和《微电子学》编委。在包括 JSSC 和 ISSCC 在内的顶级期刊和会议上发表数十篇文章。

TALK

Enhancing Efficiency in Piezoelectric Energy Harvesting: Cross-Flip Synchronized Switch Harvesting on Capacitors Rectifier and Multi-Output DC-DC Converters Utilizing Shared Capacitors

This manuscript details an innovative method known as cross-flip synchronized switch harvesting on capacitors (CF-SSHC), which is utilized in rectifiers and multi-output synchronous DC-DC converters featuring shared capacitors. This method introduces a cross-flipping mechanism that markedly surpasses traditional SSHC technology in both efficiency and output power. This study establishes a new standard for capacitor-based rectification interfaces by realizing the ultimate flipping phases and enabling multiple-input multiple-output configurations. Moreover, it showcases the system's capability to consistently harvest energy from a variety of oscillation frequencies and types, including shock and periodical oscillations, alongside off- and on-resonance scenarios. Its remarkable scalability and adaptability to different piezoelectric transducer (PT) array configurations render it an ideal candidate for meeting the dynamic requirements of Internet of Things (IoT) networks. The architecture has been crafted employing standard 0.18-μm CMOS technology, demonstrating an impressive voltage flipping efficiency of up to 83%. Relative to full-bridge rectifiers (FBR), this approach significantly augments maximum output power improving rate (MOPIR), reaching 5.06×under off-resonance and 4.78×under on-resonance conditions, besides attaining a 2.14× boost in power under shock excitation. Additionally, by leveraging six shared flying capacitors for DC-DC conversion directed at maximum power point tracking (MPPT), the proposed piezoelectric energy harvesting (PEH) framework reliably maintains a 4× MOPIR within an input power range of 1.42 μW to 28.4 μW.



姜俊敏

南方科技大学

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #18.3 / 11:20-11:45

姜俊敏，南方科技大学副教授，国家级和深圳市海外高层次人才，于 2011 年获浙江大学电子信息工程学士学位，于 2017 年获香港科技大学电子及计算机工程博士学位。于 2018-2021 年就职于美国德州仪器公司硅谷基尔比实验室。主要研究方向包括模拟与功率集成电路设计。在集成电路设计领域顶尖期刊和会议上共发表学术论文 50 余篇，包括 7 篇 ISSCC，拥有专利 30 余项，包括美国专利 6 项。2022 年获国家级海外高层次人才（青年项目），2023 年获深圳市产业发展与创新人才奖。

TALK

Batter-to-36V Continous Current Boost Converter

This work presents a battery to 12-36V hybrid boost converter with continuous input and output currents. The proposed design places a small power inductor in the middle and merges a Dickson switched-capacitor converter on the low-voltage side and a dual-branch interleaving SC voltage doubler on the HV side, obtaining high VCR and fast transient with no RHP zero. The converter delivers a maximum output power of 10.8W with a peak efficiency of 93% and a remarkable power density of 49.5mW/mm3.

黄俊威

澳门大学

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #18.4 / 11:45-12:10

黄俊威博士于 2018 年获得电子科技大学学士学位，并于 2024 年获得澳门大学博士学位。目前，他在澳门大学模拟与混合信号超大规模集成电路国家重点实验室（AMSV）担任博士后研究员，主要从事高电流密度和快瞬态响应的电源管理集成电路设计研究。他作为第一作者在国际顶尖会议和期刊 ISSCC，CICC，JSSC 和 TCAS-I 上发表了 5 篇论文。

TALK

A Dual-Loop Non-Uniform-Multi-Inductor Hybrid DC-DC Converter with Specified Inductor Current Allocation and Fast Transient Response

Efficient and high-performance power conversion from a 12V source is essential to meet the demands of modern high-end computing applications. Achieving higher efficiency and faster transient response is crucial to reduce system volume and cost. These characteristics are vital for a wide range of compute-intensive applications, including servers, portable devices, and automotive systems. This work proposes a hybrid power conversion architecture consisting of two stages to deliver a total output of 4.5A. The design employs a 1 MHz stage to provide the majority of the power, while a 20 MHz stage ensures precise load regulation and rapid transient response. The high-frequency stage utilizes optimized devices fabricated in a 180nm technology

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #19.1 / 10:30-10:55

祁楠

中国科学院半导体研究所

祁楠，中国科学院半导体研究所研究员，中国科学院大学岗位教授，博士生导师。2013 年毕业于清华大学获得工学博士，先后在美国俄勒冈州立大学、惠普公司任职博士后、高级工程师，从事硅基光电子集成芯片研究，2017 年加入中科院半导体所工作至今。主要从事光通信高速集成电路、硅基光电融合互连芯片等领域研究；主持国家自然科学基金重点项目和重大研究计划重点项目、国家重点研发计划项目课题等多项科研任务。祁楠博士是 IEEE SSCS、CAS 和 OSA 等学会会员，担任半导体学报编委、IEEE A-SSCC 和 ICTA 等会议程序委员会成员，其团队在包括 OFC、ISSCC、JSSC 等国际会议与期刊中发表论文 90 余篇。

TALK

Silicon-Photonic Transceiver Design for Co-Packaged Optics

A 4×112 Gb/s hybrid-integrated silicon photonic (SiPh) transceiver is presented for the linear-drive co-packaged optics (CPO). A quad-channel open-collector driver is co-designed with the arrayed traveling-wave (TW) Mach-Zehnder modulator (MZM) for high bandwidth (BW) and high efficiency. A linear trans-impedance amplifier (TIA) is proposed, which boosts the BW while maintaining a flat in-band response. Implemented in 180-nm SiGe BiCMOS, the driver and TIA are measured with over 35GHz BW. The complete SiPh TRX is built by co-packaging both the driver with MZM and TIA with photo detector (PD). Experimental results show 112 Gb/s channel speed in PAM-4 format. To emulate the CPO application, a compact-size evaluation board is made, and four-channel tests are completed.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #19.2 / 10:55-11:20

赵潇腾

西安电子科技大学

赵潇腾博士，西安电子科技大学教授、博士生导师，国家级青年人才项目入选者，专注于高速数据接口与芯粒（Chiplet）互连集成电路设计。主持并参与多项国家自然科学基金与科技部重点研发项目。在 IEEE ISSCC、JSSC、TMTT、TCASI、CICC、RFIC、ASSCC 等旗舰会议及期刊上发表论文 30 余篇，相关工作入选 2022 年“中国半导体十大研究进展候选”，获得科技研发及论文奖 3 项，拥有数十项专利与软件著作权。

TALK

A Reference-Less CDR Using SAR-Based Frequency Acquisition Technique Achieving 55ns Constant Band-Searching Time and up to 63.64 Gb/s/μs Acquisition Speed

A reference-less CDR using a SAR-based frequency acquisition (FA) technique is proposed for rapid interface setup. By identifying the frequency error polarity from the SLOW signal, the CDR achieves a constant band switching time of 55ns, setting a record for FA speed of up to 63.64 Gb/s/μs in the band switching step. With the help of the proposed charge pump, the total FA time of <150ns is achieved, which is at least 4X shorter than the existing works.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #19.3 / 11:20-11:45

王辉

上海交通大学

王辉，国家高层次青年人才，上海交通大学副教授。王教授在上海交通大学获得学士学位， 在加州大学圣地亚哥分校获得博士学位，博士毕业后在斯坦福大学进行博士后研究，之后加入美国高通公司，担任射频/混合信号芯片研发高级工程师，于 2022 年加入上海交通大学。

王教授长期从事射频与模拟集成电路设计的研究，并在领域内权威期刊和顶级会议发表多篇关于无线收发芯片、高性能频率芯片、高性能接口芯片等方向的研究成果。多篇论文获得最佳论文提名。授权美国专利 4 项。担任 JSSC，TCAS-I，TMTT 等学术期刊审稿人。

TALK

A 1.8GHz-3.0GHz Fully Integrated All-In-One CMOS Frequency Management Module Achieving -47/+42ppm Inaccuracy from -40°C to 95°C and -150/+70ppm After Accelerated Aging

This work presents a fully integrated FMM that employs a direct frequency synthesis structure that achieves a compact, low-cost, crystal-free FMM by: 1) fully-integrating an on-chip temperature-stabilized reference; 2) directly operating the synthesizer at fLC for RO noise suppression; 3) leveraging the high loop bandwidth to achieve fast frequency hopping with a 7μs settling time; and 4) exploiting the high frequency sinusoidal reference together with high-gain direct reference sampling.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #19.4 / 11:45-12:10

陈卓俊

湖南大学

陈卓俊，湖南大学集成电路学院副教授，博士生导师，入选湖南省湖湘青年英才、湖南省青年骨干教师培养计划，获湖南大学优秀教师新人奖、湖南省自然科学二等奖。主要从事高可靠集成电路设计，包括抗辐射模拟/混合信号集成电路设计、高能效专用加速器芯片设计等。近 5 年，主持国家自然科学基金面上/青年项目、基础加强重点项目课题等纵横向项目 20 项，成果转化 3 项，以第一作者或通讯作者身份在 IEEE JSSC 等集成电路领域顶级或权威期刊发表 SCI 论文 20 余篇（其中 IEEE Transactions 论文 15 篇），发表国际会议论文 10 余篇，获得授权国家发明专利近 20 项。

TALK

A Compute-in-Memory Annealing Processor with Interaction Coefficient Reuse and Sparse Energy Computation for Solving Combinatorial Optimization Problems

Since combinatorial optimization problems (COPs) are a class of non-deterministic polynomial-time (NP)-hard problems, it is impracticable to solve them in brute-force searches, which results in high energy consumption and long computation latency. The annealing processors based on the Ising model are naturally oriented to find approximate solutions. However, these processors face the challenges of frequent data movement between computing elements and memory units, resulting in significantly large area and high energy consumption. To address these issues, we present a fully digital annealing processor based on compute-in-memory (CIM) architecture. To enhance area efficiency, a CIM coefficient array is designed with an interaction coefficient reuse strategy. Moreover, a sparsity-aware adder tree is proposed to reduce unnecessary add operations, which can improve the energy efficiency. For searching the lowest energy state of the Ising model, a nonlinear probability flipping (NPF) approximate circuit is designed, which is based on a voting mechanism and on-chip random number generation with low hardware overhead. The proposed annealing processor is fabricated in a 55-nm CMOS process and used to solve the max-cut problem as well as the image segmentation problem. The measured results confirm the high energy efficiency (2.4 fJ at 0.9 V per spin) and the high area efficiency (402 μm2 per spin).

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #20.1 / 13:30-13:55

王源

北京大学

王源，北京大学教授，博士生导师。现任北京大学集成电路学院党委书记，微电子器件与电路教育部重点实验室主任。2021 年获得国家级人才基金支持，2024 年获得青年北京学者。长期从事类脑计算、存内计算等新型计算架构智能芯片设计研究，研制了多款人工智能芯片，在视听觉感知、认知计算、生物模拟等领域展示了广泛应用前景。作为项目负责人先后承担了国家重点研发计划项目、国家自然科学基金联合基金重点项目等国家级重大项目十余项。在包括 ISSCC、JSSC 在内的本领域期刊和会议上发表学术论文 100 余篇，获得专利授权 70 余项。

TALK

SKADI: A 28nm Complete K-SAT Solver Featuring Dual-Path SRAM-Based Macro and Incremental Update with 100% Solvability

Boolean satisfiability (K-SAT, K≥3) is an NP-complete problem hat widely exists in various fields. The key objective of the K-SAT problem is to determine whether a truth assignment exists for n Boolean variables Xi to satisfy all clauses that typically are in a conjunctive normal form F(x). Given its NP-complete nature, solving K-SAT problems on Von Neumann machines consumes extensive energy and time. To address this challenge, several ASIC solvers have been proposed, employing diverse methods such as continuous-time dynamics, Ising machine, and recurrent neural networks. However, all prior arts are incomplete solvers that are only capable of resolving satisfiable (SAT) cases, without providing proof for the unsatisfiability (UNSAT) of F(x). This constraint severely limits their practice usage, as the satisfiability of most real-world K-SAT problems is not predetermined, requiring solvers to verify the existence of solutions for F(x). This work (SKADI) presents a complete K-SAT solver. Prototyped in 28nm CMOS, the proposed design measures an average solution time of 17.1us for SAT cases and 42.2us for UNSAT cases under test sets with 50 variables and 218 clauses, offering 952× speedup and 3.4*105 × energy reduction over a complete software SAT solver on AMD Ryzen 5 4500U CPU. To authors' best knowledge, it is the first ASIC complete solver with 100% solvability, showing great potential in addressing applications like formal verification and fault diagnosis, where knowing the satisfiability of F(x) is critical.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #20.2 / 13:55-14:20

司鑫

东南大学

司鑫，东南大学副教授，紫金青年学者。研究方向为存内计算电路和存算 AI 芯片设计。累计发表存算相关 SCI/EI 论文 50 余篇，包含 15 篇 ISSCC，9 篇 JSSC。主持多项国家省部级项目/课题。担任 VLSI-DAT、ICTA 等多个 IEEE 学术会议的 TPC。

TALK

A 28nm 17.83-62.84TFLOPS/W Broadcast-Alignment Floating-Point-Compute-in-Memory Macro with Non-2's Complement MAC for CNNs and Transformers

Previous FP-CIM struggles to balance computation precision with input reusability for large overhead of peripherial alignment circuits. A 28nm broadcast-alignment true FP-CIM fabricated using embedded area-efficient adaptive-alignment scheme and format-mixed N2CMAC flow demonstrated an energy efficiency of 62.84TFLOPS/W and 90.15TOPS/W for both true BF16 and INT8 multiply-and-accumulate (MAC) operations with 100% input reusability and 0.016% accuracy loss of ViT @ImageNet.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #20.3 / 14:20-14:45

于维翰

澳门大学

于维翰 2018 年在中国澳门大学（UM）获得博士学位。2019 年至 2021 年，他作为访问学者加入斯坦福大学 Murmann Mixed-Signal Group。自 2021 年起，他担任澳门大学模拟与混合信号超大规模集成电路国家重点实验室（AMSV）助理教授。其研究兴趣包括边缘人工智能、存内计算、开关电容电路、能量收集射频收发器以及神经接口。

于博士已发表近 50 篇高质量学术论文，其中包括 12 篇发表于《IEEE 固态电路期刊》（IEEE JSSC）以及 7 篇发表于《IEEE 国际固态电路会议论文集》（IEEE ISSCC）。他荣获众多奖项，包括 FDCT Technological Invention Award, Science and Technology PSA Award, the IEEE SSCS Predoctoral Achievement Award, and IEEE Hall of Fame Award。

TALK

Breaking the Readout Wall: Energy Efficient In-Memory Processing Techniques for AIoT

1) Compute-in-memory (CIM) is a promising approach for realizing energy-efficient convolutional neural network (CNN) accelerators. Previous CIM works demonstrated a high peak energy efficiency of over 100 TOPS/W, with larger fabrics of 1000+ channels. Yet, they typically suffer from low utilization for small CNN layers (e.g., ~ 9% for ResNet-32). It penalizes their average energy efficiency, throughput density, and effective memory size by the utilization rate. In addition, the analog-to-digital converter (ADC) occupies most of their computing time (~ 90%), further hindering the CIM's throughput. This work presents an FLEX-CIM fabricated under 28-nm CMOS featuring: 1) an analog partial sum (APS) circuit to enable a flexible CIM Kernel size; 2) an overclocked fast multiply–accumulate array (FMA) to boost the throughput; and 3) an adaptive-resolution ADC to enhance the throughput and energy efficiency. The achieved utilization is 99.2% on ResNet-32. Under 4-bit MAC precision, the peak energy efficiency is 181.6 TOPS/W, and the peak throughput density is 25.63 TOPS/mm2.

2) An energy-harvester-powered ultra-low power (ULP) vibration-based condition monitoring (VbCM) chip with a digital compute-in-memory (CIM)-based deep neural network (DNN) accelerator. The VbCM chip achieves end-to-end signal processing, including a piezoelectric (PZ)-based accelerometer sensor and its readout circuit (RoC), a digital CIM-based DNN accelerator and a ULP radio system. To perform the targeted rotating bearing anomaly detection task with best-in-class accelerator power consumption and energy efficiency, the chip integrates several technologies from the algorithm level to the hardware level, including: 1) Compressing deep neural network (C-DNN) to reduce the network size through a feature

compressor module (FCM); 2) Signal chain characteristic adaptation from direct training of the time-domain feature extractor (TD-FEx); 3) ULP 13T SRAM CIM bitcell to perform high energy efficiency in-cell multiplication; and 4) ripple counter (RCNT)-based accumulation scheme to improve the overall energy efficiency of the accelerator under a 0.35 V supply voltage. The VbCM chip achieves 90.7 nW total power with an inference FR of 20 frames/s, and the DNN accelerator's energy efficiency achieves 18.8 fJ/MAC. With all the weight parameters statically stored in the CIM macros, the accelerator can operate with an inference accuracy of 91.3% while consuming 24.7 nW.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #20.4 / 14:45-15:10

薛晓勇

复旦大学

薛晓勇，博士，复旦大学微电子学院和集成芯片与系统全国重点实验室副研究员，博士生导师，从事存储器设计及应用研究，研究兴趣包括新原理存储器电路、存算一体、类脑智能算法及电路，以主要作者发表论文 80 余篇，包括 Nature Electronics 1 篇、IEEE 集成电路会刊 12 篇(含 top-1 顶刊 IEEE JSSC 3 篇)、集成电路旗舰会议 11 篇（含顶会 ISSCC、IEDM 和 VLSI 6 篇），相关工作被台积电、三星电子、Leti、MIT 等知名机构和黄如院士、张梦凡教授等知名专家引用，部分成果应用于华为海思、中兴通讯、北京智芯、中电科 58 所等；编写“十三五”国家重点出版物专著《嵌入式存储器架构、电路与应用》；担任著名期刊 IEEE TCAS-II 客座编辑；获上海市科委“探索者计划”、上海市计算机学会“杰出表现奖”、复旦大学集成电路技术集成攻关大平台“科研新秀奖”。

TALK

High-Density SRAM Design for Computing in Memory

Computing-in-memory (CIM) promises high energy efficiency (EE) and performance in accelerating the feed-forward (FF) and back-propagation (BP) processes of deep neural networks (DNNs) with less data movement and high parallelism. However, challenges still lie in large memory cells, network mapping, and IR-drop variation to realize efficient CIM implementation. In this work, a 28-nm 36 Kb static random-access memory (SRAM) CIM engine with nondestructive-read (NDR) cell and weight update energy saving is used for multiplyaccumulate (MAC) acceleration in artificial intelligence (AI) inference and train applications. A 4T1T SRAM bit-cell is proposed with NDR and records the smallest cell size of 0.173μm2. The power-on self-load-0 feature of the 4T1T cell saves the weight update energy and latency for writing 0. The sharedpath dual-mode read (SPDMR) brings fewer circuit overheads to support both FF and BP paths. The bit-interleaving weight mapping (BIWM) speeds up the BP path without slowing FF. IR-drop-aware adaptive clampers (IRDAA-Cs) with hierarchical read word-lines (RWLs) and read bit-lines (RBLs) apply possibly accurate voltages on near/far cells.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #21.1 / 13:30-13:55

邱浩

南京大学

邱浩，南京大学电子科学与工程学院副教授，国家级青年人才。南大本/硕、东京大学博士，以第一/通讯作者在 Nature Electron.、Nature Commun.、IEEE 集成电路顶刊 JSSC、ISSCC、IEDM、VLSI 等期刊和会议上发表论文 20 余篇，2 篇入选 ESI 高被引论文，他引超 2100 次，单篇最高近 1000 次，入选“爱思维尔中国高被引学者”。曾获江苏省科学技术一等奖、日本十大创新科技奖等。主持基金委重点项目、首批海外优青项目、面上项目、是创新研究群体、重大项目的核心成员、参与科技部国家重点研发计划等项目。

TALK

A 6.78-MHz Single-Stage Regulating Rectifier with Dual Outputs Simultaneously Charged in a Half Cycle Achieving 92.2%-Efficiency and 131-mW Output Power

This work proposed a 6.78-MHz single-stage dual-output (SSDO) regulating rectifier for biomedical wireless powering. It was implemented with three NMOS active diodes to minimize power loss otherwise by PMOS. To maximize POUT, dual outputs were charged simultaneously in a half cycle rather than in the conventional time-multiplexing manner. Measurement results verified two regulated voltages at 3.3V and 1.6V. The peak 92.2% ηREC and 131mW POUT were the highest compared to prior SSDO rectifiers.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #21.2 / 13:55-14:20

薛仲明

西安交通大学

薛仲明，西安交通大学副教授，博士后。本科，硕士，博士均就读于西安交通大学。主持国家自然科学基金青年基金项目 1 项，作为核心成员参加国家重点研发计划、国家自然基金重点等多项国家级纵向项目及多项横向项目。获陕西省技术发明一等奖，陕西省高等教育学校科学技术一等奖等奖励。发表 IEEE JSSC，IEEE TPE，IEEE MWCL，IEEE CICC, IEEE ISCAS 等论文 40 余篇，授权发明专利 6 项（含美国专利 1 项）。担任 IEEE TCAS-II，IEEE TPE，IEEE JSSC，IEEE Sensors Journal 等期刊的审稿人。研究方向包括高性能模拟集成电路设计，电源管理芯片与无线能量传输系统芯片等。

TALK

A 6.78MHz 94.2% Peak Efficiency Class-E Transmitter with Adaptive Real-part Impedance Matching and Imaginary-part Phase Compensation Achieving a 33W Wireless Power Transfer System

This work proposes a Class-E TX with an adaptive real part impedance matching technique and an imaginary part phase compensation controller in a 6.78MHz WPT system, to cope with the real and imaginary part impedance variation. This achieves ZVS and avoids HS and RC loss across the full complex impedance range. Measurement results show the proposed class-E architecture achieves 94.2% peak efficiency in TX and 33W maximum E2E output power in WPT system.

姚远

香港科技大学

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #21.3 / 14:20-14:45

2014 年获东北大学学士学位，于 2019 年和 2024 年分别获香港科技大学硕士和博士学位，师从暨永雄（KI Wing-Hung）教授和崔志英（TSUI Chi-Ying）教授。现留校从事博士后研究，对近场天线，无线传电系统，以及可植入医疗设备展开持续性创新性研究。

TALK

A 13.56-MHz Single-Input Dual-Output Wireless Power and Data Transfer System for Bio-Implants

A 13.56-MHz single-input dual-output (SIDO) wireless power and data transfer (WPDT) system designed for bio-implants is presented. The system incorporates a reconfigurable power amplifier (RPA) and an SIDO rectifier that generates regulated outputs of 1.2 and 2.5 V for different functional blocks of a bio-implant. A dynamic power distribution (DPD) scheme is employed to adjust the duty ratios of the outputs based on changing load conditions. The WPDT system makes use of the different reflected impedances of the two outputs to enable reliable data transfer. Implemented in a standard 65-nm CMOS process, the system achieves an uplink data rate of 423.75 kb/s, confirmed through experiments with pseudorandom binary sequence input data at distances of 6, 10, and 15 mm. Notably, the measured maximum power transfer efficiency (PTE) at coil separation of 6, 10, and 15 mm are 62.7%, 50.8%, and 32.4%, respectively, with an overall improvement of more than 20% in light-load efficiency compared to previous approaches.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #21.4 / 14:45-15:10

潘东方

中国科学技术大学

潘东方，中国科学技术大学研究员，IEEE 高级会员。主要研究方向是功率/射频集成电路设计，包括全集成隔离电源芯片、硅基毫米波雷达收发芯片、CMOS 功率放大器芯片和高速数字隔离器等。主持多项国家自然科学基金项目、博士后科学基金和企业攻关项目等。在国际会议和期刊上发表论文 30 多篇，其中第一作者发表集成电路设计领域顶级会议 ISSCC 和顶级期刊 JSSC 论文共 5 篇，以及 IEEE TCAS-I/II、CICC、ESSCIRC 和 IEEE MWTL 等。担任 IEEE JSSC、TCAS-I/II、IEEE MWTL 等国际知名期刊和会议审稿人。

TALK

A Dual-LC-Resonant Isolated DC-DC Converter Achieving 65.4% Peak Efficiency and Inherent Backscattering

A dual-LC-resonant isolated DC-DC converter incorporating inherent backscattering is proposed, increasing efficiency and achieving global voltage regulation without the need for a digital isolator. The unified power stage for both TX and RX allows a single chip and thus a single mask to be used for both. The converter achieves 65.4% peak efficiency, and 1.5W maximum output power.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #22.1 / 13:30-13:55

刘佳欣

电子科技大学

刘佳欣，电子科技大学特聘研究员、博士生导师。本科毕业于山东大学，硕博毕业于电子科技大学，美国德州大学奥斯汀分校联合培养博士生，清华大学博士后。
主要研究领域为模拟与混合信号集成电路设计。在芯片设计领域发表论文 50 余篇，其中顶级会议 ISSCC 和期刊 JSSC 论文 20 余篇。担任 IEEE TCAS-II 等多个期刊编委及会议 TPC 委员。

TALK

A Fully Dynamic Noise-Shaping SAR ADC Achieving 120dB SNDR and 189dB FoMs in 1kHz BW

This paper presents a fully dynamic and high-resolution NS-SAR ADC. It achieves 120.6dB SNDR and 132.5dB SFDR in 1kHz BW. The power consumption is 139.1μW, leading to a SNDR-based Schreier FoM of 189.2dB. With sampling rate varying from 1kS/s to 2MS/s, it maintains stable SNR while the power scales almost linearly. These advances are enabled by the combination of predict and skip (PAS) scheme, hybrid mismatch shaping, system-level chopping and floating inverter amplifier (FIA).

沈林晓

北京大学

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #22.2 / 13:55-14:20

沈林晓目前是北京大学博雅青年学者，助理教授，承担国自然面上，重点研发计划课题等项目与课题。他目前的研究兴趣包括：高性能 ADC 设计、智能传感器接口系统、和成像系统等。
沈林晓荣获多个国际奖项，包括 2024 年 CICC 最佳学生论文奖 ，大陆（含港澳）76 年首次的 ISSCC 技术论文奖等。他目前担任 CICC 技术委员会成员。

TALK

Rail-to-Rail ADC Input Buffer Designs Employing Continuous-Time Correlated Level Shifting and Split Coarse-Fine Techniques

With the development of high-resolution ADCs (>13b) leveraging the SAR topology, the pursuit of power efficiency in ADC design continues to make remarkable strides. However, as the CDAC increases to satisfy the kT/C noise specification, excessive driving stress is imposed on the front-end input buffer. Furthermore, a separate higher supply voltage is typically required for the driver to accommodate the input swing while maintaining the linearity requirement. The increasing load and wide supply voltage often cause the power consumption of the ADC core to be overshadowed by the power consumption of the driving buffer, presenting a bottleneck in achieving an overall energy-efficient system. This talk will discuss two techniques to address the above issues: continuous-time correlated level shifting and split coarse-fine techniques.

2025 年 3 月 28 日 · 第 3 天
大宴会厅 3
Talk #22.3 / 14:20-14:45

沈易

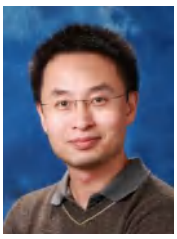
西安电子科技大学

沈易，西安电子科技大学教授，长期从事模拟和混合信号集成电路设计、高速模数转换器研究。发表 IEEE JSSC、IEEE TCAS-I、IEEE ISSCC、IEEE CICC 等学术论文 40 余篇。主持国家重点研发计划课题、国家自然科学基金面上项目、青年项目等多项科研项目。研究成果获得 2022 年教育部自然科学一等奖 1 项，2020 年中国电子学会自然科学一等奖 1 项等。先后担任国际期刊 IEEE TCAS-II、IEEE OJCAS、IEICE ELEX 的编委。

TALK

Energy-Efficient Pipelined ADC with Parallel-Operation SAR Sub-Quantizer and Dynamic Deadzone Ring Amplifier

Pipelined ADCs are widely used for wireless communication and instrumentation applications, but they are usually power-hungry due to the substantial use of residue amplifiers and flash quantizers. To address this challenge, this work proposes a parallel-operation SAR sub-conversion scheme and a low-noise dynamic deadzone ring amplifier to reduce the pipelined stages and improve the ADC power efficiency. The prototype 14b 1GS/s pipelined ADC achieves 68.2dB SNDR, 85.8dB SFDR, and 173.3dB FoM.



潘江鹏

香港中文大学

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #22.4 / 14:45-15:10

潘江鹏获香港中文大学电子工程学士学位和哲学硕士学位，后于葡萄牙里斯本技术大学（Instituto Superior Técnico, Technical University of Lisbon）取得电气与计算机工程博士学位。2001 年， 他加入香港中文大学电子工程系任教，现为该系教授。其研究领域涵盖高能效数据转换器电路（尤其是 Delta-Sigma 调制器）以及可穿戴生物医学设备与光学接口电路。

TALK

Bandpass Delta-Sigma modulators based on N-path Filters

In this talk, we will introduce a novel class of bandpass Delta-Sigma modulators (BPDSMs) that utilize N-path filters (NPFs). BPDSMs are an appealing solution for directly digitizing radio-frequency (RF) or intermediate-frequency (IF) signals. However, traditional BPDSMs, which rely on resonators implemented with active-RC, Gm-C, or Gm-LC circuits, are hindered by poor power efficiency and limited flexibility. Our proposed solution, the Gm-NPF circuit, offers a fresh approach to implementing resonators in BPDSMs. This method presents a core advantage in power efficiency, as it only requires a low-frequency amplifier to deliver high gain in the high-frequency passband. Furthermore, it enables a wide range of passband frequency tunning. In this talk, we will report the first two NPF-based BPDSMs and share their measurement outcomes. Additionally, we will provide a concise overview of the analysis of these complex periodically time-varying linear systems.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #23.1 / 15:25-15:50

邓伟

清华大学

邓伟，清华大学集成电路学院长聘副教授，入选国家高层次人才计划和国家青年人才计划。电子科技大学学士和硕士，日本东京工业大学博士，曾任美国苹果公司总部资深主任工程师，负责面向高速无线通信 SoC 的毫米波/混合信号芯片设计。现任职清华大学，主要研究方向为硅基射频/毫米波/太赫兹芯片设计与系统集成。

现任 ISSCC、VLSI、CICC、A-SSCC、RFIC 和 ESSCIRC 的技术委员会成员，IEEE SSCS 杰出讲师，以及 IEEE JSSC、IEEE SSC-L、半导体学报等期刊副主编或客座编辑，负责射频和无线方向。在 JSSC、IEEE T-CAS I、IEEE T-MTT 等期刊以及 ISSCC、VLSI 等国际会议发表论文 160 余篇，其中在 JSSC 和 ISSCC 发表论文 40 余篇；主持射频和无线芯片设计领域的多项国家重点科研项目。

TALK

D-Band Distributed MIMO Radar Transceiver and System

This talk introduces a D-band 4TX/4RX distributed MIMO radar transceiver with real-time synchronization for multistatic imaging system. The proposed synchronized radar system eliminates the time error, frequency error, and slope error of local oscillator signals between radar stations to ensure the correct acquisition and analysis of radar signals, which enables the combination of target data from multitude of transmitting and receiving stations coherently. In addition, several circuit design techniques for D-band radar transceivers are investigated. This work achieves better detection performance than the traditional MIMO radar with the same number of channels, demonstrating its advantages in future cooperative coherent multistatic imaging system.

2025 年 3 月 28 日 · 第 3 天
大宴会厅 1
Talk #23.2 / 15:50-16:15

刘力源

中国科学院半导体研究所

刘力源，男，博士，研究员，博士生导师。中国科学院半导体研究所研究员，中国科学院大学岗位教授。于 2005 年和 2010 年分别获清华大学微电子研究所电子工程系电气工程学士学位和博士学位；2010-2012 在清华大学电子工程系从事博士后研究；2012 年 7 月加入中国科学院半导体研究所半导体超晶格国家重点实验室，任副研究员。2018 年 1 月任半导体物理实验室(原半导体超晶格国家重点实验室)研究员。

刘力源研究员 CMOS 图像传感器、智能化处理器以及感存算融合的视觉芯片研究在 IEEE ISSCC、JSSC、TCAS-I/II 等集成电路领域重要学术会议和期刊上发表多篇论文。完成了 800×600 分辨率、1000fps 帧率高速图像传感器的整体设计和列并行读出电路设计，国内首次实现了具有 70dB 动态范围的超高速图像传感器和超高速相机，传感器通过电子四所组织的第三方测试；提出了一种基于动态可重构混合架构的单片视觉芯片，集成高速图像传感器、冯诺依曼型像素并行和行并行阵列处理器和非冯诺依曼型自组织映射（SOM）神经网络，是全球首个在复杂高级识别任务中也能达到 1000fps 系统级性能的视觉芯片；开展 CMOS 太赫兹图像传感器的研究，突破了 1THz 频段的 CMOS 太赫兹像素的关键技术，实现了国际上首款大阵列 CMOS 太赫兹图像传感器，扩展了传统 CIS 的光谱感知能力，为大规模展 CMOS 太赫兹图像传感器奠定了基础。

学术兼职包括：半导体学报编委，国际集成电路技术与应用大会议(ICTA)程序委员会主席(2019-2020)，亚洲固态电路会议(A-SSCC)程序委员会成员(2013-2018)；电气与电子工程师协会(IEEE)会员，IEEE 固态电路协会(SSCS)北京分会副主席；中科院青年创新促进会会员、 北京电子学会(BIE)理事，中国图形图象学会类脑视觉专委会委员，中国运筹学会智能工业数据解析与优化专委会理事。

TALK

A 3 THz CMOS Image Sensor

This paper presents a 3 THz terahertz CMOS image sensor (Tera-CIS). The sensor has a column-parallel readout (CPRO) architecture that integrates an antenna-coupled pixel array and CPRO circuit chains on a monolithic chip. The proposed compact 2T pixel adopts a step-covered patch antenna and a defected ground structure (DGS) to obtain sufficient sensitivity and bandwidth. The step-covered patch antenna model is developed to predict the pixel performances precisely. The DGS structure suppresses mutual coupling among adjacent pixels and shrinks the pixel pitch. In the CPRO circuit chain, chopping and oversampling techniques are employed to reduce noise and flexibly balance the dynamic range (DR) characteristics with the imaging rate. A digital decimation filter with a timemultiplexing fashion is adopted to alleviate resource pressure. A 16.4 k-pixel Tera-CIS was fabricated with a standard 0.18 μm CMOS

process. A 3 THz imaging platform with four different continuous-wave terahertz quantum cascade lasers was established. The pixel sensitivity was 753 V/W at 3.4 THz, with a measured detection bandwidth of 0.78 THz (from 3.08 to 3.86 THz). The DR in the voltage domain of the sensor reached 73 dB at 8 fps while the maximum DR in the power domain was 39.8 dB. Meanwhile, the sensor can operate up to 130 fps. The imaging system can achieve high-resolution imaging and clearly identify concealed objects.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #23.3 / 16:15-16:40

陈喆

东南大学

陈喆，副教授。2006 年本科毕业于电子科技大学，2014 年博士毕业于东南大学。2016 年~2018 年，赴美国德克萨斯州立大学博士后研究工作。2014 年至今，在东南大学信息科学与工程学院，毫米波全国重点实验室工作。2016 年~2018 年，赴美国德州大学进行博士后研究。

主要研究方向毫米波太赫兹 CMOS/SiGe 高速通信芯片、毫米波太赫兹频率源芯片等。主持国家重点研发计划项目芯片课题、国家自然科学基金面上、青年项目，及国内企业联合开发芯片项目等。在国际核心期刊 IEEE Journal of Solid-State Circuits, IEEE Transactions on Microwave Theory & Techniques, IEEE Solid-State Circuits Letters, IEEE Microwave and Wireless Components Letters，及国际学术会议 IEEE International Solid-State Circuits Conference (ISSCC) ，IEEE International Microwave Symposium (IMS)， IEEE International Microwave Symposium (RFIC)，IEEE International Wireless Symposium 等上发表学术论文八十余篇，持有多项国家发明专利，在国际学术会议作邀请报告及担任国内太赫兹学术会议 TPC 共主席等，担任多个国际核心期刊审稿人，获得教育部“学术新人奖”、华为-东南大学“紫金青年学者”。

TALK

Silicon-based THz Direct Modulation Communications

At present, there is a large demand for ultra-high-speed transmission over short distances by leveraging the rich frequency spectrum resources of terahertz band. For instance, in transmission scenarios ranging from meters to centimeters between large data cabinets, high-speed circuit boards, and chip-to-chip, there is huge demand for low-cost, high-integration, and high-speed interconnection solutions. Silicon-based terahertz direct modulation technology can achieve high-speed transmission in meter-level short-distance scenarios through large bandwidth, multiple channels, or multiple polarizations, while achieving low power consumption and high energy efficiency, making it promising for low-cost and large-scale applications. This research has achieved real-time high-speed transmission of 20/32/64 Gbps in the D-band based on direct modulation scheme in CMOS technology, providing possible silicon-based solutions for the next-generation short-distance ultra-high-speed interconnections.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 1

Talk #23.4 / 16:40-17:05

郭开喆

东南大学

郭开喆，东南大学青年首席教授、博士生导师。目前研究方向为用于 6G 高速通信和感知的毫米波和太赫兹 CMOS 集成电路设计。2010 年本科毕业于吉林大学物理学院，2013 年硕士毕业于电子科技大学电子工程学院，2020 年博士毕业于比利时鲁汶大学电气工程学院 MICAS 实验室。从 2021 年到 2023 年，在香港城市大学太赫兹和毫米波国家重点实验室做博士后。2023 年加入东南大学和紫金山实验室。获得过 IEEE 集成电路协会博士生成就奖。以第一作者发表 1 篇 ISSCC，2 篇 JSSC，2 篇 TACS-I，2 篇 TTST，以通信作者发表 2 篇 TMTT。参与项目包括江苏省科技重大专项项目、鹏城国家实验室重大攻关项目。

TALK

A 0.68-THz Receiver With Third-Order Subharmonic Mixing in 65-nm CMOS

This work a 0.68-THz receiver with third-order subharmonic mixing in a 65-nm CMOS technology. A third-order subharmonic mixer based on a double-balanced topology is proposed. The spurious mixing product of the mixer is utilized to increase the IF output of the mixer, thus improving the conversion gain and noise figure of the mixer. Besides, compensating capacitors are incorporated in the double-balanced topology to alleviate the severe signal imbalance in this topology at very high frequencies caused by its layout asymmetry. With enhanced signal balance, the conversion gain, noise figure, and isolation of the third-order subharmonic mixer are improved. The receiver achieves a measured noise figure of 28.4 dB at 682 GHz including the loss of the antenna. Among all the Silicon receivers above 430 GHz, this work has the lowest noise figure. Thanks to the inherent wide bandwidth of the double-balanced topology, the high order of the subharmonic mixer, and the high multiplying factor of the LO generation circuits, the proposed receiver with an integrated voltage-controlled oscillator obtains a measured input frequency range of 138 GHz, which is the highest among all the Silicon receivers above 400 GHz.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #24.1 / 15:25-15:50

卢旭阳

上海交通大学

卢旭阳，上海交通大学副教授，毛军发院士射频异质异构集成全国重点实验室（上海交通大学）骨干成员，海外优青。博士毕业于美国普林斯顿大学，研究方向是射频、模拟、毫米波、太赫兹、集成光学、以及生物电子集成电路。

TALK

Integrated Wireless Power Transfer, Communication, and Actuation

In this talk, a self-propelling microrobot that moves through ionic fluids at um/s will be presented. It employs on-chip traveling wave electroosmosis pump for actuation and a sub-GHz parity-time symmetry energy harvesting method for enhanced energy transfer efficiency during movement.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #24.2 / 15:50-16:15

陈秋锦

澳门大学

陈秋锦博士分别于 2020 年和 2024 年获得南方科技大学学士学位和澳门大学模拟与混合信号超大规模集成电路国家重点实验室博士学位。目前，陈博士是澳门大学模拟与混合信号超大规模集成电（AMSV）国家重点实验室的博士后研究员，研究方向包括射频能量采集与电源管理。陈博士担任了以下期刊的审稿人：IEEE Transactions on Circuits and Systems I: Regular Papers、IEEE Transactions on Circuits and Systems II: Express Briefs 和 Microelectronics Journal。

TALK

A Single-Input RF Energy-Harvesting Interface With Compensated-CEPE Control and 3-D Hill-Climbing MPPT Achieving − 28.5 dBm Sensitivity

This work presents a single-input radio frequency energy-harvesting (RFEH) interface with 3-D hill-climbing (HC) maximum power point tracking (MPPT). We use constant energy packet extraction (CEPE) control that facilitates power detection with low quiescent current. To reduce the error of the CEPE scheme at a low-voltage conversion ratio (VCR), we modify it with turn-on time compensation. We obtain the 3-D MPPT by searching the optimal: 1) the number of rectifier stages; 2) DC–DC input impedance; and 3) rectifier shunt input capacitance. Furthermore, we replace the RF circuit with an artificial neural network (ANN) model to speed up the simulation. The prototype chip for the 2.4-GHz RFEH interface fabricated in a 65-nm CMOS exhibits > 97% MPPT accuracy. The low-power design facilitates the highest sensitivity (−28.5 dBm) and efficiency (10.4% at −20 dBm PIN) among the compared works with single-input rectifiers. In addition, it shows near-consistent efficiency across varying temperatures.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 2

Talk #24.3 / 16:15-16:40

张兆博

南方科技大学

张兆博，2017 本科毕业于南方科技大学微电子科学与工程专业，2023 年获得澳门大学电机及电脑工程博士学位。2024 年至今在茂睿芯（深圳）科技有限公司担任模拟 IC 设计工程师。张兆博主要研究方向为射频能量收集，DC-DC 转换器，参考电压源等。

TALK

A High-Effieiency Low-Cost Multi-Antenna RF Energy Harvesting System With Leakage Suppression

This article presents a multi-antenna RF energy harvester (MARFEH) with leakage suppression to achieve high output power and avoid the effects of interference and blind spots in the room, and all the RF rectifiers sharing only one buffering capacitor to achieve low cost. The proposed leakage-suppressed rectifier utilizing adaptive VTH compensation (AVC) and an RF switch can achieve self-turned off operation to prevent power leakage due to power imbalance among all the parallel-connected rectifiers. The RF harvester also exhibits maximum power point tracking (MPPT) and a 1.8-V regulated output through a boost DC-DC converter. The MPPT is realized by an optimized on-chip Perturb and Observe (P&O) controller and achieves sub-μW system control power consumption. Meanwhile, MPPT is used to estimate the RF input power to drive the AVC circuit to improve rectifier efficiency and assist in leakage suppression. The chip prototype was designed in a 180-nm CMOS process and occupies an area of 0.89 mm2. Using a single antenna with AVC and MPPT enabled, the proposed harvester achieves a power conversion efficiency (PCE) of about 37% and 38% at an input power of -10dBm and +4dBm, respectively. The measured peak PCE is 44% at -0.3dBm. Wireless tests show that the peak output power at different test conditions is significantly improved when the number of antennas increases from 1 to 2 and to 3. Furthermore, an accurate rectifier model is presented to significantly shorten the system simulation time of the rectifier-DC-DC two-stage topology.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #25.1 / 15:25-15:50

周杰

电子科技大学

周杰，博士、电子科技大学讲师。研究方向主要为硅基全集成相控阵系统及其电路模块、无源电路组件等。现已发表 IEEE 高水平收录论文 40 篇，含：JSSC、TCAS-I、MWCL、ISSCC、IMS、RFIC、CICC 等。授权专利 4 项(含欧美专利 2 项)。曾获 IEEE MTT 学会 Undergraduate/Pre-graduate Scholarship Award。兼任 IEEE TCAS-I/II、MWCL 等期刊审稿人。

TALK

A Phase-Modulation Phase-Shifting Phased-Array Transmitter With Phase Self-Calibration and Deep PBOs Efficiency Enhancement

In this article, a digital phase-modulation (PM) phase-shifting (PS) phased-array transmitter is proposed. Both PM and PS are implemented in a PS modulator. Meanwhile, a self-calibration loop is introduced in the PS modulator for improved phase linearity and minimized phase error. The phase control voltages for the PS modulator are generated from the self-calibration loop based on the output signals and reference signals. To reduce the calibration time, a capacitor-array-based state store memory is introduced in the self-calibration loop. Efficiency at 2.5-/6-/12-dB power back-off (PBO) is enhanced by class-G Doherty switched-capacitor power amplifier (SCPA). As a verification of the concept, a 2.1–2.9-GHz four-element phased array transmitter is designed and fabricated in a conventional 40-nm CMOS technology. The transmitter features a 10-bit fast locking phase self-calibration with measured 0.4◦ rms phase error and 0.2-dB rms power error. The measured peak saturated output power of each element is 26.95 dBm at 2.4 GHz. Besides, the measured system efficiency at 0-/2.5-/6-/12-dB PBO is 37.25%/34.24%/30.12%/21.23%. For 20-MHz 64-QAM/15-MHz 256-QAM modulation signal, it exhibits EVM of 4.65%/2.84%, average output power of 19.91/16.59 dBm, and average system efficiency of 24.12%/19.21% at 2.4 GHz. By connecting monopole antenna units with a gain of 4.21 dBi, the measured peak effective isotropic radiated power (EIRP) of phased-array transmitter is 42.05 dBm.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #25.2 / 15:50-16:15

丰光银

华南理工大学

丰光银，新加坡南洋理工大学博士，华南理工大学微电子学院副教授、博士生导师，担任广东省智能通感融合芯片重点实验室常务副主任，兼任鹏城实验室博士生导师；主持或参与国家重点研发计划青年科学家项目、国家自然科学基金联合重点项目、国家自然科学基金面上项目、广东省重点研发计划项目、广东省自然科学基金面上项目等 10 余项；专注于硅基毫米波前端芯片设计、高能效收发机架构等方面的理论和技术研究，发表 SCI/EI 论文 70 余篇，包含 3 篇集成电路领域顶级期刊论文 JSSC，1 篇顶级会议论文 ISSCC；授权中国发明专利 11 项，美国发明专利 1 项，科研成果转化 1 项；曾获新加坡经济发展局集成电路设计专项奖学金、粤港澳大湾区高价值专利培育布局大赛银奖；所指导的学生荣获 RFIT2024、GSMM2024 等国际学术会议最佳学生论文奖、中国国际大学生创新大赛（2024）国赛金奖。

TALK

Silicon-Based Wideband Low-Noise Amplifier for mm-Wave Wireless Communications

Due to the large available spectrum, mm-Wave wireless communications have attracted great attention both from academia and industry. As the first active circuit in a receiver chain, LNA's performances such as bandwidth, noise figure, gain, and linearity, play a crucial role in determining the performance of the overall system. In this talk, we will discuss a broadband LNA based on a tri-coupled transformer (XFMR) for enhanced noise cancelling. In contrast to conventional noise-cancelling structures, the proposed design utilizes the combination of a single transistor and a tri-coupled XFMR innovatively to achieve noise reduction, Gm boosting, as well as wideband matching, simultaneously. Besides, a pole-tuning technique for bandwidth extension will be covered in this talk.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #25.3 / 16:15-16:40

高立

华南理工大学

高立，华南理工大学教授，国家级青年人才，小米青年学者。主要从事射频毫米波电路芯片及系统设计的研究。2020 年在加州大学圣地亚哥分校获得博士学位，师从美国工程院院士 Gabriel Rebeiz 教授。2020-2024 先后在联发科美国公司和苹果公司担任射频芯片高级工程师，参与研发了联发科公司第一款 5G 毫米波商业芯片并大规模量产。2024 年加入华南理工大学微电子学院。研究成果发表论文 50 余篇，谷歌学术引用 2000 余次，H 因子 25。

TALK

A Compact Millimeter-wave Reconfigurable Dual-band LNA with Image-rejection in 28-nm Bulk CMOS for 5G Application

This paper presents a reconfigurable dual-band low noise amplifier (LNA) for 5G millimeter-wave (mmWave) applications in the TSMC 28-nm bulk CMOS process. The reconfigurable LNA is based on a two-stage amplifier design with switchable triple-coupled transformer and capacitor technologies applied to the inter-stage and output matching networks. The switchable triple-coupled transformer can change the self-inductance of the transformer coils by tuning the magnetic flux entering the coils. To suppress image frequency interference, magnetic-electric hybrid coupling is integrated into the inter-stage matching network, which introduces a transmission zero, resulting in a high image rejection ratio. The measured result shows the low band has a peak gain of 18.1 dB with a 3 dB bandwidth of 23.8-33.5 GHz and the high band has a peak gain of 18.9 dB with a 3 dB bandwidth of 34.4-41.4 GHz. The image rejection ratio is better than 32.7 dBc with an intermediate frequency of 8 GHz. The measured NF is better than 3.5 dB at both bands. The IP1dB is -19 to -15.1 dBm / -18.5 to -15.2 dBm in the low/high band. The fabricated LNA has a very compact core size of 0.09 mm2, and the total power consumption is only 14 mW.

2025 年 3 月 28 日 · 第 3 天

大宴会厅 3

Talk #25.4 / 16:40-17:05

杨秉正

电子科技大学

杨秉正，电子科技大学“百人计划”特聘研究员、博士生导师。主要研究方向为射频、微波、毫米波、太赫兹功率放大器、发射机等集成电路设计。发表集成电路、微波领域 IEEE JSSC、TMTT 等 IEEE 期刊论文及 IEEE ISSCC、CICC、RFIC、IMS 等国际会议论文 20 余篇。授权欧美专利 2 项，授权中国发明专利 2 项。曾获 2021-2022 IEEE SSC-Society Predoctoral Achievement Award、2021 IEEE MTT-Society Graduate Fellowship Award 等奖项。

TALK

A 56-to-64GHz Linear Power Amplifier with 30.2dBm Psat and 23.5% PAEpeak Using Scalable Matched-Zone-Expanding Radial Power Combining with EM-Loss Reduction in 40nm Bulk CMOS

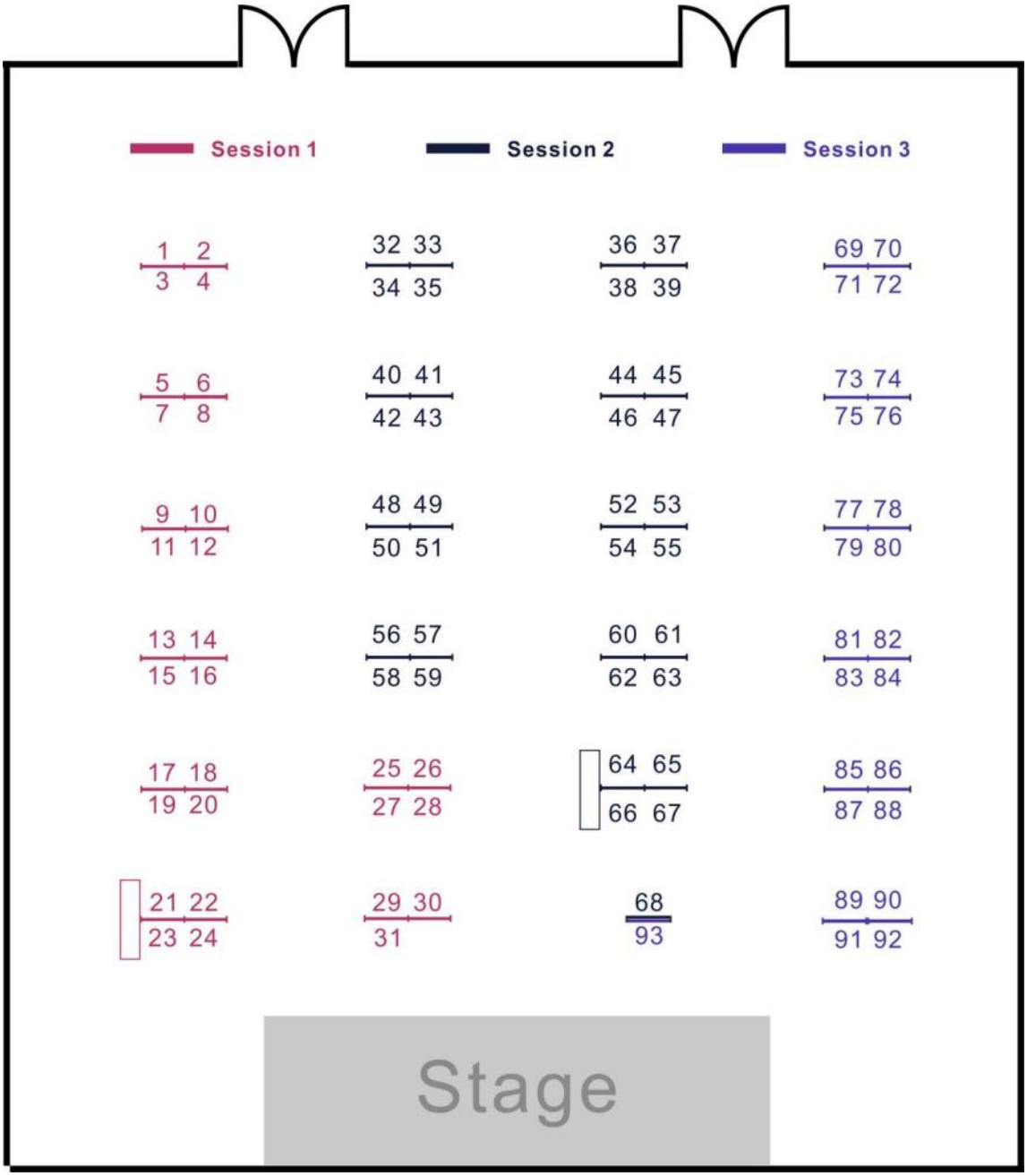
A 56-to-64GHz linear watt-level power amplifier is proposed in this work using scalable matched-zone-expanding techniques with EM-loss-reduced radial power combiner in 40nm CMOS process. The proposed PA demonstrates a small-signal gain of 23.5dB, a 3dB S21 bandwidth from 56 to 64GHz. The large-signal continuous-wave test shows 30.0/30.2dBm Psat with 23.5/23.1% peak PAE and 27.7/28.9dBm OP1dB with 16.0/20.4% PAE at 58/60GHz, respectively. It can also support maximal 9.6Gb/s 64QAM signals.

POSTER SESSION 学生海报展示

2025 年 3 月 26 日 18:30-21:00

大宴会厅 1

Session 1: Analog, Sensors and Data Converters P01-P31	**玫红色区域**
Session 2: Digital and Power P32- P68	**深蓝色区域**
Session 3: RF, Wireless and Wireline P69-P93	**蓝紫色区域**



Session 1: Analog, Sensors and Data Converters

P01 海报题目：**A 1920×1080 Array 2-D/3-D Image Sensor With 3-μs Row-Time Single-Slope ADC and 100-MHz Demodulated PPD Locked-In Pixel**

报告人：陈全民，天津大学

指导老师：徐江涛

摘要：This article presents a 1920×1080 array 2D/3D image sensor with 3μs row-time single-slope ADC (SSADC) and 100MHz demodulated locked-in pixel. To obtain reliable depth information, a backside-illuminated 6μm×6μm PPD pixel with high built-in electric field is used to accelerate charge transfer. Storage diodes are designed to collect demodulated electrons for correlated double sampling readout. The 2-tap pixel and differential multiplexing readout architecture realize both image modes (2D and 3D) working with full-HD resolution. To overcome the limitation of quantization speed in conventional structures, we introduce a 4-bit time-to-digital converter (TDC) into the 8-bit SSADC for residual information quantization, achieving 3μs row-time and 12-bit readout accuracy. In addition, we have proposed a detection and correction circuit in the data stitching process, which resolves error code problem. The common-mode output of two different taps is removed through full differential readout for the background light cancelling. A prototype chip is fabricated in a 110-nm BSI CIS process. The designed PPD enabled a low depth noise of under 0.43% over the range of 0.3–1.5 m, with a modulation frequency of 100 MHz. By adopting the high-speed SSADC, the 2D and 3D frame rates achieve 300fps and 60fps, respectively.

P02 海报题目：**A 28nm 8-Bit 16-GS/ DAC With >60dBc/>40dBc SFDR up to 2.3GHz/5.4GHz Using 4-Channel NRZ-Output-Overlapped Time-Interleaving**

报告人：陈思皓，清华大学

指导老师：杨华中

摘要：This paper validates in silicon a four-channel nonreturn-to-zero (NRZ) output-overlapped (OO) time-interleaving (TI) digital-to-analog converter (DAC) for the first time. The proposed 4-ch TI DAC achieves a sampling rate (Fs) of 16-GS/s, with each sub-DAC operating at a speed of only Fs/4. Compared with conventional RZ structures, the proposed structure uses fewer clocks and avoids the use of high-speed clocks. Additionally, the output-overlapping design reduces DAC's sensitivity to dutycycle mismatches. The DAC was fabricated in 28nm CMOS, incorporating a low-complexity phase error correction (PEC) unit to ensure precise phase alignment for the sub-DACs. Experimental results demonstrate that this DAC achieves a spurious-free dynamic range (SFDR) of >60dBc (>40dBc) up to 2.3GHz (5.4GHz), representing a significant advancement over the state-of-the-art solutions within the 2.3GHz frequency range of interest.

P03 海报题目：**An Easy-Drive 16MS/s Pipelined-SAR ADC Using Split Coarse-Fine Input Buffer Sampling Scheme and Fast-Robust Background Inter-Stage Gain Calibration**

报告人：陈卓毅，北京大学

指导老师：沈林晓

摘要：This work presents an easy-drive 16MS/s Pipelined-SAR ADC with split coarse-fine input buffer sampling scheme, enabling high linearity from DC to Nyquist for rail-to-rail operation. It also introduces a

fast, PVT-robust background inter-stage gain calibration using offset cancellation and metastability detector with probability control. The ADC achieves 79.4dB SNDR and 99.4dB SFDR at Nyquist, corresponding to FoMs of 176.3dB and 13.3fJ/conv.-step FoMw with the integrated input buffer.

P04 海报题目：**A 0.0045 mm2 31.5uW 312.5kHz-BW 2nd-Order Noise-shaping SAR ADC with a Dynamic-BulkSwitching Single-Transistor Amplifier**

报告人：崔佳佳，北京大学

指导老师：沈林晓

摘要：This paper presents an area-compact noiseshaping (NS) SAR ADC with a 2nd-order error-feedback (EF) loop filter, which features a power-efficient single-transistor amplifier (STA) with a dynamic-bulk-switching scheme. The prototype chip achieves 76dB SNDR over a 312.5kHz bandwidth with a power consumption of 31.5uW from a 0.9V supply, resulting in a Schreier FoM of 176dB and occupying an area of 0.0045mm2.

P05 海报题目：**A 74.3 dB SNDR 3rd-order VCO-Based DSM with built-in Passive Low-Pass Filter in 65nm CMOS**

报告人：丁书群，清华大学

指导老师：唐仙

摘要：This paper presents a voltage-controlled oscillator (VCO)-based continuous-time delta-sigma modulator (DSM) with 3rd-order noise shaping capabilities, adopting only two active VCOs. To address the inherent nonlinearity in the VCO's voltage-frequency characteristic, we propose the inclusion of a passive low-pass filter (LPF) within the DSM loop. This addition significantly reduces the input voltage range of the first VCO and facilitates an additional 20dB/decade noise shaping by setting the LPF's pole to match the DSM's signal bandwidth. Designed and fabricated in a 65 nm CMOS process, the prototype VCO-based DSM demonstrates a signal to noise and distortion ratio (SNDR) of 74.3 dB, a dynamic range (DR) of 81.2 dB, and consumes 318 µW with a signal bandwidth of 200 kHz, achieving a Schreier Figure of Merit (FoMs) of SNDR with 162.3 dB.

P06 海报题目：**A 93.3dB SNDR, 180.4dB FoMs Calibration-Free Noise-shaping Pipelined-SAR ADC with Cross-Stage Gain-Mismatch Error Shaping Technique and Negative-R-Assisted Residue Integrator**

报告人：高继航，北京大学

指导老师：沈林晓

摘要：This paper presents a new method for ADC gain and mismatch error shaping. With the unified multi-stage gain-mismatch error shaping technique, the proposed Pipelined-SAR architecture is free from both errors, therefore can be measured without any off-chip calibration.

P07 海报题目：**Cryo-CMOS Dual-Qubit Homodyne Reflectometer Array With Degenerate Parametric Amplification**

报告人：耿宇杰，电子科技大学

指导老师：王成

摘要：In quantum computers, the quantum state discrimination of the physical quantum bits (Qubits) occupies ~80% of the quantum error correction (QEC) cycle. The RF reflectometry or dispersive readout

determines the Qubit state by monitoring the RF reflection of the attached high-Q resonant tank. Compared to their dc counterparts, the RF reflectometers enjoy a high signal-to-noise ratio (SNR), low drifting, and fast speed. As a result, a high-fidelity, single-shot, scalable reflectometer array based on cryogenic CMOS (Cryo-CMOS) ICs is in demand for the future large-scale Qubit array (10^3~10^6 Qubits). However, the classic Cryo-CMOS heterodyne reflectometers, consisting of MOSFET-based LNA, mixer, and baseband blocks, suffer from high noise temperature and dc power. To address these issues, the Cryo-CMOS parametric circuitry based on varactors is explored. In this article, a dual-Qubit homodyne reflectometer array with 2 RX channels and 1 TX channel is demonstrated. In the RX, the degenerate parametric amplifier (DPA) enjoys a Q-enhanced, λ/2 differential-mode (DM) resonator for the high-gain parametric amplification. The common mode (CM) RF input of DPA interacts with the DM resonator by a nonreciprocal, dynamic mode coupling (DMC). It eliminates the necessity of a circulator and the potential oscillation of DPA. The scalability challenge of the DPA's noise temperature Tnoise versus the environment temperature Tenv is also investigated. In the TX, a current-mode logic (CML) divider with interstate locking and a vector modulator (VM) is implemented to achieve fast modulation for the spur and noise rejection. Measured at 4.2 K, the implemented 65 nm Cryo-CMOS chip presents a 4.5~7 GHz bandwidth, 52 dB peak RF gain, and 78 K noise temperature, and generates a 10 MHz TX pulse train with −22 dBm RF power and 30 dB tunability. It consumes a total dc power of 33 mW.

P08 海报题目：**A 75dB-SNDR 10MHz-BW 2-Channel Time-Interleaved Noise-Shaping SAR ADC Directly Powered by an On-Chip DC-DC Converter**

报告人：龚浩宇，澳门大学
指导老师：冼世荣

摘要：Conventional ADCs require a low-noise power supply from the power delivery network (PDN). The commonly used PDN consists of a DC-DC converter that boosts or bucks the external power source to the desired voltage level and a low dropout (LDO) regulator is required to suppress the ripple from DC-DC. However, the power efficiency of this type of PDN is limited by the dropout voltage of the LDO. Moreover, the DC-DC itself needs to provide a higher voltage output to counteract this dropout voltage and the higher conversion ratio results in a lower efficiency. Therefore, to enhance the power efficiency, this work proposes a 10MHz BW 2-channel time-interleaved noise-shaping SAR ADC (TI-NS-SAR) directly powered by an on-chip boost DC-DC converter for both supply VDD and reference VREF, without using LDO. As the VREF is the most sensitive node of the NS-SAR, the DC-DC's ripple is directly injected into the ADC through VREF causing the performance drop. Some existing techniques can suppress the ripple originated inside the ADCs; like decoupling capacitors, ripple cancellation/calibration techniques in [1], [2], etc. However, they still need a low-noise external VREF. They are not the corresponding solutions to the ripple originating from the external PDN. Therefore, to mitigate the interference to the ADC from the ripple generated by the on-chip DC-DC, this work utilizes proper frequency management and ripple noise shaping technique, based on the co-design of the NS-SAR and the DC-DC.

P09 海报题目：**A 12b 3GS/s Pipelined ADC with Gated-LMS-Based Nonlinearity Calibration**

报告人：古明阳，清华大学
指导老师：孙楠

摘要：This paper proposes a novel PWL nonlinearity calibration technique that digitally extracts the

calibration coefficients in the background through gated LMS filters with adaptive thresholds. A dual-path amplification scheme is also proposed to improve power efficiency and settling accuracy. Using these techniques, a prototype 12b 3GS/s pipelined ADC achieves a 58.8dB SNDR with a 1.5GHz input and consumes 32.5mW with an on-chip background calibration engine. This corresponds to an FoMS of 165dB and an FoMW of 15.2fJ/conv-step.

P10 海报题目：**A 26-GΩ Input-Impedance 112-dB Dynamic-Range Two-Step Direct-Conversion Front-End With Improved Δ-Modulation for Wearable Biopotential Acquisition**

报告人：郝禹植，上海交通大学

指导老师：陈铭易，连勇

摘要：This article presents a high dynamic range (DR) direct conversion front-end (Direct-FE) IC enabling the wearable acquisition of weak bio-potentials superposed onto large motion artifacts (MAs). The prototype IC has been fabricated in a standard 0.18-µm CMOS process. Benefiting from the proposed feedback (FB) two-step direct conversion architecture with an improved Δ -modulation, as well as a novel differential difference amplifier (DDA) and a dynamic-element-matching (DEM) technique, it achieves a peak input range of 3.56 VPP , an input-referred noise (IRN) of 2.2 µVrms , an input impedance of 26 GΩ, and a ±1.8-V electrode dc offset (EDO) tolerance, while consuming only 63-µW power. Compared with state-of-the-art Direct-FEs, the proposed work demonstrates an advanced DR (112 dB) and a competitive FOM DR (175 dB). The prototype IC has been validated based on in vivo experiments, demonstrating its capability for artifact-tolerant wearable bio-potential acquisition.

P11 海报题目：**A 16-bit 10-GS/s Calibration-Free DAC Achieving <-77dBc IM3 up to 4.95GHz in 28nm CMOS**

报告人：黄成宇，清华大学

指导老师：李学清

摘 要 ： This paper presents a current-steering DAC with switching-activity-controlled data-weighted-averaging (SAC-DWA). It utilizes half redundant elements to achieve a controlled switching activity, which can suppress the ISI-induced distortion and shape the mismatch in the meantime. A silicon-verified 16-bit 10-GS/s calibration-free DAC with SAC-DWA is fabricated in 28nm CMOS. Measurement results show that the DAC achieves <-77dBc up to 4.95GHz and > 70dBc SFDR up to 1.95GHz.

P12 海报题目：**A 70dB SNDR 80MHz BW Filter-Embedded Pipeline-SAR ADC Achieving 172dB FoMS with Progressive Conversion and Floating-Charge-Transfer Amplifier**

报告人：黄思语，清华大学

指导老师：揭路

摘要：This work presents a filter-embedded pipe-SAR ADC with 70.1dB SNDR over 80MHz BW. It introduces a progressive conversion scheme that mitigates the speed penalty of the filtering operation, and adopts a dynamic floating-charge transferrer to achieve high-speed, high-efficiency and robust residue amplification. The prototype ADC consumes 4.9mW, achieves a Schreier FoM of 172.2dB, provides >30dB out-of-band suppression for full-scale blockers, and is highly scalable in the clock frequency.

P13 海报题目：**A 160-MHz BW 68-dB SNDR 36.2 mW Continuous-Time Pipelined ΔΣ ADC With DAC Image Prefiltering**

报告人：李珂，澳门大学

指导老师：冼世荣

摘要：This article reports a continuous-time (CT) pipelined delta-sigma (ΔΣ) analog-to-digital converter (ADC) featuring a proposed prefiltering scheme to tackle the DAC image issue. We introduce a fast-shunting route for high-speed DAC image current with a passive RC low-pass filter (LPF) on the quantization (QTZ) path. Together with another LPF on the signal path to align the delay, the CT front-end stage provides a residue signal with a small amplitude and smooth edges, relaxing the linearity requirements on the residue amplifier (RA) and the back-end stage. Specifically, the RC delay in the two LPFs is tracked over process variation, relaxing the signal leakage to the back end. For the back-end stage, we use an all-pass filter (APF) analog delay in a second-order CT cascade of integrators with feedforward (CIFF) ΔΣ modulator (DSM) with an input feedforward path. Such an APF can restore the unity signal transfer function (STF) under the influence of excess loop delay (ELD), thus simplifying the matching requirement between analog and digital domains' transfer functions. Prototyped in a 28-nm CMOS process, the proposed ADC operates with a clock of 3.2GHz, occupying an active area of 0.104 mm 2 . It exhibits a 72-dB dynamic range (DR) and a 68.5-dB peak signal-to-noise-and-distortion ratio (SNDR) over a 160-MHz bandwidth (BW). The modulator consumes 36.2 mW, yielding 165-dB Schreier figure-of-merit (FOMs) based on the SNDR.

P14 海报题目：**Xiling: Cryo-CMOS 18-bit Dual-DAC Manipulator with 4.6μV Precision and 4.1nV/Hz0.5 Noise Co-integrated with the Single Electron Transistor at 60mK**

报告人：李英杰，电子科技大学

指导老师：王成

摘要：This paper presents a 65nm Cryo-CMOS, high-precision (4.6μV), low noise (4.1nV/Hz^0.5), low DC power (60μW) 18-bit dual R-2R digital-to-analog converter (DAC) manipulator, which is integrated with the single electron transistor (SET) at 60mK. The DAC adopts the resistor nonlinearity calibration and ordered element matching (OEM), achieving the measured INL and DNL of ±0.8LSB under a 18-bit resolution. A clear Coulomb diamond of the SET has also been recorded at 60mK.

P15 海报题目：**Artificial Neural Network Based Calibration for a 12 b 250 MS/s Pipelined-SAR ADC With Ring Amplifier in 40-nm CMOS**

报告人：刘斌;寄俊垚，西安交通大学

指导老师：张鸿

摘要：This paper presents a 2-stage pipelined-SAR ADC with artificial-neural-network (ANN) based digital calibration algorithm to calibrate the mismatch error in the 1st -stage capacitive DAC (CDAC) and the inter-stage gain error (IGE) together. Previous ANN-based calibration schemes suffer from excessive power and hardware overhead due to the large number of network parameters. To facilitate hardware implementation, the proposed algorithm only requires N1+1 input parameters (N1 is the resolution of the 1st -stage SAR ADC), in which the overall output of the 2nd -stage SAR ADC is combined into a single parameter. In addition, the ANN utilizes a single-neuron hidden layer with linear activation function to calculate the actual bit weight of the ADC, remarkably reducing the hardware overhead and power

consumption of the calibration circuit. The prototype 12-bit, 250 MS/s pipelined-SAR ADC with "loop-unrolled" architecture is implemented in 40-nm CMOS, in which a ring amplifier with improved bias circuit is used to realize a robust closed-loop gain for residue amplification. With the ANN-based calibration circuit implemented in an FPGA, the calibrated ADC achieves the SNDR of 65.0 dB and the SFDR of 84.0 dB at Nyquist input (124 MHz), with a Schreier figure of merit of 169.0 dB and a Walden figure of merit of 14.0 fJ/conv-step. The ADC core consumes 4.95 mW, with an active area of only 0.013 mm2.

P16 海报题目：**A Robust Near-Zero Power Wakeup Timer With a Hybrid Reconfigurable FLL Directly Powered by Uncertain Harvested Voltage Down to 0.3V**

报告人：刘瑞，南方科技大学

指导老师：呼唤

摘要：Energy-harvesting systems require circuits to operate under ultra-low voltage supplies. Though the batteries are removed, a power management circuit is necessary to ensure a consistent voltage supply. In contrast to the state-of-the-art works, this work proposes a wakeup timer that is directly powered by harvested energy, thus obviating the need for additional power management circuits. In addition, we propose a hybrid FLL with an extended range of operation using digital-intensive architecture. Fabricated in 65 nm CMOS process, the chip consumes a total power consumption of 696 nW under 0.3 V supply. In addition, a temperature coefficient of 29ppm/∘C, and a line sensitivity of 0.95%/V are measured over a temperature/supply range of 0−100∘C and 0.3−0.6 V, respectively.

P17 海报题目：**A 12.2uW 99.6dB-SNDR 184.8dB-FOMs DT Zoom PPD ΔΣM with Gain-Embedded Bootstrapped Sampler**

报告人：栾耀晖，北京大学

指导老师：沈林晓

摘要：This paper presents a Gain-Embedded Bootstrapped Sampler input stage adopted in zoom pseudo-pseudo-differential ADC. It achieves simultaneous subtracting, sampling, and amplifying function, suppresses kT/C noise and relaxes input driver requirements. Segment DEM together with segment digital slope coarse ADC is adopted for power-saving. It achieves 99.6dB-SNDR over 4kHz bandwidth while consuming over 12.2uW, corresponding to a state-of-the-art FOM of 184.8dB.

P18 海报题目：**A 10kHz-BW 24.9μW 90.1dB SNDR Noise-Shaping SAR ADC With Complementary Parametric Amplifiers**

报告人：钱磊，上海交通大学

指导老师：Yan Liu

摘要：Noise shaping successive-approximation-register (NS SAR) analog-to-digital converters (ADC) have shown excellent power efficiency and received popularity in power-constrained designs with high precision requirements, such as IoT sensor instrumentation and brain machine interface. Active or passive quantization error amplification is usually required to realize filter shaping [1–2]. The noise and power consumption of the residual amplifier (RA) become one of the important factors limiting the overall ADC performance. Many quantization error amplifiers already exist for design trade-off between power, area and noise, such as duty cycle amplifiers (DCA) [2], gmR amplifiers [3–4], dynamic amplifiers, floating inverter amplifiers (FIA) [5], capacitors stacking [6], etc. In this work, we propose to use passive differential

complementary parametric amplifier with kT/C noise dominance and near-zero power consumption to form RA. To demonstrate this technique, an 8 -bit ADC is designed. Fabricated in a typical 180 nm CMOS process, the prototype ADC achieves 90.1 dB SNDR over a 10 kHz bandwidth with an OSR of 12.5 and consumes 24.9μ W from a 1.8 V supply voltage, resulting in a SNDR based Schreier FoM of 176.2dB.

P19 海报题目：**A PMOS-Based Deep Cryogenic CMOS Temperature Sensor Achieving a Range from 10K to 410K with a Relative Inaccuracy of 0.5% (3σ)**

报告人：沙英哲，复旦大学

指导老师：刘琦 黄张成

摘要：A PMOS-based deep cryogenic CMOS temperature sensor with an ultra-wide range from 10K to 410K and a low relative inaccuracy of 0.5% is presented. The PMOS threshold voltage is selected as the sensing parameter because of its good linearity and high sensitivity. A linear function of PMOS threshold with temperature-independent coefficients is established using three bias states. To the best of our knowledge, this work is the first CMOS temperature sensor down to 10K.

P20 海报题目：**A 4,100μm2 Wire-Metal-Based Temperature Sensor with a Fractional-Discharge FLL and a Time-Domain Amplifier with ±0.2°C Inaccuracy (3σ) from −40 to 125°C and 45fJ·K2 Resolution FoM in 28nm CMOS**

报告人：石丹，澳门大学

指导老师：李家明

摘要：This paper proposes a wire-metal-based temperature sensor with a frequency-locked-loop (FLL) architecture. The innovations of this work are two-fold: 1) a fractional-discharge scheme by extracting the fractional pulse from the 5-phase voltage-controlled ring-oscillator (VCRO) to shrink the discharge window to 10% of the FLL output, preserving the power budget while avoiding using voluminous resistors; 2) a time-domain amplifier (TDA) with chopping to amplify the output from the sensing front-end, eliminating the dc offset and 1/f-noise induced by the TDA. Fabricated in 28nm CMOS, the 4,100μm2 temperature sensor achieves 3σ inaccuracies (from 30 samples) of 1.5°C/□0.2°C after 1-/2-point trimmings across −40 to 125°C, respectively. Moreover, it achieves an R-FoM of 45fJ·K2 , the best in the state-of-the-art when compared with the resistor-based temperature sensors in the 28/65nm processes.

P21 海报题目：**An 8b 10GS/s 2-Channel Time-Interleaved Pipelined ADC with Concurrent Residue Transfer and Quantization, and Automatic Buffer Power Gating**

报告人：陶云松，清华大学

指导老师：孙楠

摘要：The speed of pipelined ADCs is limited to 3GS/s. This work proposes a high-speed pipelined stage that parallelizes residue transfer and quantization. It uses differential sampling and a source follower to realize the inter-stage gain, which enables the fastest 8b single-channel voltage-domain pipelined ADC running at 5GS/s. With the proposed automatic power gating method, a prototype 8b 10GS/s 2-channel time-interleaved ADC achieves the best FoMw of 22fJ/conv-step among published ADCs over 6GS/s.

P22 海报题目：**A Bridge-Less Hybrid SSHI Rectifier With High Efficiency Over Wide Load Range for Piezoelectric Energy Harvesting**

报告人：王储辉，香港中文大学
指导老师：Ka Nang Leung，郭建平

摘要：As the load deviates away from the maximum power point (MPP), the output power of the current piezoelectric energy harvester with synchronous switch harvesting on inductor (SSHI) drops quickly. To achieve high energy harvesting efficiency under a wide load range, this article presents a hybrid SSHI (H-SSHI) interface circuit for piezoelectric energy harvesting (PEH), combining the advantages of series SSHI (S-SSHI) and parallel SSHI (P-SSHI) techniques. An additional bias-flip estimation strategy has been implemented to mitigate charge loss during light load conditions, thereby enhancing energy harvesting efficiency. Only two on-chip switches are employed for bias-flip operations in addition to an external inductor and storage capacitor. The bridge-less topology can also decrease the flipping loss. The proposed H-SSHI circuit is fabricated in a 0.18- μ m BCD process. A maximum of 974% harvesting improvement is measured compared to the ideal full-bridge rectifier (FBR). Moreover, when both the efficiency enhancement and the load range are considered, this design achieves a figure of merit (FOM) of 76, which proves the significant harvesting efficiency improvement for bias-flip circuits over a wide load range.

P23 海报题目：**A 0.36nW, 820μm2, 32kHz Conduction-Angle-Adaptive Crystal Oscillator in 28nm CMOS for Real-Time Clock Applications**

报告人：王鹏，香港科技大学
指导老师：张奕涵

摘要：32.768kHz (32kHz) crystal oscillators (XO) are widely used in real-time clocks (RTC) embedded in various electronic systems. Their performance is critical in battery-powered Internet-of-Things (IoT) sensor nodes when serving as wake-up timers. Extending the battery life requires an ultra-low power (ULP) XO, as it must stay always-on. It also requires good frequency stability; otherwise, the system has to extend its communication guard times for synchronization, in which power-hungry transceivers need to stay active, leading to extra waste in power [1]. These demands have motivated much recent research to seek alternatives to the classic inverter-based Pierce oscillator, which is simple in design but typically consumes 10~100nW of power [2]–[5]. Pulse-injection XOs (PIXOs) are popular due to their sub-nW power consumption. Their power reduction comes from using a tiny conduction angle in the form of short pulses for class-C-like operations. However, positioning current injections to the optimum timing typically requires generating an accurate delay, making pulse generators area-consuming [6]–[10]. Moreover, these methods cannot initiate the oscillation, as the zero-crossing instants, which are the starting times of the delay, are only available once an oscillation is present. These PIXOs, hence, need to embed separate start-up circuits to build up the initial oscillation, necessitating extra control logic and facing robustness challenges under accidental but strong interferences. A compact and easy-to-use ULP XO remains in demand from the cost-sensitive IoT market.

P24 海报题目：**A Tripolar Stimulator with Return-Electrode-Based Charge-Pack Injection Technique for Charge Imbalance Correction in Spatiotemporal Stimulation**

报告人：吴家磊，天津大学
指导老师：王科平

摘要：The circuit design of a stimulator faces two major challenges when applied in spatiotemporal stimulation: electric field distribution which affects spatial resolution, and current distribution which causes a large offset voltage on charge imbalance. By introducing a return electrode, this paper proposes a tripolar stimulator with the return-electrode-based charge-pack injection technique, which is the first design to achieve high spatial resolution while compensating the offset voltage on charge imbalance within ±7.5mV.

P25 海报题目：**A Sub-1 V 90 dB-SNDR Power/BW Scalable DTDSM Using Low-Voltage Cascoded Floating Inverter Amplifiers in 130 nm CMOS**

报告人：武辛婕，浙江大学
指导老师：虞小鹏

摘要：This paper presents a sub-1V delta-sigma modulator (DSM) with power and bandwidth (BW) scalability for IoT applications. It is built around a fully dynamic and low-voltage floating inverter amplifier (LVFIA). To extend the power and BW scalability of the LVFIA, its relatively supply-independent bias current is auto-controlled by DSM's sampling frequency fs. Dynamic techniques such as auto-zeroing and chopping are applied to achieve low noise. Fabricated in a 130nm CMOS, the proposed sub-1V DSM shows a near-consistent SNDR (~90dB) and linearly scalable power and BW (2.5nW/Hz) over a ×30 scaling range of fs. It achieves Walden FoM and Schreier FoM of 51.3fJ/conv-step and 175.7dB, respectively.

P26 海报题目：**A 320MHz BW NS TD-ADC Assisted C/DT Hybrid Pipelined ADC with SAB-based Residue Amplifying Filter**

报告人：邢凯，澳门大学
指导老师：陈知行

摘要：With the advent of WLAN technologies, over 320 MHz BW and >65 dB DR ADCs become indispensable to support newly developed WiFi standards. Three classic solutions can reach the said targets but involve various compromises (Fig. 1 top). CT MASH ADCs [1] rely on a relatively high OSR (⩾7) as well as NS order to accommodate the adequate noise spectral density (NSD), limiting the energy efficiency. The CT pipeline (PIPE) ADC [2–3] obviates the feedback loop and its 1st stage energy effectively provides preliminary quantization, residue generation, amplification, and filtering. However, the backend CT quantization can be power-hungry [2] [4]. The DT NS pipeline ADC offers a low-power alternative [5] but loses the intrinsic anti-aliasing (AA) ability from its CT counterparts. This work hybridizes CT and DT NS PIPE, gaining the pros from the CT PIPE front-end and DT PIPE backend. Together with the Single amplifier biquad (SAB) - Residue Amplifying Filter (RAF) and NS TD-QTZ, the C/DT PIPE ADC demonstrates superior energy efficiency over CT MASH ADCs with 320MHz BW.

P27 海报题目：**A Compact Low-power 16b SAR ADC using Reservoir-Charge-Redistributed DAC and Configurable Floating-Inverter-Based Comparator**

报告人：袁晨曦，澳门大学
指导老师：陈知行

摘要：Systems-on-chip applications have become imperative for high-precision ADCs with low power consumption and compact silicon area. SAR ADCs exhibit outstanding energy efficiency but necessitate high fidelity and fast settling reference voltages, often consuming considerable power and/or area. To alleviate such overheads, the passive-charge-sharing SAR ADCs have been reported [1][2][3], as shown in Fig.1. However, [1] suffers from a large reservoir capacitor (CREF) to capacitive DAC (CDAC) ratio of 80 for 14-bit resolution, and will further expand to 320 for 16-bit. It also undergoes input-dependent bit weight errors and SNR degradation due to the shared bit capacitor (cap) and reference cap. While [2][3] mitigates such constitutes by separating the bit and reference caps, its CREF/CDAC still limits to ≥8, owing to the shrunken step size. This work proposes a reservoir-charge-redistributed SAR ADC that preserves the high SNR and linearity natures in [2] and decouples the compromise between the quantization step size and the value of CREF in [2][3], thus significantly suppressing the CREF/CDAC to 0.35X. A configurable floating inverter amplifier (FIA) –based comparator is also presented to improve the energy efficiency further and enable a regular 1.2V supply implementation, which is different from 3.3V in [1][2][3]. The ADC achieves an 80.9dB SNDR and 100.3dB SFDR at Nyquist input and consumes 291.7μW power from a single supply at 1MS/s, yielding a 32.1fJ/conv.-step FoMwalden and 173.3dB FoMsch.

P28 海报题目：**A 362-TOPS/W Mixed-Signal MAC Macro With Sampling-Weight-Nonlinearity Cancellation and Dynamic-Amplified Accumulation**

报告人：张冉，澳门大学
指导老师：冼世荣

摘要：This work presents a high energy-efficiency mixed-signal multiply-and-accumulate (MAC) macro in charge-domain for machine learning (ML) systems. It involves crucial features aimed at enhancing energy efficiency, throughput, and area efficiency, namely: 1) a parallel-serial (ParSer) scheme to augment the throughput by parallel input channels and reduce the power via serial analog accumulation rather than digital summation; 2) the weight-independent parallel digital-to-analog converter (DAC) sampling (WIPDS) to cancel weight nonlinearity during sampling and allow for resource-efficient DAC, significantly saving power and area; 3) a high energy-efficiency dynamic amplifier (DA) introduced to improve drivability and counteract attenuation of the serial accumulation, thereby attaining the desired accuracy with relaxed the afterward analog-to-digital converter (ADC) resolution and consequently reducing power consumption; 4) an optimized SAR ADC to reach higher energy efficiency. Fabricated in 28-nm CMOS technology, the prototype exhibits a peak energy and area efficiency of 362 TOPS/W and 3.23 TOPS/mm², respectively.

P29 海报题目：**A 5-MS/s 93.4-dB-DR Three-Step Incremental Zoom ADC with Single Sampling**

报告人：张煊昊，电子科技大学
指导老师：刘佳欣

摘要：The zoom ADC can achieve high resolution with low power by a coarse-fine architecture, but its bandwidth is very limited due to oversampling during the fine ΔΣ conversion. This paper presents a

single-sampling incremental zoom ADC. It addresses the fundamental bandwidth limitation by obviating oversampling while still retaining the merit of noise shaping. It also realizes the efficient three-step conversion with a highly hardware-reused architecture. A prototype ADC is implemented in 28 nm CMOS process. Operating under 5 MS/s sampling rate and 0.9-/1.8-V dual power supplies, it measures 89.5 dB signalto-noise-and-distortion ratio (SNDR) and 93.4 dB dynamic range (DR) with 2.5 MHz bandwidth while consuming 2.36 mW power and occupying 0.19 mm2 area. Overall, this work achieves the competitive SNDR-based Schreier FoM of 179.7 dB and DRbased Schreier FoM of 183.6 dB.

P30 海报题目：**A Fully Dynamic Noise-Shaping SAR ADC Achieving 120dB SNDR and 189dB FoMs in 1kHz BW**

报告人：赵晗，电子科技大学
指导老师：刘佳欣

摘要： High-resolution ADCs with micro power and kHz-level BW have wide applications in portable instrumentation, implantable devices and smart sensors. To enhance flexibility and improve energy efficiency, many systems require duty-cycled operation and expect power scaling with speed. State-of-the-art high-resolution ADC solutions include DSMs, zoom, SAR and noise-shaping (NS) SAR ADCs. The DSM in [1] achieves a high DR of 136dB but limited THD of -116dB, and it consumes high power due to the 4th-order loop filter. The zoom ADC in [2] combining with a coarse SAR and a fine DSM achieves 119.8dB SNR, but it can only process DC signals. The dynamic zoom ADCs [3-5] solve the signal BW issue by updating the reference for DSM, however their energy efficiency is not fully exploited due to over-ranging and low quantization resolution (<5b) limited by DWA. Multi-step SAR ADCs [6,7] can achieve >100dB SNDR by employing residue amplification, but the hardware cost required for gain and capacitor calibrations is non-trivial. NS-SAR ADCs [8-12] can achieve high energy efficiency by introducing noise shaping capability to SAR ADCs, but their SNDRs are limited to around 90~105dB. Besides, most of the ADCs with >100dB SNDR rely on static amplifiers, resulting in high static power.

P31 海报题目：**A 320×256 6.9mW 2.2mK-NETD 120.4dB-DR LW-IRFPA with Pixel-Paralleled Light-Driven 20b Current-to-Phase ADC**

报告人：卓毅，北京大学
指导老师：鲁文高

摘要： Long-wavelength (LW) cryogenic (from 80 down to 40K) infrared focal plane arrays (IRFPAs) are extensively employed because of their sensitivity and rapid response. Readout circuits (ROIC) with high dynamic range (HDR) can significantly improve the signal-to-noise ratio (SNR) of LW-IRFPAs due to enhancement of well capacity. However, neither conventional current-voltage nor current-frequency modulation can avoid analog circuits, making the ROIC susceptible to interference [1-8]. In these ROICs, active analog circuits are usually the primary power consumption item. Moreover, the long data transfer bus with a high swing across the pixels consumes power and introduces crosstalk. To address these issues, an LW-IRFPA architecture with pixel-paralleled light-driven current-to-phase A/D conversion (IP-ADC) is implemented in this work. The key circuit includes: 1) a light-current controlled oscillator (LCO) based modulator for IP-ADC that is powered only by photo current without extra power supply; 2) a phase-reconstruction circuit to enhance low light performance while reducing quantization noise by sub-phase extraction; 3) a pixel-level 20b asynchronous gray-code counter for high equivalent full well

capacity during phase quantization; and 4) a low-swing bus data transfer circuit to reduce transmission power consumption and crosstalk. Overall, this work demonstrates a 320×256, 30μm pixel pitch, 10.55μm wavelength quantum-well infrared photo detector (QWIP) IRFPA. The ROIC used in IRFPA is fabricated in a 0.18μm standard CMOS process. The performance of this IRFPA achieves 120.4dB HDR, 2.2mK noise.

Session 2: Digital and Power

P32 海报题目：**A Heterogeneous TinyML SoC with Energy-Event-Performance-Aware Management and Compute-in-Memory Two-Stage Event-Driven Wakeup**

报告人：董彦池，北京大学

指导老师：黄如

摘要：This paper presents a heterogeneous TinyML SoC with E2p- aware system-level energy management achieving a minimum 3.5μW and 30000× peak-to-idle power ratio. The energy-event-performance (E2P)-aware management utilizes various fully synthesizable monitors to be aware of the runtime status of heterogeneous blocks and hierarchical voltage regulation for MEP search at system level, which gains >28% energy saving compared to single block MEP. A 2-stage CIM-based event-driven wakeup scheme is also developed to reduce the always-on energy by over 87%. The presented TinyML SoC is suitable for edge AI applications with state-of-the-art low-power features.

P33 海报题目：**An Energy-Efficient Unstructured Sparsity-Aware Deep SNN Accelerator With 3-D Computation Array**

报告人：方潮铭，西湖大学

指导老师：Mohamad Sawan，杨杰

摘要：We designed an energy-efficient deep spiking neural network accelerator chip that leverages a three-dimensional computing array and unstructured sparsity acceleration. This design has undergone a series of optimizations targeting cutting-edge spiking transformer and spiking ResNet network structures. It has been validated through tape-out with the 40nm CMOS, achieving an energy efficiency of 0.078 pJ/SOP, while also achieving a 77.6% accuracy rate for ImageNet image recognition, which is the best level among similar works.

P34 海报题目：**A 28nm 4.35TOPS/mm2 Transformer Accelerator with Basis-vector Based Ultra Storage Compression, Decomposed Computation and Unified LUT-Assisted Cores**

报告人：黄宗乐，清华大学

指导老师：刘勇攀

摘要：The area-efficient Transformer accelerator exploiting matrix redundancy is presented with four features: 1) A proposed basis-vector decomposition sparing 25.5x model storage for Transformer like Bert-Base, allowing full on-chip inference on devices with about 13MB memory like smartphones, at only 1.28% accuracy loss. 2) An area-efficient self-programming LUT-assisted computing cell by result prefetch; 3) A unified task-insensitive core supporting fast decomposed computing, resulting in a remarkable 73% energy saving; 4) A NoC design facilitating hybrid data reuse to reduce communication. It achieves 4.35 TOPS/mm2 dense area efficiency, 4 times than the state-of-the-art counterpart at same fabrication level. It also demonstrates 213%-429% higher overall energy efficiency.

P35 海报题目：**A 512-nW 0.003-mm2 Forward-Forward Closed Box Trainer for an Analog Voice Activity Detector in 28-nm CMOS**

报告人：黎俊德，澳门大学

指导老师：于维翰

摘要：Analog Voice Activity Detector (VAD) is a promising candidate for a power and cost-efficient solution for AIoT voice assistants. Regrettably, the PVT variation from the analog circuits and data misalignment from sensors limit the VAD accuracy with conventional back propagation model-based training(BPMBT). This brief presents a forward-forward closed box trainer (FFBBT) for analog VADs. It trains the analog circuit without knowing the circuit model or finding its gradient. Thus,it is insensitive to PVT variation and offset, achieving a measured VAD accuracy improvement of ~3% and an accuracy variation reduction of 5.6×. Moreover, a Tensor-Compressed DerivativeFree Optimizer (TCDFO) is also proposed to reduce the require dmemory for FFBBT by 1600×. The FFBBT with TCDFO issynthesized in 28 nm CMOS with a power of 512 nW and an area of 0.003 mm2.

P36 海报题目：**SLAM-CIM: A Visual SLAM Backend Processor With Dynamic-Range-Driven-Skipping Linear-Solving FP-CIM Macros**

报告人：李梦洁，复旦大学

指导老师：曾晓洋

摘要： Simultaneous localization and mapping (SLAM), a pivotal technology in robotics, autonomous vehicles, and surveillance, has gained prominence with the emergence of edge intelligence. Developing energy-efficient, low-latency SLAM systems is essential due to resource constraints and real-time demands. Compute-in-memory (CIM) architectures have been proven to be efficient for matrix multiplications. However, applications for SLAM raise new challenges in memory access and computation aspects: the linear system solving (LS) requires row transformation and causes frequent CIM updates, while the backend optimization causes redundant memory access; back-end optimization dominates SLAM's computation and requires high precision and high dynamic range. Thus, we propose SLAM-CIM, a visual SLAM backend processor for edge robotics. A dynamic-range-driven-skipping CIM macro is designed to realize energy-efficient floating point (FP)-multiply-and-accumulate (MAC) operations. A preconditional-conjugate-gradient-based in-memory linear solver (PILARS) is designed to achieve LS without additional row transformations. This reduces memory access by 2.08× and linear-system-solving latency by 3.84×. SLAM-CIM further minimizes CIM weight updates through incremental bundle adjustment (BA), increasing average CIM utilization by 2.8×. A silicon prototype is fabricated using 28-nm CMOS technology. The measurements show that SLAM-CIM achieves accurate and efficient SLAM operations with an average energy efficiency of 31.53 TFLOPS/W.

P37 海报题目：**Pro-Cache-CIM: A 28nm 69.4TOPS/W Product-Cache based Digital-Compute-in-Memory Macro Leveraging Data Locality Pattern in Vision AI Tasks**

报告人：李响，清华大学

指导老师：刘勇攀

摘 要： Digital-based compute-in-memory macros (DCIM) that leverage lookup tables (LUT) have demonstrated remarkable advantages in achieving high energy efficiency while maintaining full precision. By pre-computing summation results, LUT-based DCIMs eliminate the energy consumption of one or two

stages of addertrees. However, scaling these LUT-based DCIMs to higher orders—which requires using wider bit-widths for indexing LUT content—poses significant challenges. This is primarily due to the exponential growth in the combinations of pre-computed results, which consequently leads to proportional increases in area and power consumption, ultimately degrading both area and energy efficiency. This work leverages the data locality pattern observed in vision AI tasks to overcome the scaling limitations of LUT-based DCIMs. In such tasks, the activations (ACT) within small regions tend to fall within a narrow range. With the weight-stationary dataflow of typical CIMs, we can replace the large and inefficient LUT memory with a small, efficient cache that stores the products of ACTs and WTs. However, applying the product-cache to DCIMs presents several challenges: (1) The multipliers needed for handling cache misses result in significant power and area overhead; (2) The inherent high parallelism of DCIMs leads to a considerable stall rate, as the cache miss of any single channel can cause the entire CIM macro to stall. To tackle these challenges, this paper introduces a product-cache based DCIM macro featuring three key components: (1) A product cache-based multiplier that leverages the data locality of ACTs and the stationary property of WTs to cache their products, achieving enhanced energy efficiency; (2) A shared single cycle booth16 multiplier that replaces 32 booth4 multipliers with 8 1W2R-6T-SRAM-based booth16 multipliers, significantly reducing power and area overhead; (3) A PRE3 cache controller (preload, pre lookup, pre-update) that anticipates future misses and preemptively updates the missed products, leading to improved overall throughput by minimizing stall cycles.

P38 海报题目：**A 98.5% Peak Efficiency 2/3-Phase Buck-or-Boost Converter With VCR-Independent Loss Optimization and Unconditional RHP Zero Elimination Achieving 2.76A/mm2-Current-Density and 6.5μs Recovery**

报告人：李昕蔓，澳门大学
指导老师：江洋

摘要： We propose a Li-ion battery power profile-friendly buck-or-boost converter with 2/3 phase operations to achieve always optimized Pcon in buck and unconditional RHP zero elimination. Our design supports up to 6A IOUT, resulting in an on-chip current density of 2.93A/mm2. The measured peak conversion efficiency is 98.5%. Due to the topology property, our converter achieves a fast recovery time of up to 6.5μs when a 1A load step occurs with a rise time of 20ns.

P39 海报题目：**A 28 nm 0.25-0.61 mW 31-60fps Versatile SoC for Diverse Extreme Edge ML Workloads with Flexible Hetero-Fabric Dataflow Orchestration and Compute/Storage-Density-Adjustable CIM**

报告人：李耀雷，清华大学
指导老师：刘勇攀

摘要： This work presents an ultra-low power versatile SoC for diverse extreme edge ML workloads. It has four key features: 1) Hetero-fabric and flexible dataflow orchestration co-design to achieve high utilization of the compute-in-memory (CIM) core and digital core (Dcore) with reduced L1 memory access. 2) Performance-balance-aware DVFS enabling layer-wise adjustable clock frequency ratio of CIM and Dcore for further power reduction. 3) A reconfigurable-LUT-based CIM macro with dynamic adjustable compute and storage density to fit the varying layers of neural network models. 4) A multi-operator-fused unified Dcore, where various operators can all be uniformly implemented on the multiply-accumulate-based

reconfigurable PEs. The fabricated 28nm chip achieves 7× higher SoC energy efficiency compared with the state-of-the-art tinyML SoC. It supports diverse extreme edge applications and various tinyML models, achieving practical performance (e.g., no less than 30fps) with no more than 0.5mW power on all tasks of MLPerf Tiny while meeting the quality target.

P40 海报题目：**An 85-264Vac to 3-4.2Vdc 1.05W Capacitive Power Converter with Idle Power Reduction and 4-Phase 1/10X SC Converter Achieving 5.11mW Quiescent Power and 78.2% Peak Efficiency**

报告人：刘刚，南方科技大学

指导老师：姜俊敏

摘要：This work presents an 85-264Vac to 3-4.2Vdc Capacitive Power Converter with a fully integrated power stage in a .18μm HV SOI process. This converter improves output power due to the increased AC-DC output voltage using a 1/10X SC converter. Three operating modes are proposed to reduce the AC-DC output voltage ripple. A smaller capacitor can be used to improve the power density of this system. Two capacitors in series with two LDMOS are added to reduce idle power to generate zero waves. This power converter achieves 1.05W output power, 5.11mW idle power reduction, and 78.2% peak efficiency with a chip area 2.71mm2.

P41 海报题目：**A 28nm 4.05μJ/Encryption 8.72kHMul/s Reconfigurable Multi-Scheme Fully Homomorphic Encryption Processor for Encrypted Client-Server Computing**

报告人：卢思佳，清华大学

指导老师：刘雷波

摘要：Fully homomorphic encryption (FHE) allows arbitrary encrypted computation on ciphertexts, enabling privacy-preserving machine learning (PPML) applications. However, the several orders of magnitude slowdown and memory expansion brought by FHE hinder its applicability, necessitating domain-specific accelerators. This work presents an energy-efficient 4.05μJ/Encryption FHE processor with architecture-circuit optimizations to achieve 8.72kHMul/s in throughput to address this issue. Combining both circuit-level techniques and architectural optimizations, the proposed chip achieves the highest throughput for NTT among fabricated FHE accelerators with the highest area efficiency.

P42 海报题目：**A 2.5-A 3-ns-Response-Time Calibration-Free Hybrid LDO Using Scalable Self-Clocked Stochastic Flash-ADC for In-Loop Quantization**

报告人：吕天睿，中山大学

指导老师：郭建平

摘要：This paper presents a dual-loop hybrid low-dropout regulator (LDO) to resolve the conflicts between transient response and load capability. At the digital end, a scalable stochastic flash analog-to-digital converter (SF-ADC) performs fast loop control based on Gaussian-distributed input offset voltage (V_{OS}), enhancing load transient response while reducing circuit complexity. In the analog loop, a fully differential error amplifier (EA) is implemented to suppress the nonlinearity of the SF-ADC, resulting in a fine-regulated output with a 1.67mV/A load regulation. Moreover, the SF-ADC and the power gates (PGs) are implemented with digital standard cells only, being free of external clocks and extra calibrations. Fabricated in a 65-nm CMOS process, the proposed LDO achieves 2.5-A maximum load current ($I_{L,MAX}$) within an active area of 0.127 mm2. Under a 1.3A/0.8ns current up-stepping, the LDO achieves a 3-ns

response time, and the measured output droop (V_{DRP}) is 127 mV.

P43 海报题目：**A 30-110V Resonant Buck-Boost Power-Bus Charger Achieving 50-A Peak Laser-Current Pulse Generation in 2ns for MHz-Frequency Automotive LiDAR Transmitter**

报告人：马航枭，澳门大学
指导老师：江洋

摘要：This work present a resonant buck-boost power-bus charger that can regulate a 30-110V supply from a nominal 48V (supporting 40~60V) automotive power source and support an IDL,pk of 50A with a full-width half maximum pulse-width of 2ns. The VBUS can recover to 110V in 272ns and 90V in 250ns after bus discharge, backing MHz-frequency LiDAR transmitter operations. Under a VBUS of 90V and an IDL,pk of 46A, the proposed solution reduces system power by 43%.

P44 海报题目：**A Cross-Coupled Hybrid Switched-Capacitor Buck Converter With Extended Conversion Range and Enhanced DCR Loss Reduction**

报告人：马乔博，澳门大学
指导老师：江洋

摘要：This article presents a hybrid switched-capacitor (SC) buck converter designed to optimize the reduction in inductor average current (IL,DC) across a wide voltage conversion ratio (VCR) range for Li-ion battery-powered systems. The proposed topology is bases on a modified dual-path (DP) hybrid power stage structure and elevates the inductor de-energizing voltage to enhance IL,DC reduction. With a dual-branch interleaved cross-coupled structure, it reduces the required number of SC cells, thereby lowering costs. Moreover, the converter attains a seamless switching-phase transition around VCR of 0.5, ensuring smooth operations and simplifying control complexity. A stable efficiency is maintained across the entire VCR range by balancing inductor DC resistance (DCR) loss and switch/path conduction loss. In the circuit design aspect, a two-quadrant level shifter (2QLS) is proposed to meet power switch driving requirements in a positive-negative wide-range floating domain. Fabricated in a 180-nm BCD process with a 4.42 mm2 chip area, the converter prototype attains a peak conversion efficiency of 91% when converting a 2.7 ~ 4.2 V input to a 1 ~ 1.8 V output. It delivers a maximum load current of 4.2 A using two 4.7- μ H inductors with 175 m Ω DCR in 16.7 mm3 each and achieves an average efficiency of 90% with only 1.5% variation.

P45 海报题目：**A Fully Integrated 48-V GaN Driver Using Parallel-Multistep-Series Reconfigurable Switched-Capacitor Bank Achieving 7.7nC/mm2 On-Chip Bootstrap Driving Density**

报告人：穆旭初，澳门大学
指导老师：江洋

摘要：This work presents a fully integrated switched-capacitor (SC) floating-domain gate driver with enhanced driving capability and reduced charge-sharing loss. The proposed driver employs a reconfigurable SC bank (RSCB) to achieve multistep gate driving and minimized bootstrapping capacitance (CBST) area cost. An autonomous switching control determines the reconfiguration of the proposed RSCB by comparing the sensed gate-to-source transient voltage with a triggering level. Fabricated using a 180-nm SOI BCD process, the prototype supports a switching frequency of up to 6MHz and a 48V input for a half-bridge GaN testbench, occupying only 0.048mm2 of on-chip bootstrap

capacitance. The measured delivered gate charge over the CBST area reaches up to 7.7nC/mm2, making a 38-fold improvement over conventional techniques, also achieving a 16.2 times reduction in the required CBST area compared to prior designs when driving the same power devices.

P46 海报题目：**A 27.9-mW 802.15.4/4z 1T2R Transceiver With FIR-Embedded Quadrature Hybrid Correlation and AoA Localization**

报告人：聂云昭，清华大学

指导老师：李宇根

摘要：This article presents an IEEE 802.15.4/4z ultra wideband (UWB) transceiver architecture that employs a finite-impulse response (FIR)-embedded quadrature hybrid cor relation (QHC) method for low power and multipath mitigation.Like a rake receiver, the proposed analog correlator shifts a code instead of a UWB signal with FIR taps to relax the design complexity of an equalizer in the analog correlation. As a result, the power consumption for each FIR tap is reduced by more than ten times. A least-square-error-based FIR algorithm is proposed for the multipath mitigation of a burst position mod ulation (BPM) signal. To validate the proposed FIR-embedded QHC method, an 8-GHz 1T2R transceiver is implemented in 65-nm CMOS. The transceiver supports synchronization, BPM at 0.98/7.8 Mbaud/s, and precise localization. The receiver achieves −102-dBm sensitivity and consumes 12.2 mW/channel, while the FIR circuits consume 5.3% only. The chip supports localization with an rms time-of-arrival (ToA) error of 1.5 cm and an rms angle-of-arrival (AoA) error of 3.8◦ . With the duty-cycled operation, the transceiver consumes 27.9 mW at 0.98 Mbaud/s in the payload field and features the lowest power consumption among HRP-capable UWB transceivers.

P47 海报题目：**A 0.67-to-5.4 TSOPs/W Spiking Neural Network Accelerator With 128/256 Reconfigurable Neurons and Asynchronous Fully Connected Synapses**

报告人：齐翔羿，上海交通大学

指导老师：赵健

摘要：Spiking neural networks (SNNs) are garnering increasing attention due to their potential to explore the complexities of the human brain and utilize its capabilities. The broad spectrum of applications presents challenges in designing SNN-based neuromorphic systems First, the SNN uses complex models [e.g., Izhikevich (IZ)] for brain simulations and simpler models [e.g., Leaky Integrate and Fire (LIF)] for efficient machine learning, presenting a challenge in realizing neuron circuits supporting diverse applications. Second, densely connected networks with uneven spike distributions lead to Network-on-Chip (NoC) congestion and delays, complicating the optimization of throughput/area. An SNN accelerator, featuring 128/256 reconfigurable neurons and asynchronous fully connected synapses, has been developed to address these challenges. The reconfigurable neuron circuit is capable of switching between the LIF neuron model and the IZ neuron model. The proposed chip achieves a peak power efficiency of 5.37 TSOPs/W and throughput of 25.6 MSOPs/s. The near-threshold operation of neurons, in conjunction with asynchronous fully connected synapse, reduces energy by 9.42× to a 9.27 pJ/pixel in image feature extraction.

P48 海报题目：**An 85-230VAC to 3.3-4.6VDC 1.52W Capacitor-Drop Sigma-Floating-SC AC-DC Converter with 81.3% Peak Efficiency**

报告人：宋飞，澳门大学

指导老师：路延

摘要：This work proposes a fully SC-based non-isolated AC-DC converter, fabricated in 180nm BCD process. The topology is optimized for Internet of Things (IoT) and smart home devices to converter a AC mains (110V@60Hz or 220V@50Hz) input to a battery voltage (3.3～4.6V). Sigma-SC rectifier is utilized to reduce the freewheeling current loss and share the output current stress. It reaches a peak efficiency as high as 81.3%, with a maximum efficiency improvement of approximately 8%, compared with previous designs. Floating-SC DC-DC converter is introduced to enhance the output power and the equivalent output decoupling capacitance. With these two proposed approaches, the maximum output power of the AC-DC converter is 1.52W with 739mW/cm^3 power density (BOM).

P49 海报题目：**A 28nm 0.22μJ/Token Memory-Compute-Intensity-Aware CNN-Transformer Accelerator with Hybrid-Attention-Based Layer-Fusion and Cascaded Pruning for Semantic-Segmentation**

报告人：谭雍昊，香港科技大学

指导老师：郑光廷，涂锋斌

摘要：To tackle the heavy memory and computation overheads caused by the long token length in high-resolution semantic segmentation task, which is an vital task in autonoumous driving and relies on hybrid cnn-tranformer model. In this paper, we propose a hybrid attention mechanism coupled with a KV-weight-reused scheduler to fuse the layers between convolution and attention. Additionally, we introduce a cascaded feature map pruning strategy to achieve unified convolution-attention pruning. Compared with SOTA transformer accelerator, our chip ahieves 52.9TOPS/W energy efficiency and 0.22uJ/token energy consumption.

P50 海报题目：**A 93%-Peak-Efficiency Battery-Input 12-to-36V-Output Inductor-in-the-Middle Hybrid Boost Converter with Continuous Input and Output Currents and Fast Transient with No RHP Zero**

报告人：唐田田，南方科技大学

指导老师：姜俊敏

摘要：This paper presents a battery to 12-36V hybrid boost converter with continuous input and output currents. The proposed design places a small power inductor in the middle and merges a Dickson switched-capacitor converter on the low-voltage side and a dual-branch interleaving SC voltage doubler on the HV side, obtaining high VCR and fast transient with no RHP zero. The converter delivers a maximum output power of 10.8W with a peak efficiency of 93% and a remarkable power density of 49.5mW/mm3.

P51 海报题目：**E-NPU: A 34~126nJ/Class Event-Driven Adaptive Neural SoC with Signal-Dynamics-Aware Feature Clustering and Multi-model In-Memory Inference/Training for Personalized Medical Wearables**

报告人：田丰实，香港科技大学
指导老师：Kwang-Ting Tim Cheng

摘要：We propose an event-driven adaptive neural SoC (E-NPU) for personalized medical wearables, featuring three innovations: a self-adaptive processing architecture with energy-efficient signal-dynamics-aware feature extraction plus clustering, multi-model multi-precision CIM cores for task-aware classification, and inter-core pipelines for direct error feedback on-chip training. These enhancements achieve over 1.7x energy reduction, 95.6%–99.6% accuracy, and 2.49x and 3.41x reductions in latency and external memory access, addressing inter-patient variance and enabling long-term patient-specific medical applications.

P52 海报题目：**A Hybrid-Resonance Single-Stage Dual-Output Rectifier With High Voltage Difference for Wireless Power Transfer System**

报告人：王凡涛，西北工业大学
指导老师：马彦昭

摘要：This paper presents a novel hybrid-resonance single-stage dual-output rectifier designed for high voltage electrical stimulation with a large voltage difference. By leveraging the advantages of series and parallel resonance, a high voltage is generated with parallel resonance and another low voltage is produced with series resonance. Through rigorous mathematical analysis, it is demonstrated that parallel and series resonance achieve higher system efficiency under light and heavy load conditions in most wireless power transmission systems, respectively. Additionally, the parallel resonance can provide readily tens of volts. Therefore, combining series and parallel resonance can improve system efficiency and meet high voltage requirement in electrical stimulations. The overall system utilizes hysteresis control to generate dual outputs with three operational phases, which can switch between parallel and series resonance. In parallel resonance, a zero-voltage detection (ZVD) is adopted to charge the high voltage, and in series resonance, the low voltage is charged using zero current detector (ZCD). The proposed rectifier, fabricated in a 0.18μm BCD process, achieves dual outputs of 20V and 6V with a voltage difference of 14V, approximately 7~8 times higher than traditional single resonant rectifiers. When operating at maximum power of 760mW, the peak efficiency reaches 92.2%.

P53 海报题目：**A 28nm 3.14 TFLOPS/W BF16 LLM Fine-Tuning Processor with Asymmetric Quantization Computing for AI PC**

报告人：王文迅，清华大学
指导老师：刘勇攀

摘要：The work presents an energy-efficient fine-tuning processor designed to support asymmetric quantization for privacy-preserving LLM fine-tuning on AI PCs. It implements a asymmetric quantization computing friendly tensor array and uniform transposition engine covering 4/8/16b transposition, also a 4-bit quantization and semi-structured sparsity to reduce memory access, achieving up to 3.14 TFLOPS/W for BF16*4bit computations and improving energy efficiency by 1.2~1.75x over previous state-of-the-art designs.

P54 海报题目：**A 28nm 17.83-to-62.84TFLOPS/W Broadcast-Alignment Floating-Point CIM Macro with Non-Two's-Complement MAC for CNNs and Transformers**

报告人：王幸，东南大学
指导老师：司鑫

摘要：Previous FP-ClM struggles to balance computation precision with input reusability for large overhead of peripherial alignment circuits. A 28nm broadcast-alignment true FP-CIM fabricated using embedded area-efficient adaptive-alignment scheme and format-mixed N2CMAC flow demonstrated an energy efficiency of 62.84TFLOPS/W and 90.15TOPS/W for both true BF16 and INT8 multiply-and-accumulate (MAC) operations with 100% input reusability and 0.016% accuracy loss of ViT @ImageNet.

P55 海报题目：**SKADI: A 28nm Complete K-SAT Solver Featuring Dual-path SRAM-based Macro and Incremental Update with 100% Solvability**

报告人：吴子涵，北京大学
指导老师：王源

摘要：Boolean satisfiability (K-SAT) is a fundamental problem with wide-ranging applications in domains such as electronic design automation (EDA) and artificial intelligence (AI). However, K-SAT problems(K≥3) are proven to be NP-complete, which makes their resolution in conventional Von Neumann architectures both energy-intensive and time-consuming. Recently, several ASIC-based K-SAT solvers have been proposed as low-cost alternatives. However, these designs are limited to resolving satisfiable (SAT) cases and cannot provide proof of unsatisfiability (UNSAT). This limitation significantly impedes their practical applicability, as the satisfiability of most real-world K-SAT cases is not predetermined, necessitating solvers that can verify the existence or absence of solutions. To address this gap, this work presents a complete K-SAT solver capable of handling both SAT and UNSAT cases. The proposed architecture incorporates several novel features: a dual-path SRAM-based macro enabling bidirectional clause-literal deductions, a position-encoded counter for efficient multi-level clause state tracking, and an incremental update strategy for assignment management. Fabricated using a 28nm CMOS process, the measurement results demonstrate that the proposed solver achieves energy and area efficiencies of 24.8-12.9 TOPS/W and 56.8-227.1 GOPS/mm2 across supply voltage of 0.65-0.9V. Operating at 200 MHz and 0.9V, the solver achieves average solution times of 17.1 μs for SAT cases and 42.1 μs for UNSAT cases, with a power consumption of 3.39 mW. In particular, the solver guarantees 100% solvability for all cases, showing potential for applications such as formal verification and fault diagnosis, where knowing the satisfiability is crucial.

P56 海报题目：**A 300-kHz 3-Level Flyback Converter Achieving 93% Peak Efficiency and 50% Reduction in Transformer Size**

报告人：武远卓，澳门大学
指导老师：黄沫

摘要：This work proposes a 3-level flyback converter with coupled inductors, enabling the use of low-VDS switches, and reducing both transformer size and core loss. The proposed 1 passive-clamp and 1 active clamp (1PC1AC) scheme minimizes power loss while maintaining ZVS in both primary-side switches with only one clamping switch. Working at 300kHz, the prototype achieves maximum 40-W POUT, 93% peak

efficiency, and reduces the transformer size by up to 50%, all at a comparable cost.

P57 海报题目：**A 180-MHz 45.3% Peak Efficiency Isolated Converter using Q-downsize Class-D Power Amplifier with Inherent Shoot-through Current Blocking and High Tolerance for Efficiency Despite Frequency Misalignments**

报告人：夏添，澳门大学
指导老师：黄沫

摘要：This work proposed an isolated DC-DC converter with a Q-downsize transmitter, featuring inherent shoot-though current blocking and high tolerance for efficiency despite frequency misalignments. The Q-downsize technique facilitates 45.3% peak efficiency and maximum 1-W output power, at 180-MHz operating frequency. The high tolerance and symmetrical structure maintain a good EMI performance. This converter meets the CISPR-32 Class-B certification requirements.

P58 海报题目：**A Single Li-Ion Battery Powered Buck Converter with > 90% Efficiency Over 10-μA to 500-mA Loading Range by Utilizing Compensator-Based Built-In Mode Tracking Technology**

报告人：谢依玲，中山大学
指导老师：郭建平

摘要：An ultralow quiescent current dual-mode dc dc buck converter is presented in this article to achieve high efficiency over a wide load range for Internet of Thing (IoT) applications. In medium and heavy load conditions, the valley-current mode (VCM) with adaptive on-time (AOT) is employed to guarantee loop stability and seamless transition between pulsewidth modulation (PWM) and pulse-frequency modulation (PFM). A hiccup mode (HM) is proposed to minimize the power consumption of control circuits in light load conditions. Based on the compensator in the VCM, a built-in mode tracking technology is proposed to achieve the predictable and seamless mode transition without load current sensing circuits. Imple mented in a 0.18-μm BCD technology, the proposed converter has an efficiency higher than 90% over 10-μA to 500-mA loading range within the supply range of a single lithium-ion battery. Under a 2.4–5.5-V input voltage and 0–1-A loading current range, the output ripple is less than 20 mV. When the load current steps from 2.4 μA to 200 mA within 10 ns, the output undershoot is 152 mV.

P59 海报题目：**A 6.78MHz 94.2% Peak Efficiency Class-E Transmitter with Adaptive Real-part Impedance Matching and Imaginary-part Phase Compensation Achieving a 33W Wireless Power Transfer System**

报告人：熊宇豪，西安交通大学
指导老师：耿莉

摘要：This work proposes a Class-E TX with an adaptive real part impedance matching technique and an imaginary part phase compensation controller in a 6.78MHz WPT system, to cope with the real and imaginary part impedance variation. This achieves ZVS and avoids HS and RC loss across the full complex impedance range. Measurement results show the proposed class-E architecture achieves 94.2% peak efficiency in TX and 33W maximum E2E output power in WPT system.

P60 海报题目：**A Segmented-Interlacing Multi-Phase Hybrid Converter with Inherently Auto-Balanced ILs and Boosted IL Slew Rate during Load Transients**

报告人：杨佳成，澳门大学

指导老师：黄沫

摘要：The paper presents a segmented-interlacing multiple-phase hybrid buck converter with inherently auto-balanced inductor currents. Its ability to overlap duty cycle D extends VCR range and achieves >5× instantaneous inductor current slew rate during load step-up transient, compared to conventional 3P4S converter. The segmentation allows for fSW downsizing, enhancing the light-load efficiency. It achieves a peak efficiency of 91.7% and 92.9% at 12-V VIN, 1-V and 1.8-V VO, respectively.

P61 海报题目：**A 25-nA Modified Hybrid Ladder Converter with Efficient Output-Capacitor Charge Recycling and 90% Battery Lifetime Extension**

报告人：杨建新，澳门大学

指导老师：黄沫

摘要：This paper presents a modified hybrid ladder converter that efficiently recycles output capacitor energy during the DVS of loading low-power SoC. It enhances light-load efficiency by RMS current reduction, accurate ZCD, and split-phase control. Adaptive VRAMP scheme greatly reduces IQ without compromising output voltage ripple or transient response. The converter achieves 25-nA IQ, 82.9% efficiency at 1-μA load current, and a maximum 73% energy saving, extending battery life by 90%.

P62 海报题目：**A Bi-Directional Dual-Path Boost-48V-Buck Hybrid Converter for High-Voltage Power-Transmission Cable in Light-Weight Humanoid Robots**

报告人：杨文杰，澳门大学

指导老师：路延

摘要：Thick and heavy cables in humanoid robots account for a certain portion of the total weight. This paper presents a bidirectional dual-path boost-buck converter reusing the parasitic cable inductor for 48V-bus power delivery, to reduce the system weight. Also, the proposed phase alignment scheme greatly reduces the cable current ripple in such high-voltage conversion case. We achieve a peak chip efficiency of 96.7% at 16.5W output, and a maximum transmission power of 45W.

P63 海报题目：**A 4-phase Integrated Voltage Regulator with In-package Inductors Achieving 89.0% Peak Efficiency and 65% Droop Improvement for 6A/2ns Transient**

报告人：袁恺，香港中文大学（深圳）

指导老师：刘寻

摘要：This paper introduces a 28nm, 50MHz, 4-phase integrated voltage regulator (IVR) designed for vertical power delivery to computing processors and GPUs. The proposed IVR utilizes ramp-adjusted current balance to enhance reliability in multiphase operation and employs a multiple-trigger-enabled transient enhancement technique for droop reduction. The IVR achieves an 88mV Vout undershoot for an 6A/2ns transient, respresenting a 65% improvement compared to PWM control alone. The IVR possesses a current density of 7A/mm², attains a peak efficiency of 89%, and maintains an efficiency of up to 83.9% at a 7A load current using in-package, small form factor inductors.

P64 海报题目：**An Up-to-70-V Output Hybrid Boost Converter with Halved Voltage Stress Achieving 7-W Output Power and 73.8% Peak Efficiency at CR of 14**

报告人：张定暄，中山大学
指导老师：郭建平

摘要：This work presents a high-voltage DC-DC boost converter with a Halved-Voltage-Stress (HVS) architecture for applications like LED backlighting and LiDAR. The proposed design uses flying capacitors to reduce voltage stress and inductor current, achieving a high conversion ratio of 14 and peak efficiency of 73.8% at 70-V output. Measured results demonstrate significant improvements over conventional designs in efficiency and output voltage.

P65 海报题目：**A 67μW/Channel, 0.13nW/Synapse/Bit Nose-on-a-Chip for Non-invasive Diagnosis of Diseases with On-chip Incremental Learning**

报告人：张吉霖，清华大学
指导老师：陈虹

摘要：Portable electronic noses (E-noses) are proposed to detect possible pathological changes in the body by analyzing the patient's exhaled gas. As a diagnostic tool for early disease detection, this approach helps to reduce the need for tissue sampling, greatly alleviating pain and discomfort for the patient while avoiding the risk of infection or complications. However, the composition of exhaled gas varies greatly depending on the environment with changing conditions and patients using different devices in different locations (such as hospital, health center, home and so on), which makes the E-nose difficult to maintain a satisfying accuracy in detecting diseases for different patients. Besides, with the increasing demand for intelligence of E-noses, the circuit complexity and the amount of gas data to be processed are constantly growing, as a result, the overall power consumption issue poses a great challenge for power-constrained portable E-noses. To overcome these challenges, we introduce ANP-O: a 67μW/Channel 0.13nW/Synapse/Bit E-nose system including a 16-channel gas sensor array, 16 ADC-free analog front-end circuits, and an asynchronous olfactory processor.

P66 海报题目：**An 80W Single-Inductor DC-DC Architecture for Simultaneous Flash Charging and Dual-Output PoL Supply with 92.1% Peak Efficiency from 15V-to-28V Input to 12.6V/3.3V/1V Outputs Using 1.3mm3 Inductor**

报告人：张雄杰，澳门大学
指导老师：江洋

摘要：This paper presents a high-density DC-DC power delivery (PD) scheme using the proposed synergetic PD architecture (SyPoDA), enabling simultaneous 3-cell Li-ion battery charging under USB PD 3.2 protocol and single inductor dual-output (SIDO) point-of-load (PoL) supplies. The proposed SyPoDA synergizes a switched-capacitor (SC) flash charger with our proposed hybrid SIDO converter, featuring 1) power stage sharing along charging and load-supply paths, 2) constant inductor DC current (IL,DC) reduction at the PoL side, and 3) uninterrupted steady-state SIDO output current. It can improve the utilization of the high-voltage part power stage, reduce the inductor size, and lower the output capacitor (CO) requirement, improving the total power density. In circuit design, we propose a pulse-current-based gate driver (PCGD) circuit for monolithic GD integration. Fabricated in a 180-nm BCD process, the proposed SyPoDA prototype within a total 3D volume of 117mm³ achieves a 92.1% peak efficiency at 42W

total output when converting a 15-to-28-V input to three outputs of 12.6V/3.3V/1V. It supports a maximum output power of 80W.

P67 海报题目：**A 285-nA Quiescent Current, 94.7% Peak Efficiency Buck Converter With AOT Control for IoT Application**

报告人：张玉鑫，西安电子科技大学

指导老师：蔡觉平

摘要：An ultralow quiescent current dc–dc buck converter based on adaptive on-time (AOT) control is presented in this article. To minimize the energy wastage of the dc–dc buck converter circuit when the Internet-of-Things (IoT) device is in standby mode, a control loop with nano-ampere quiescent current is proposed in this converter. To reduce the quiescent current consumed by the voltage reference and improve its line sensitivity (LS), the voltage reference in the proposed converter is preregulated and based on the subthreshold CMOS implementation, with a quiescent current of only 20 nA. Meanwhile, for purpose of maintaining high efficiency of the converter under the ultralow load, an adaptive comparator based on the dynamic bias mode selection circuit is proposed, which converts the load conditions into time information and switches the bias current and gain of the comparator under ultralow loads, and the quiescent current of the comparator is only 65 nA. The proposed converter is implemented in a 0.18-μm BCD process with an area of 1.35 mm2. Experimental results show that the converter has a minimum quiescent current of 285 nA, maintains more than 80% conversion efficiency over a load range of 10 μA–300 mA and a peak efficiency of 94.7%, and has an output of 0.9–4.8 V over a supply condition of 2–5.5 V.

P68 海报题目：**A 6.78MHz Single-Stage Regulating Rectifier with Dual Outputs Simultaneously Charged in a Half Cycle Achieving 92.2% Efficiency and 131mW Output Power**

报告人：庄泉荣，南京大学

指导老师：邱浩

摘要：This work proposed a 6.78MHz single-stage dual-output (SSDO) regulating rectifier for biomedical wireless powering. It was implemented with three NMOS active diodes to minimize power loss otherwise by PMOS. To maximize POUT, dual outputs were charged simultaneously in a half cycle rather than in the conventional time-multiplexing manner. Measurement results verified two regulated voltages at 3.3V and 1.6V. The peak 92.2% ηREC and 131mW POUT were the highest compared to prior SSDO rectifiers.

Session 3: RF, Wireless and Wireline

P69 海报题目：**A Sub-6GHz Wideband Transmitter with LO Harmonic Rejection RF Front-ends Using Frequency-Adaptive Calibration**

报告人：白浩宇，北京大学

指导老师：廖怀林

摘要：This paper presents a broadband 0.1-6GHz transmitter that integrated a 0.1-2.5GHz local oscillator (LO) harmonic rejection (HR) RF front-end (RFFE) based on the LO frequency-adaptive calibration scheme. In the HR-RFFE, a programmable RC network is set to achieve the intermediate frequency domain harmonic rejection and pre-calibration. In the 8-phase LO generator, the cross-connected Gilbert phase

detector provides the detection of the orthogonality of 90° shifted LO signals for the calibration of the LO phase errors due to the frequency variation. The in-phase (I) and quadrature (Q) signals are calibrated separately and summed in the power amplifier. Implemented in 40nm CMOS, the transmitter occupies 1.1 × 1.1mm2. With the baseband and RFFE, the transmitter achieves a gain of over 26dB, a P1dB compression point of 16.1dBm, and a system efficiency of 25.9%, while operating at 0.1-6GHz. With the calibration techniques, the 3rd and 5th LO harmonic rejection ratios are over 46.9 dBc and 53.5 dBc, respectively.

P70 海报题目：**An 18.5-to-23.6GHz Quad-Core Class-F23 Oscillator Without 2nd/3rd Harmonic Tuning Achieving 193dBc/Hz Peak FoM and 140-to-250kHz 1/f3 PN Corner in 65nm CMOS**

报告人：曹瀚璋，南京理工大学
指导老师：吴文，黄同德

摘要：This paper introduces a quad-core Class-F23 VCO with a circular trifilar transformer to extend the differential-mode resonance around the 3rd harmonic and an 8-shape stacked inductor to extend the common-mode resonant peak around the 2nd harmonic. The 65nm-CMOS 18.5-t0-23.6GHz VCO achieves -138.2dBc/Hz phase noise, 193dBc/Hz FoM at a 10MHz offset, a 160kHz 1/f3 corner frequency.

P71 海报题目：**A 56-Gbaud 7.3-Vppd Linear Modulator Transmitter with AMUX-Based Reconfigurable FFE and Dynamic Triple-Stacked Driver in 130-nm SiGe BiCMOS**

报告人：陈福栈，香港科技大学
指导老师：俞捷，潘权

摘要：A linear transmitter with an analog multiplexer (AMUX) and a linear driver is proposed. The AMUX adopts the timing relationship between re-timed half-rate data streams to implement inherent re-configurable feed-forward equalizer (FFE). The linear driver utilizes dynamic triple-stacked topology to achieve large output swing without breakdown. Fabricated in 130-nm SiGe BiCMOS, the linear transmitter achieves 56-Gb/s 7.3-Vppd NRZ and 112-Gb/s 4.2-Vppd PAM-4 outputs.

P72 海报题目：**A 6.5-to-6.9-GHz SSPLL with Configurable Differential Dual-Edge SSPD Achieving 44-fs RMS Jitter, -260.7-dB FOMJitter, and -76.5-dBc Reference Spur**

报告人：陈天乐，中国科学院微电子研究所
指导老师：杨尊松

摘要：A dual-edge subsampling phase-locked loop (SSPLL) is proposed to reduce the in-band phase noise (PN) of the crystal oscillator (XO) and reference buffer (RBUF) by 3dB without degrading frequency resolution. It is able to achieve even and odd locking modes by configuring the dual-edge subsampling phase detector (SSPD) to ensure that the PLL can lock in steps of FREF. With a 100-MHz input reference and 6.5-to-6.9-GHz output, the prototype in 65-nm CMOS achieves an RMS jitter of 44fs, a jitter-power figure-of-merit (FOMJitter) of −260.7-dB, and a spur level of −76.5dBc. The total power consumption is 4.4mW at 6.8GHz.

P73 海报题目：**A 0.0006-mm2 0.13-pJ/bit 9–21-Gb/s Sampling CDR with Inverter-Based Frequency Multiplier and Embedded 1:3 DEMUX in 65-nm CMOS**

报告人：董志成，西安电子科技大学
指导老师：赵潇腾，刘术彬

摘要：This poster presents a 9–21-Gb/s inductorless frequency-multiplying sub-sampling (FMSS) clock and data recovery (CDR) circuit with an embedded 1:3 demultiplexer (DEMUX) for multi-lane serial interfaces. It features a compact design with linear models and theoretical analysis of the FMSS architecture. An inverter-based frequency multiplier in the clock feedback path enables a ring voltage-controlled oscillator (RVCO) and transmission-gated retimers to operate at one-third rates. The primary-secondary sub-sampling phase detector (SSPD) allows full-rate triple-frequency clocks with low swings. The frequency multiplier can suppress in-band noises, while a ~200-MHz loop bandwidth effectively mitigates out-of-band RVCO noises. A duty cycle corrector (DCC) ensures fine retiming deskewing. Fabricated in 65-nm CMOS technology, the proposed CDR, occupying only 0.0006 mm^2, achieves the best-in-class 349-fsrms jitter and 0.13-pJ/bit energy efficiency. A jitter tolerance (JTOL) of 0.34 UIpp is measured at 21 Gb/s with the bit error rate (BER) of less than 10^-12.

P74 海报题目：**A 0.6V Fully-Integrated BLE Transmitter in 65nm CMOS Using a Common-Mode-Ripple-Cancelled Hybrid PLL and a Duty-Cycle-Controlled Class-E/F2 PA Achieving 25% System Efficiency at 0dBm**

报告人：冯礼群，清华大学
指导老师：李宇根

摘要： A 0.6V fully-integrated BLE TX in 65nm CMOS is proposed to achieve high system efficiency with following features: (1) a sub-mW RDAC-based hybrid PLL with common-mode (CM) ripple cancellation to reduce reference spur by 19.6dB; (2) a switching current-source (SCS) D/VCO with a step-up transformer and shared bias resistor for differential varactors to achieve a FoM of 187.2dB with 400μW power consumption; (3) a duty-cycled controlled class-E/F2 digital PA to suppress 3rd-harmonic distortion (HD3) by 12dB without degrading the PA efficiency; (4) a calibration-free 1-bit ΔΣ highpass modulation with FIR filtering to overcome the nonlinearity problem of a low-voltage DCO in two-point modulation. Thanks to the above features, the proposed TX achieves the highest system efficiency of 25.8% at 0dBm output among the TXs with the closed-loop FM modulation. The TX exhibits HD2/HD3 of -50.1dBm/-52.1dBm and satisfies BLE requirements while occupying a compact area of 0.46mm2 without external components.

P75 海报题目：**A Differential Series-Resonance CMOS VCO with Pole-Convergence Technique Achieving 202.1dBc/Hz FoMTA at 10MHz Offset**

报告人：郭晋华，华南理工大学
指导老师：秦培

摘要： Voltage controlled oscillator with ultra-low phase noise is extensively pursued for various applications, such as high-speed wireless/wireline communications, high-speed AD/DAs, etc. In this paper, we present a differential series-resonance VCO topology with a pole-convergence technique. The proposed VCO achieves a PN@10MHz of -152.89dBc/Hz from 9.122GHz, a TR of 17.7% (7.65GHz to 9.135GHz), and a 190dBc/Hz and 202.13dBc/Hz peak FoM and FoMTA at 10MHz offset, and the core area is 0.39×0.49mm2.

P76 海报题目：**A 56 Gb/s DAC-DSP-based Transmitter with Adaptive Retiming Clock Optimization Using Inverse-PR-based PD Achieving 8-UI Converge Time in 28-nm CMOS**

报告人：韩晨曦，西安电子科技大学
指导老师：刘术彬

摘要：This paper presents a 1-56 Gb/s DAC-DSP based transmitter (TX) with 4-taps FFE. The proposed adaptive clock optimization scheme is built on the phase rotator (PR) and inverse-PR based phase detector, ensuring rapid convergence with low hardware overhead. Fabricated in a 28-nm CMOS, the TX prototype achieves the fastest clock optimization speed of 8UI with 2.8mW and 0.001-mm2 extra power and area, respectively. The total TX consumes 173mW at 56-Gb/s PAM4 signaling with 97.8% RLM in 0.25 mm2 area.

P77 海报题目：**A 19.58-to-21.38-GHz Low-Power Quad-Core VCO with Compact 3rd-Order Q-boost Inductors Achieving -191.8-dBc/Hz FoM and -205.4-dBc/Hz FoMA**

报告人：孔祥键，广东工业大学
指导老师：郭春炳

摘要：This paper proposes a quad-core VCO utilizing our developed 3rd -order Q-boost inductor technique. The equivalent Q and inductance can be greatly enhanced by setting three coils in-phase coupling with each other, and the distributed layout improves the area efficiency due to the multi-core floor plan. Therefore, a low-PN, low-power, and compact VCO is realized scoring −132.7dBc/Hz PN at 10 MHz offset, 4.85−mW power consumption, 0.044−mm2 core area, −191.8dBc/Hz figure-of-merits (FoM) and −205.4dBc/Hz area-figure-of-merits (FoMA), when oscillating at 19.9 GHz.

P78 海报题目：**An Energy-Efficient Composite Phase Shift 16-QAM Frequency Multiplying TX Achieving a 3.4% EVM in 65nm CMOS**

报告人：刘瑞，南方科技大学
指导老师：呼唤

摘要：Next-generation bioelectronic/IoT devices demand highly-integrated wireless systems at extremely low cost and high energy efficiency, where the transmitter (TX) often dominates the overall power consumption, posing a major design challenge to the entire system. Although sub-GHz TXs with sub-mW power consumption have been reported recently [1–3], the simple modulation scheme (OOK, FSK, etc.) limits the spectral efficiency and data rate, while is not well-suited for applications, such as brain-computer interface, real time image transmission, etc. Therefore, a QAM architecture is usually desired with an expected data rate up to tens of Mbps. State-of-the art QAM-modulated sub-GHz TX architectures can be categorized as follow. Conventional direct-conversion architecture in Fig. 1(a) provides excellent error-tolerable performance at the expense of extra power/hardware overhead. The quadrature structure in [4] modulates phase/amplitude separately by leveraging a multi-phase PLL or injection-locked ring oscillator (ILRO) [Fig. 1(b)(c)], however, requires precise phase/amplitude control to achieve good error vector magnitude (EVM). In [5], the QAM signal is generated by combining two adjacent vectors through a RF-DAC in a polar-like structure. Despite extra power saving, it suffers from significant phase/amplitude mismatch and limited EVM. In this paper, we proposed an ultra-low power 16-QAM TX based on the composite phase shift (CPS) technique. The modulation scheme in this paper demonstrates excellent mismatch-resilient performance as analyzed in the following part, resulting in an

improved EVM at the target data rate with high energy efficiency and low hardware overhead.

P79 海报题目：**Compact Full-Duplex Receiver with Wideband Multi-Domain Hilbert-Transform-Equalization Cancellation Based on Multi-Stage APFs Achieving 65dB SIC Across 120MHz BW**

报告人：马星宇，复旦大学

指导老师：李巍

摘要： A 0.5-5GHz FD RX with wideband multi-domain HTE cancellation based on multi-stage APFs is presented. Cascaded low noise 1st-order APF and 2nd-order APF with Gm and Q tunability are proposed in cancellers to meet >120MHz bandwidth and required gain/delay flatness. The FD RX achieves 34-39.7 dB SIC for 80MHz modulated signal with NF degradation of 1.2-2.1dB, while occupying only 0.5 mm2 active chip area. For 120MHz BW, total SIC of 65.1dB is measured with initial circulator isolation of 28dB.

P80 海报题目：**A Type-II Reference-Sampling PLL with Non-Uniform Octuple-Sampling Phase Detector Achieving 55-fs JitterRMS, –91.9-dBc Reference Spur and –259-dB Jitter-Power FOM**

报告人：任洪宇，中国科学院微电子研究所

指导老师：杨尊松

摘要： A type-II reference-sampling phase-locked loop (PLL) with a non-uniform octuple-sampling phase detector (PD) is proposed to lower the PD's in-band phase noise without raising the PLL's input load and crystal oscillator's power consumption. A low-noise multi-modulus divider and clock generator are utilized to generate sampling clocks without power-hungry retimers, further improving the jitter-power Figure-of-Merit (FOM). With a 150-MHz input reference, the prototype in 28-nm CMOS achieves an RMS jitter of 55fs and a FOM of −259dB with a spur level of −91.9dBc. The total power consumption is 3.34mW at 4.8GHz.

P81 海报题目：**A 0.65V-VDD 10.4-11.8GHz Fractional-N Sampling PLL Achieving 73.8fsRMS Jitter, -271.5dB FoMN, and -61dBc In-band Fractional Spur in 40nm CMOS**

报告人：沈鑫宇，中国科学院大学

指导老师：张钊

摘要： In this paper, we propose a 0.65V-VDD 10.4-to-11.8GHz FN sampling PLL (LVFN-SPLL) [Fig. 19.8.1(bottom)] achieving 73.8fsrms jitter, -271.5dB division-N FoM (FoMN), and a -61dBc in-band fractional spur. The QE is compensated by the LV coarse DTC (LVC-DTC) and fine resistor-based DAC (R-FDAC). It features: 1) a hybrid cascaded DPD (HC-DPD) to compensate the INL of the LV-C-DTC and SPD concurrently with little noise folding and significantly reduced hardware overhead, compared to the conventional DPD; 2) LV-C-DTC to reduce the DTC-induced PN at low VDD; 3) using the negative low-level inverter (NL-INV), the LV-SPD achieves reduced noise and INL with better voltage headroom, thus further lowering the in-band PN and DPD hardware overhead, and reducing the VDD sensitivity.

P82 海报题目：**A 47.3-to-58.4GHz Differential Quasi-Class-E Colpitts Oscillator Achieving 198.8dBc/Hz FoMT**

报告人：宋昌汶权，香港中文大学(深圳)

指导老师：吴亮

摘要： A mm-wave single-core VCO is reported. Instead of relying on harmonic extraction or multi-core

coupling, the PN is significantly improved by Quasi-Class-E Colpitts oscillation based on a two-port resonator. It enables fundamental oscillation, waveform shaping for power efficiency enhancement, and PN suppression. The 40nm CMOS prototype measures an FTR of 47.3 to 58.4GHz (21.1%) and PN from –124.9 to –119.8 at 10MHz offset with 5.5 to 10.5 mW power consumed, achieving 198.8dBc/Hz peak FoMT.

P83 海报题目：**A 4-26 Gbaud Configurable Multi-Mode Non-Uniform EOM with Improved Twin PI for High-Speed Wireline Communication Achieving 3-μs EW/EH Evaluation and 0.99-R2 Accuracy**

报告人：苏宪霆，西安电子科技大学
指导老师：刘术彬

摘要：This paper presents a configurable multi-mode eyeopening monitor (EOM) with non-uniform sampling and quantization for on-chip high-speed link built-in-self-test (BIST). The EOM can operate in three modes, enabling it to not only capture the colored eye diagram but also rapidly outline its contour, eye height (EH), and eye width (EW). In the non-uniformscanning mode (NSM), the EH and EW are swiftly measured using an optimization algorithm to adjust the control codes of a 7-bit twin phase interpolator (PI) and a 6-bit R-2R digital-to-analog converter (DAC). In the fast-multi-sampling mode (FMSM), the reduced number of sampled error bits in each pixel facilitates a prompt generation of the eye contour. The EOM can also reconstruct the eye diagram in the multi sampling mode (MSM) by analyzing the probability density function (PDF) of a 128×63 pixel array. Fabricated in 28-nm CMOS technology, the EOM can operate in 4-26 Gbaud within 0.005-mm² area. At 26 Gbaud, it consumes 14.55 mW with 0.99-R2 accuracy and takes up 933 μs in the MSM, 597 μs in the FMSM, and ~3 μs in the NSM, respectively.

P84 海报题目：**A Compact 90–180 GHz, 15–18 dBm Power Amplifier With Novel Self-Shielding Load-Open Balun and Broadband Fourth-Order LC Ladder Power Combiner in 28-nm CMOS**

报告人：唐大伟，东南大学
指导老师：洪伟

摘要：This article presents a compact four-way six-stage power amplifier (PA) operating in the 90–180 GHz range with 15–18 dBm saturated output power (Psat) in 28-nm bulk CMOS. A compact neutralized amplifier core utilizing a modified MOS capacitor is proposed, achieving a fourfold size reduction. The output network features a three-conductor self-shielding loadopen (SSLO) balun-based dual LC-tank, and a slow wave coplanar waveguide (CPW) based 4th-order LC ladder, achieving a total loss of less than 2.5 dB. Staggered transformer-based broadband matching is employed to achieve a flat gain of 20 dB. At input, a parallel winding balun-based 1-to-8 power splitter is introduced to provide balanced power distribution. Measurements indicate that the PA achieves a maximum smallsignal gain of 21 dB and delivers Psat more than 15 dBm, peaking at 18 dBm at 140 GHz. Compared to the state-of-the-art, this PA offers the widest operating band among F-band and D-band silicon-based PAs with comparable Psat, making it a promising candidate for high data rate and long-distance communication in D-/F-bands.

P85 海报题目：**An 8-to-28GHz 8-Phase Clock Generator Using Dual-Feedback Ring Oscillator in 28nm CMOS**

报告人：田野辰，复旦大学
指导老师：闫娜

摘要：This work proposes an 8-phase 8-28GHz clock generator consisting of a dual-feedback ring oscillator injection locked by a delay locked loop. The dual-feedback ring oscillator decouples the

feedback loop setting the frequency and the feedback loop locking the phases, thus significantly expanding the maximum operation frequency. Fabricated in a 28nm CMOS process, the 8-phase clock generator maintains the output jitter less than 40fs and the maximum phase error less than 3° across 8-28GHz.

P86 海报题目：**A W-Band Scalable 1×4 Phased-array Transmitter Front-end with >15/17 dBm OP1dB/Psat in SiGe BiCMOS**

报告人：王宗祥，东南大学
指导老师：陈继新

摘要：This paper designs and implements a W-band scalable 1×4 phased-array transmitter (TX) front-end (FE) with a linearity-enhanced power amplifier (PA). Each channel of the TX FE integrates a phase-inverting variable gain amplifier (PI-VGA) for fast 180° phase reversal, a 6-bit high-resolution phase shifter (PS) covering 0° to 360° and a linearity-enhanced PA based on two-path power combining architecture. In addition, a stability-enhanced technique and a compact power splitter are used in the design of the PA. The digital Serial Peripheral Interface (SPI) network is integrated in the TX FE and each channel can be controlled independently. Three shielded Wilkinson power dividers (WPDs) are adopted at the input of the TX FE to realize four-way power distribution. Benefiting from the high-performance PA, the OP1dB and Psat per channel are 15.6 dBm and 17.6 dBm respectively at 94 GHz. An 18 Gbps wireless data rate using 64-quadratic-amplitude modulation (QAM) is completed by the TX FE, which is higher compared with other state-of-the-art W-band phased-array transceivers (TRXs) and TRX FEs.

P87 海报题目：**A2×24 Gb/s Single-Ended Transceiver With Channel-Independent Encoder-Based Crosstalk Cancellation in 28-nm CMOS**

报告人：吴泓志，南方科技大学
指导老师：潘权

摘要：This article presents a mode decomposition encoder-based crosstalk cancellation (EB-XTC) scheme with orthogonal quasi-transverse electromagnetic (quasi-TEM) wave transmission that improves signal integrity (SI) across a pair of closely coupled differential channels for low-cost single-ended multiple input multiple output (SE-MIMO) applications. It achieves a nearly 100% crosstalk-induced jitter (CIJ) reduction ratio while relieving the pressure of the equalizer without channel dependence. To verify the scheme, a SE transceiver (TRX) is implemented in 28 nm CMOS. It consists of an encoding transmitter (TX) with a reconfigurable fractional-spaced feed-forward equalizer (FS-FFE) and a decoding receiver (RX) with a continuous-time linear equalizer (CTLE). The proposed FS-FFE reduces the number of source-series-terminated (SST) driver slices while ensuring sufficient resolution, thus reducing the chip area overhead and extending the bandwidth by 40%. Validated with 4-and 10-in differential channels, the wire-bonding packaged TRX operates up to 24 Gb/s/p-i-n at a bit error rate (BER) < 1e − 12 and compensates for up to − 2 dB far-end crosstalk and 20 dB Nyquist loss with 2.9 pJ/bit energy efficiency.

P88 海报题目：**A 278-348 GHz 6th Harmonic Injection Locking Frequency Multiplier based on 3rd Harmonic Injection Locking Oscillator in 130 nm SiGe Process**

报告人：严铮，东南大学

指导老师：陈继新 陈喆

摘要：This paper presents a 3rd ILO and a 6th ILFM fabricated in 130-nm SiGe BiCMOS technology. A hybrid-Colpitts model has been proposed to improve the conventional model of the Colpitts oscillator above 100 GHz. The 3rd ILO can be locked from 285 GHz to 345 GHz and the 6th ILFM can be locked from 278 GHz to 348 GHz. The maximum output power of the 3rd ILO is 1.1 dBm at 285 GHz with a peak DC-RF efficiency of 1.92% and the maximum output power of the 6th ILFM is 1.33 dBm at 288 GHz with a peak DC-RF efficiency of 1.5%. The 3-dB BW of the 6th ILFM is from 278 to 333 GHz. To the best knowledge of the authors, the measured locking range of 70GHz (22.3%) and the 3-dB BW of 55 GHz (18%) are the widest for the reported injection locking signal sources above 100 GHz.

P89 海报题目：**A 6.8-to-14.4GHz Octave-Tuning Fractional-N Charge-Pump PLL with Slide-Dithering-Based Background DTC Nonlinearity Calibration for Near-Integer Fractional Spur Mitigation Achieving 78fs RMS Jitter and -258.6dB FoMT**

报告人：叶宗霖，电子科技大学

指导老师：王政

摘要：Driven by emerging applications in wireless communication systems, the demand for fractional-N phase-locked loop (PLL) to exhibit better rms jitter, lower spurious tones and higher figure-of-merit (FoM) is becoming more and more indispensable. As the rms jitter is approaching sub-100fs, the discrete jitter contributed by the fractional spur is becoming dominant. Oigital-to-time converter (DTC) is usually used to cancel the quantization error (QE) in fractional-N PLLs so as to mitigate fractional spurs. Moreover, the linearity of the DTC is of vital importance to effectively cancel the QE. However, improving the linearity of the DTC involves sacrificing its thermal noise performance. Hence, a DTC nonlinearity calibration (NLC) is urgently desired. Even though previous work has dealt with fractional spur at MHz, the suppression of fractional spur at kHz is still challenging due to the difficulties in extracting DTC's nonlinearity fingerprint (NLF) in near-integer fractional-N channel.

P90 海报题目：**A 7.2G-16GHz ADPLL based on a Single-core Dual-mode DCO**

报告人：张宁远，北京大学

指导老师：廖怀林

摘要：This work proposed a 75.9% wide frequency tuning range (FTR), low-jitter All Digital Phase Locked Loop (ADPLL) based on a new single-core dual-mode digital controlled oscillator (DCO). The two modes of DCO consisted of Parallel-Mode and Series-Mode, demonstrating continuous frequency tuning from 6.76GHz to 16.29GHz. The coefficient of mutual inductance (k) requirement of the resonant tank was flexible and the implementation was high-frequency friendly. Fabricated in a 40nm-CMOS process, the proposed ADPLL had a frequency tuning range from 7.2GHz to 16GHz. The power consumption was 18.9 mW and the active chip area was 0.18 mm2. The RMS jitter spanned from 91.65fs to 103.8fs. The corresponding figure-of-merit tuning (FoMT) was -246.8 dB/-245.7 dB.

P91 海报题目：**A 112Gb/s 0.61pJ/b PAM-4 Linear TIA Supporting Extended PD-TIA Reach in 28nm CMOS**

报告人：张阳奕，南方科技大学

指导老师：潘权

摘要：Employing several design techniques including regulated active-input-termination TIA (AIT-TIA) and signal interpolation-based single-ended-to-differential converter (S2D) achieves the longest 0.2inch PD-TIA reach with an excellent power efficiency of 0.61pJ/bit.

P92 海报题目：**A Reference-Less CDR Using SAR-Based Frequency Acquisition Technique Achieving 55ns Constant Band-Searching Time and up to 63.64Gb/s/μs Acquisition Speed**

报告人：章宇浩，西安电子科技大学

指导老师：赵潇腾

摘要：A reference-less CDR using a SAR-based frequency acquisition (FA) technique is proposed for rapid interface setup. By identifying the frequency error polarity from the SLOW signal, the CDR achieves a constant band switching time of 55ns, setting a record for FA speed of up to 63.64 Gb/s/μs in the band switching step. With the help of the proposed charge pump, the total FA time of <150ns is achieved, which is at least 4X shorter than the existing works.

P93 海报题目：**A 200-GHz Modulable Transceiver With 35-dB TX ON/OFF Isolation and 16Gb/s Code Rate for MIMO Radar in 130nm SiGe Process**

报告人：周睿，东南大学

指导老师：陈继新

摘要：This paper presents a 200-GHz modulable transceiver for multiple-input multiple-output (MIMO) radar applications. The transmitter consists of a ×6 amplifier multiplier chain, a mode-switchable modulator, an ON/OFF-isolation-enhanced PA, and an on-chip self-filtering folded-dipole antenna. The mode-switchable modulator provides phase and amplitude modulation capabilities, suitable for achieving waveform orthogonality in MIMO radars. PA with ON/OFF isolation enhance technology can provide high switching isolation at the saturated output. To obtain a low noise figure (NF), the receiver consists of a wideband low-noise amplifier and an I/Q mixer. The measurement results show a peak output power of 10.3 dBm at 184 GHz, and a peak EIRP of 12 dBm with a 4-dB bandwidth from 180 to 232 GHz without lens. The receiver exhibits 24 dB conversion gain and 12 dB single sideband NF. Furthermore, phase and amplitude modulation ability is demonstrated by a Non-Return-to-Zero (NRZ) signal with 35-dB ON/OFF isolation and 16 Gb/s code rate.

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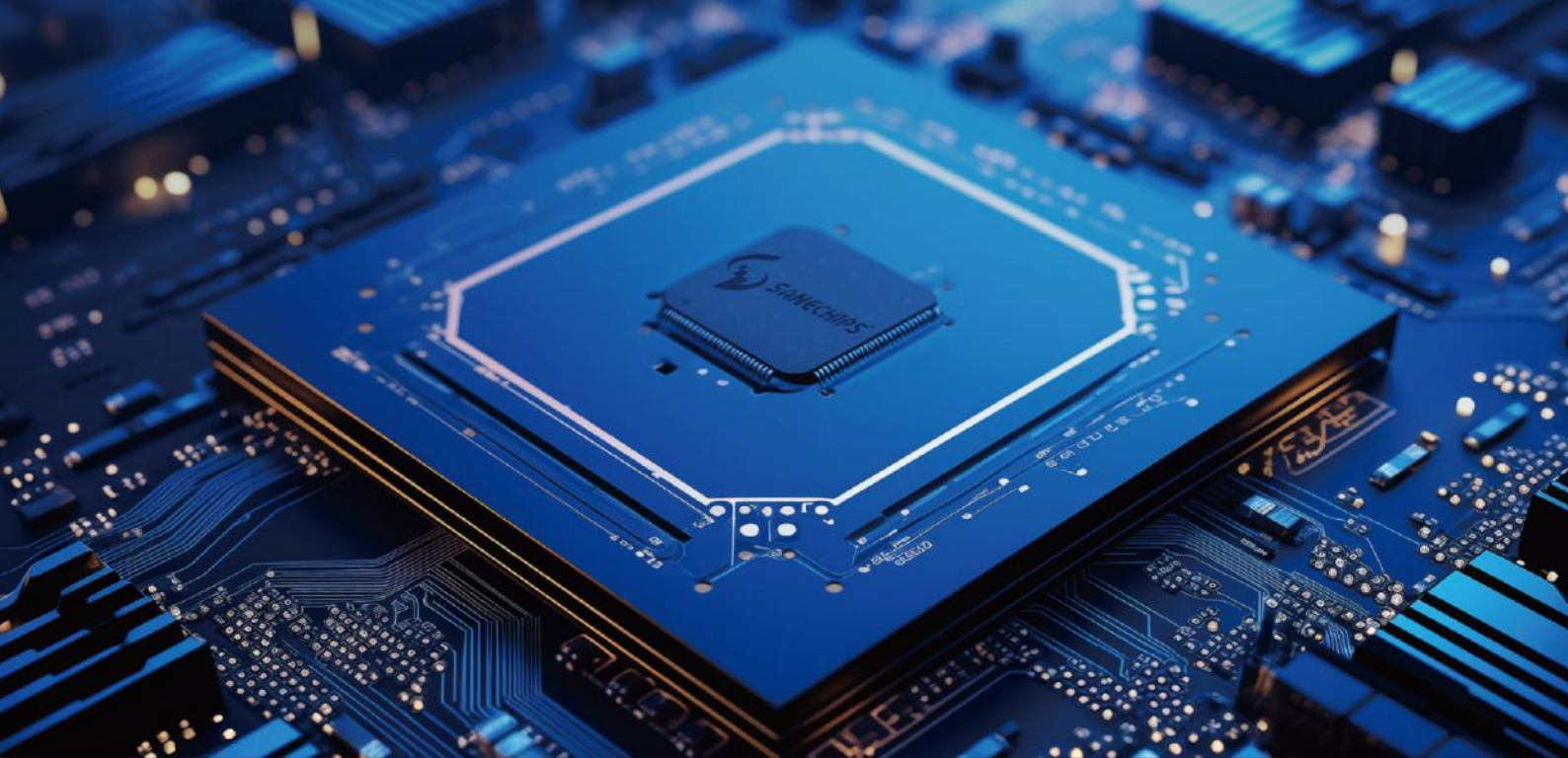

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